F81216AD

LPC to 4 UART + 9-bit Protocol

Release Date: July, 2008
Version: V0.20P

F81216AD Datasheet Revision History

Version	Date	Page	Revision History
V0.20P	2008/7/24	-	Release Version

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1. General Description

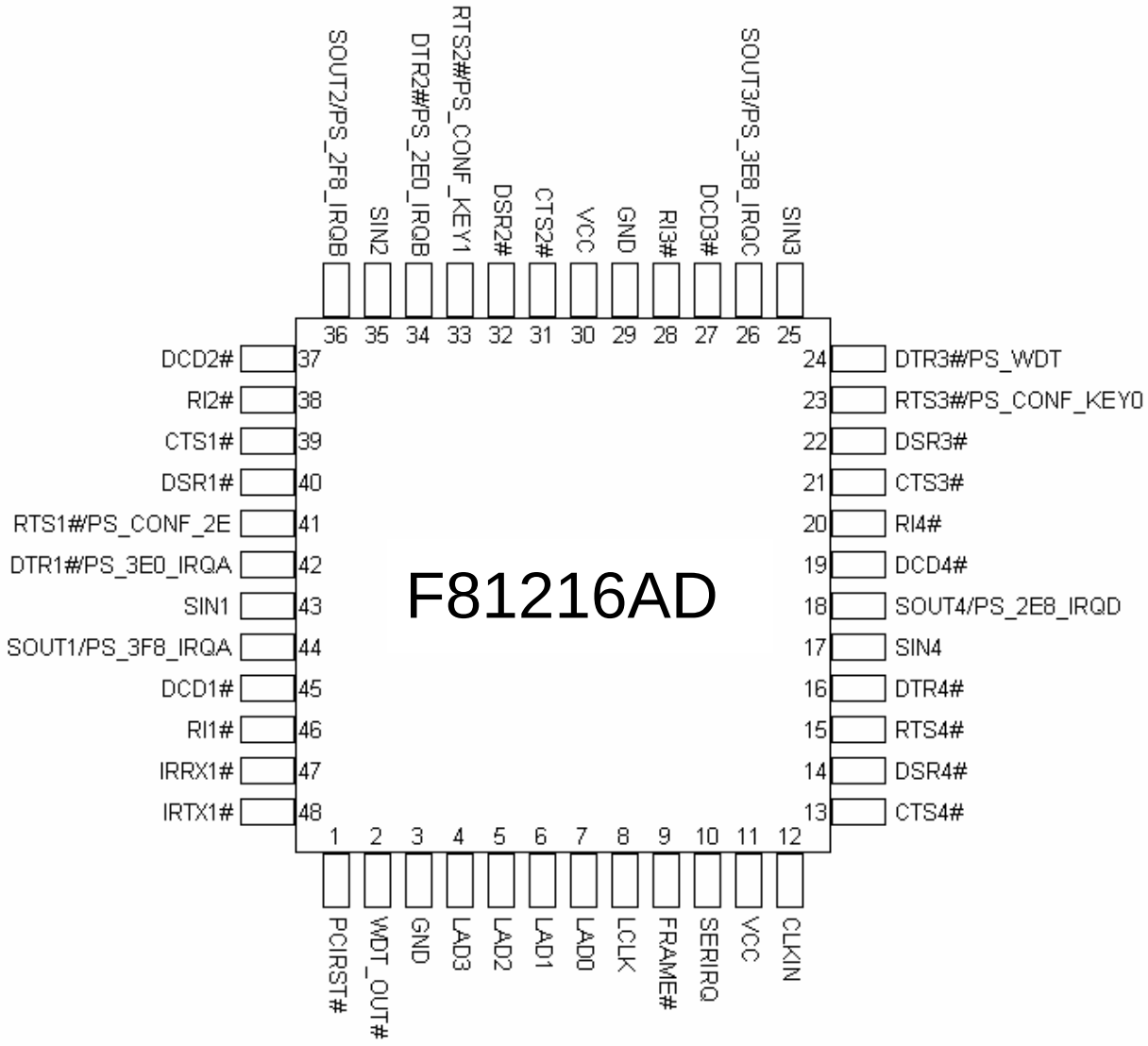
The F81216AD mainly provides 3 pure UART ports and one UART+ IR port through LPC. Each UART includes 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and an interrupt system.

One watch dog timer is provided for system controlling and the time interval can be programmed by register or hardware power on setting pin. One clock 24/48MHz input is necessary, and default is 24MHz. Powered by 3.3V voltage, the F81216AD is in the small 48pin LQFP package (7mm x 7mm).

2. Feature List

- Supports LPC interface
- Totally provides 4 UART (16550 asynchronous) ports
  - 3 Pure UART
  - 1 UART+IR
- 1 watch dog timer with WDTOUT# signal
- Support 9-bit protocol
- 1 frequency input 24/48MHz
- Powered by 3Vcc
- Operation current under 10mA
- 48-LQFP(7mm x 7mm)

3. Pin Configuration



4. Pin Description

$I/O_{8t5V-d100}$ - TTL level bi-directional pin with 8 mA source-sink capability, 5V tolerance, pull-down 100K ohms
I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/OD_{12} - TTL level bi-directional pin, Open-drain outpu with 12 mA sink capability
PCI_{5V} - bi-direction pin, slew rate control, 5V tolerance.
OUT_{12} - Output pin with 12 mA source-sink capability
OD_{12} - Open-drain output pin with 12 mA sink capability
IN_t - TTL level input pin
IN_{t5V} - TTL level input pin and 5V tolerance.
IN_{ts} - TTL level input pin and schmitt trigger
IN_{ts5V} - TTL level input pin and Schmitt trigger, 5V tolerance.
P - Power

4.1 ISA/LPC Interface

Pin No.	Pin Name	Type	Description
1	PCIRST#	IN_{ts}	System PCI reset active low.
2	WDT_OUT#	OD_{12}	Watch dog timer output. When pin 24 power on setting PS_WDT=0(default), Watch Dog timer time interval setting is programmed by register. Once power on setting PS_WDT=1, watch dog timer time interval will be fixed to 10 sec.
4~7	LPC_LAD[3:0]	PCI_{5V}	When in LPC mode, these signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
8	LCLK	IN_{ts5V}	In LPC mode, this pin acts as PCI clock input.
9	FRAME#	IN_{ts5V}	In LPC mode, indicates start of a new cycle or termination of a broken cycle.
10	SERIRQ	PCI_{5V}	In LPC mode, Serial IRQ input/Output.
12	CLKIN	IN_{t5V}	Clock Input

4.2 UART Interface

Pin No.	Pin Name	Type	Description
13	CTS4#	IN_{t5V}	Clear To Send is the modem control input.
14	DSR4#	IN_{t5V}	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
15	RTS4#	$I/O_{8t5V\text{-}d100}$	UART 4 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
16	DTR4#	$I/O_{8t5V\text{-}d100}$	UART 4 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
17	SIN4	IN_{t5V}	Serial Input. Used to receive serial data through the communication link.
18	SOUT4	$I/O_{8t5V\text{-}d100}$	UART 4 Serial Output. Used to transmit serial data out to the communication link.
	PS_2E8_IRQD		Power setting pin to define the IRQD index. **Default PS_2E8_IRQD = 0**, IRQF index is programmed by register. If PS_2E8_IRQD = 1, setting IRQF index to 0x2E8.
19	DCD4#	IN_{t5V}	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
20	RI4#	IN_{t5V}	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
21	CTS3#	IN_{t5V}	Clear To Send is the modem control input.
22	DSR3#	IN_{t5V}	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
23	RTS3#	$I/O_{8t5V\text{-}d100}$	UART 3 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	PS_CONF_KEY0		Power on configuration setting pin. As for detail description, please refer to register description.
24	DTR3#	$I/O_{8t5V\text{-}d100}$	UART 3 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	PS_WDT		Power on setting pin to enable the watch dog timer. **Default PS_WDT=0**, WDT time programmed by register. When PS_WDT=1, WDT time is defined as 10 sec.

25	SIN3	IN_{t5V}	Serial Input. Used to receive serial data through the communication link.
26	SOUT3	$I/O_{8t5V-d100}$	UART 3 Serial Output. Used to transmit serial data out to the communication link.
	PS_3E8_IRQC		Power setting pin to define the IRQC index. **Default PS_3E8_IRQC = 0**, IRQF index is programmed by register. If PS_3E8_IRQC = 1, setting IRQC index to 0x3E8.
27	DCD3#	IN_{t5V}	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
28	RI3#	IN_{t5V}	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
31	CTS2#	IN_{t5V}	Clear To Send is the modem control input.
32	DSR2#	IN_{t5V}	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
33	RTS2#	$I/O_{8t5V-d100}$	UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	PS_CONF_KEY1		Power on configuration setting pin. As for detail description, please refer to register description.
34	DTR2#	$I/O_{8t5V-d100}$	UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	PS_2E0_IRQB		Power setting pin to define the IRQB index. **Default PS_2E0_IRQB = 0**, IRQB index is programmed by register. If PS_2E0_IRQB = 1, setting IRQB index to 0x2E0.
35	SIN2	IN_{t5V}	Serial Input. Used to receive serial data through the communication link.
36	SOUT2	$I/O_{8t5V-d100}$	UART 2 Serial Output. Used to transmit serial data out to the communication link.
	PS_2F8_IRQB		Power setting pin to define the IRQB index. **Default PS_2F8_IRQB = 0**, IRQB index is programmed by register. If PS_2F8_IRQB = 1, setting IRQB index to 0x2F8.

37	DCD2#	IN_{t5V}	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
38	RI2#	IN_{t5V}	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
39	CTS1#	IN_{t5V}	Clear To Send is the modem control input.
40	DSR1#	IN_{t5V}	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
41	RTS1#	$I/O_{8t5V-d100}$	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	PS_CONF_2E		Power on configuration setting. Default PS_CONF_2E = 0, setting the configuration to 0x4E. If PS_CONF_2E =1, setting the configuration to 0x2E.
42	DTR1#	$I/O_{8t5V-d100}$	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
	PS_3E0_IRQA		Power setting pin to define the IRQA index. **Default PS_3E0_IRQA = 0,** IRQB index is programmed by register. If PS_3E0_IRQA = 1, setting IRQA index to 0x3E0.
43	SIN1	IN_{t5V}	Serial Input. Used to receive serial data through the communication link.
44	SOUT1	$I/O_{8t5V-d100}$	UART 1 Serial Output. Used to transmit serial data out to the communication link.
	PS_3F8_IRQA		Power setting pin to define the IRQA index. **Default PS_3F8_IRQA = 0**, IRQA index is programmed by register. If PS_3F8_IRQA = 1, setting IRQA index to 0x3F8.
45	DCD1#	IN_{t5V}	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
46	RI1#	IN_{t5V}	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
47	IRRX1	IN_{ts5V}	Infrared Receiver input.
48	IRTX1	OUT_{12}	Infrared Transmitter Output.

4.3 Power

Pin No.	Pin Name	Type	Description
11,30	VCC	P	3.3V power supply.
3, 29	GND	P	Ground.

5. Functional Description

The F81216AD totally provides 4 UART ports through LPC interface. Among 4 UART ports, one ports can support serial infrared communication. Besides, each UART includes 16-byte send/receive FIFO, a programmable baud rate generator, completed modem control capability and interrupt system.

One watch dog timer is provided for system controlling and the time interval can be programmed by register or hardware power on setting pin.

This IC needs one clock 24/48MHz input, and default is 24MHz. Powered by 3.3V voltage, the F81216AD is in 48 pin LQFP

5.1 LPC Interface

The F81216AD can support LPC interface serving as a bus interface between host (chipset) and peripheral (I/O chip) by hardware trapping. This interface provides much less pins and more efficient transmission. Data transfer on the LPC bus is serialized over a 4 bit bus. The general characteristics of the interface implemented in F81216AD are listed as below:

- One control line, namely LPC_FRAME#, which is used by the host to start or stop transfers. No peripherals drive this signal.
- The LPC_LAD[3:0] bus, which communicates information serially. The information conveyed is cycle type, cycle direction, chip selection, address, data, and wait states.
- PCIRST# is an active low reset signal.
- An additional 33 MHz PCI clock is needed in the F81216AD for synchronization.
- Interrupt requests are issued through LPC_SERIRQ.

5.2 UART

A Universal Asynchronous Receiver/Transmitter (UART) is used to implement serial communication. The F81216AD incorporates four fully function UART compatible with NS16550D. The UART ports perform serial to parallel conversion on receiving characters and parallel to serial conversion on transmitting characters. The controllable characteristics of the

data transmission are baud rate, number of information bits per character, type of parity checking, number of stop bits and breaking the transmission. The serial format is a start bit, followed by five to eight data bits, a parity bit(if programmable), and one, one and half, or two stop bits. The UART also includes completed modem control capability and interrupt system that may be software trailed to the computing time required to handle the communication link. The UART also has a FIFO mode to reduce the number of interrupts presented to the CPU. In the UART, there is 16-byte FIFO for both receive and transmit mode.

5.2.1 UART Port Register

5.2.1.1 Receiver Buffer Register – Base + 0

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	RBR[7:0]	R	The data received . Read only when LCR[7] is 0

5.2.1.2 Transmitter Holding Register – Base + 0

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	THR[7:0]	W	Data to be transmitted. Write only when LCR[7] is 0

5.2.1.3 Divisor Latch (LS) – Base + 0

Power-on default [7:0] = 0x01h.

Bit	Name	R/W	Description
7:0	DLL[7:0]	R/W	Baud generator divisor low byte. Access only when LCR[7] is 1.

5.2.1.4 Divisor Latch (MS) – Base + 1

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	DLM[7:0]	R/W	Baud generator divisor high byte. Access only when LCR[7] is 1.

5.2.1.5 Interrupt Enable Register – Base + 1

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:4	Reserved	R/W	Return 0 when read. Access only when LCR[7] is 0
3	EDSSI	R/W	Enable Modem Status Interrupt. Access only when LCR[7] is 0.
2	ELSI	R/W	Enable Line Status Error Interrupt. Access only when LCR[7] is 0.
1	ETBFI	R/W	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR[7] is 0.
0	ERBFI	R/W	Enable Received Data Available Interrupt. Access only when LCR[7] is 0

5.2.1.6 Interrupt Identification Register – Base + 2

Power-on default [7:0] = 0x01h.

Bit	Name	R/W	Description
7	FIFO_EN	R	0 : FIFO is disabled 1 : FIFO is enabled.
6	FIFO_EN	R	0 : FIFO is disabled. 1 : FIFO is enabled.
5:4	Reserved	R	Return 0 when read.
3:1	IRQ_ID[2:0]	R	000 : Interrupt is caused by Modem Status 001 : Interrupt is caused by Transmitter Holding Register Empty 010 : Interrupt is caused by Received Data Available. 110 : Interrupt is caused by Character Timeout 011 : Interrupt is caused by Line Status..
0	IRQ_PENDN	R	1 : Interrupt is not pending. 0 : Interrupt is pending.

5.2.1.7 FIFO Control Register – Base + 2

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:6	RCVR_TRIG[1:0]	W	00 : Receiver FIFO trigger level is 1. 01 : Receiver FIFO trigger level is 4. 10 : Receiver FIFO trigger level is 8.

			11 : Receiver FIFO trigger level is 14.
5:3	Reserved	W	
2	CLRTX	W	1 : Reset the transmitter FIFO.
1	CLRRX	W	1 : Reset the receiver FIFO.
0	FIFO_EN	W	0 : Disable FIFO 1 : Enable FIFO

5.2.1.8 Line Control Register – Base + 3

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7	DLAB	R/W	0 : Divisor Latch can't be accessed. 1 : Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	1 : Transmit a break condition. 0 : Transmitter is in normal condition.
5:3	STKPAR EPS PEN	R/W	XX0 : Parity Bit is disable 001 : Parity Bit is odd. 011 : Parity Bit is even 101 : Parity Bit is logic 1 111 : Parity Bit is logic 0
2	STB	R/W	0 : Stop bit is one bit 1 : When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1:0	WLS[1:0]	R/W	00 : Word length is 5 bit 01 : Word length is 6 bit 10 : Word length is 7 bit 11 : Word length is 8 bit

5.2.1.9 MODEM Control Register – Base + 4

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:5	Reserved	R/W	Return 0 when read.
4	LOOP	R/W	0 : UART in normal condition. 1 : UART is internal loop back

3	OUT2	R/W	0 : All interrupt is disable. 1 : Interrupt is enabled/disabled by IER.
2	OUT1	R/W	Read from MSR[6] is loop back mode
1	RTS	R/W	0 : RTS# is forced to logic 1 1 : RTS# is forced to logic 0
0	DTR	R/W	0 : DTR# is forced to logic 1 1 : DTR# is forced to logic 0

5.2.1.10 Line Status Register – Base + 5

Power-on default [7:0] = 0x60h.

Bit	Name	R/W	Description
7	RCR_ERR	R	0 : No error in the FIFO when FIFO is enabled 1 : Error in the FIFO when FIFO is enabled.
6	TEMT	R	0 : Transmitter is in transmitting. 1 : Transmitter is empty.
5	THRE	R	0 : Transmitter Holding Register is not empty. 1 : Transmitter Holding Register is empty.
4	BI	R	0 : No break condition detected. 1 : A break condition is detected.
3	FE	R	0 : Data received has no frame error. 1 : Data received has frame error.
2	PE	R	0 : Data received has no parity error. 1 : Data received has parity error.
1	OE	R	0 : No overrun condition occur. 1 : A overrun condition occur.
0	DR	R	0 : No data is ready for read. 1 : Data is received .

5.2.1.11 MODEM Status Register – Base + 6

Power-on default [7:0] = 0xX0h.

Bit	Name	R/W	Description
7	DCD	R	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	Complement of RI# input. In loop back mode , this bit is equivalent to

			OUT1 in MCR
5	DSR	R	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	0 : No state changed at DCD#. 1 : State changed at DCD#.
2	TERI	R	0 : No Trailing edge at RI#. 1 : A low to high transition at RI#.
1	DDSR	R	0 : No state changed at DSR#. 1 : State changed at DSR#.
0	DCTS	R	0 : No state changed at CTS#. 1 : State changed at CTS#.

5.2.1.11 Scratch Register – Base + 7

Power-on default [7:0] = 0x00h.

Bit	Name	R/W	Description
7:0	SCR_DATA[7:0]	R/W	Scratch register.

5.3 IR Function

The F81216AD infrared interface provides a two way wireless communications port using infrared as the transmission medium. The IrDA 1.0 (SIR) is found in UART1 IrDA SIR specifies asynchronous serial communication at baud rate up to 115.2Kbps. Each byte is sent serial LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. IRTX acts as a transmit pin and IRRX acts as a receiving one. As for detail description, please refer to register description.

5.4 Watch Dog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to low level, the signal default is tri-state (need external pull up resister).

The time interval has three ways:

One is the hardware power on setting to enable, timer set to 10 second (24MHz). If 48MHz clock input, the timer is set to 5 second.

Two is programmed by registers.

The other is set the base address into registers, and use the base address the control it.

The timer unit has three kinds: 10mS, 1S, 1Min.

5.4.1 Watchdog Port Register

5.4.1.1 Timer Status and Control Register – Base + 0

Power-on default [7:0] = 0x02 when DTR3#/PS_WDT is pull-up, else 0x0.

Bit	Name	R/W	Description
7:3	Reserved	R/W	Return 0 when read.
2:1	WDT_UNIT[1:0]	R/W	00 : Timer Unit is 10ms. 01 : Timer Unit is 1 second 10 : Timer Unit is 1 minute. 11 : reserved.
0	WDT_EVENT	R/W	When read 0 : no time out occur. 1 : time out has occurred. when write 0 : no action 1 : clear the time out status.

5.4.1.2 Timer Count Number Register – Base + 1

Power-on default [7:0] = 0x0Ah when DTR3#/PS_WDT is pull-up , else 0x00h.

Bit	Name	R/W	Description
7:0	WDT_CNT[7:0]	R/W	The number of count for watchdog timer. Write the same value to enable the timer, write 0 to disable timer.

5.5 Serial IRQ

F81216AD supports a serial IRQ scheme. Because more than one device may need to share the signal serial IRQ signal line, an open drain signal scheme is used. The clock source is the PCI clock. The serial interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: a start frame, several IRQ/Data frame, and one Stop frame.

5.5.1 Start Frame

There are two modes of operation for the SERIRQ Start frame: Quiet mode and Continuous mode. In the Quiet mode, the peripheral drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the states machines of the peripherals from idle to active states. The host controller will then take over driving SERIRQ signal low in the next clock and will continue driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the SERIRQ high for one clock and then tri-states it. In the Continuous mode, only the host controller initiates the START frame to update IRQ/Data line information. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start frame.

5.5.2 IRQ/Data Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the peripheral device drives the SERIRQ high. During the Turn-around phase, the peripheral device left the SERIRQ tri-stated. The IRQ/Data Frame has a number of specific order, as shown in Table 5-1. The F81216AD is only support IRQ3, IRQ4, IRQ5, IRQ9, IRQ10, and IRQ11.

Table 5-1 IRQSER Sampling periods

IRQ/Data Frame	Signal Sampled	# of clocks past Start
1	IRQ0	2
2	IRQ1	5
3	SMI#	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26

10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47
17	IOCHCK#	50
18	INTA#	53
19	INTB#	56
20	INTC#	59
21	INTD#	62
32:22	Unassigned	95

5.5.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate SERIRQ by a Stop frame. Only the host controller can initiate the Stop frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the next SERIRQ cycle's Sample mode is the Continuous mode.

6. Register Description

Registers are programmed by port 0x4E(0x2E) and 0x4F(0x2F). 0x4E is the index port and 0x4F is the data port .

RTS1#/PS_CONF_2E	Index Port	Data Port
0 (default)	0x4E	0x4F
1	0x2E	0x2F

To enable configuration registers programming, entry key must output twice to index port continuously. The entry key is decided by power on setting pins RTS2#/PS_CONF_KEY1 and RTS3#/PS_CONF_KEY0 as following:

RTS2#/PS_CONF_KEY1	RTS3#/PS_CONF_KEY0	Entry key
0	0	0x77 (default)
0	1	0xA0
1	0	0x87
1	1	0x67

To exit configuration registers programming, output 0xAA to index port.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	0	0	0	1	0
21	Chip ID Register	0	0	0	1	0	1	1/0	0
23	Vender ID Register	0	0	0	1	1	0	0	1
24	Vender ID Register	0	0	1	1	0	1	0	0
25	Clock Select Register	-	-	-	-	-	-	-	0
27	Port Select Register	-	-	-	1/0	-	-	1/0	1/0

Device Configuration Registers

"-" Reserved or Tri-State

UART1 Device Configuration Registers (LDN CR00)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	0	1/0	1/0
61	Base Address Low Register	1/0	1/0	1/0	1/0	1/0	0	0	0
70	IRQ Channel Select Register	-	-	0	0	0	0	1/0	1/0
F0	Clock Select Register	0	0	0	0	0	0	0	0
F1	IR Control Register	-	-	-	0	0	0	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
UART2 Device Configuration Registers (LDN CR01)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	0	1/0	0
61	Base Address Low Register	1/0	1/0	1/0	1/0	1/0	0	0	0
70	IRQ Channel Select Register	-	-	0	0	0	1/0	0	0
F0	Clock Select Register	0	0	0	0	0	0	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
UART3 Device Configuration Registers (LDN CR02)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART3Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	0	1/0	1/0
61	Base Address Low Register	1/0	1/0	1/0	0	1/0	0	0	0
70	IRQ Channel Select Register	-	-	0	0	0	1/0	0	1/0
F0	Clock Select Register	0	0	0	0	0	0	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
UART4 Device Configuration Registers (LDN CR03)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	0	1/0	0

61	Base Address Low Register	1/0	1/0	1/0	0	1/0	0	0	0
70	IRQ Channel Select Register	-	-	0	0	1/0	0	0	1/0
F0	Clock Select Register	0	0	0	0	0	0	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0

WDT Device Configuration Registers (LDN CR08)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1/0
60	Base Address High Register	0	0	0	0	0	1/0	0	0
61	Base Address Low Register	0	1/0	0	0	0	0	1/0	0
70	IRQ Channel Select Register	-	-	-	0	0	0	0	0
F0	Timer Status and Control Register	-	-	-	-	-	0	1/0	0
F1	Timer Count Number Register	0	0	0	0	1/0	0	0	1/0

6.1. Global Control Registers

6.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

6.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h : Select UART 1 device configuration register 01h : Select UART 2 device configuration register 02h : Select UART 3 device configuration register 03h : Select UART 4 device configuration register 08h : Select Watchdog Timer device configuration register

6.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	02h	Chip ID 1 of F81216AD..

6.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	16h	Chip ID2 of F81216AD.

6.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1 of Fintek devices.

6.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2 of Fintek devices.

6.1.7 Clock Select Register — Index 25h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	CLK_SEL	R/W	0	1 : The CLKIN is 48MHz 0 : The CLKIN is 24MHz. This bit must program to indicate the frequency of the clock source, or the device will not function correctly.

6.1.8 Port SelectRegister — Index 27h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	PORT_4E_EN	-	-	The default value of this bit is decided by power on strap pin PS_CONF_2E. The default is “1” when PS_CONF_2E is low during power on. 0: The configuration port is 0x2E/0x2F. 1: The configuration port is 0x4E/0x4F.
3-2	Reserved	-	-	Reserved.

1-0	ENTRY_KEY_SEL	R/W	0	Configuration Entry Key Select. The default value of these bits are determined by PS_CONF_KEY1 and PS_CONF_KEY0. 00: The entry key is 0x77. 01: The entry key is 0xA0. 10: The entry key is 0x87. 11: The entry key is 0x67.

6.2. UART1 Registers (CR00)

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR1_EN	R/W	-	0: disable UART 1. 1: enable UART 1. This bit is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. The power value will “1” if an external pull up resistor is attached to SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. Otherwise, the power on value will be “0”.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	-	The MSB of UART 1 base address. This byte is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. The power on default is 0x03 if SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA is pull up. Otherwise, it is 0x00.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	-	The LSB of UART 1 base address. This byte is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. The power on default is 0xF8 if SOUT1/PS_3F8_IRQA is pull up. It is 0xE0 if DTR1#/PS_3E0_IRQA is pull up. Otherwise, it is 0x00.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	URAIRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
4	URAIRQ_SHAR	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.
3-0	SELUR1IRQ	R/W	-	Select the IRQ channel for UART 1. This byte is determined by SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA. The power on default is 0x03 if SOUT1/PS_3F8_IRQA or DTR1#/PS_3E0_IRQA is pull up. Otherwise, it is 0x00.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	9BIT_MODE_URA	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit..
6	AUTO_ADDR_URA	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_URA and SADEN_URA)

5	RTS_Invert	R/W	0	0: Default non function 1: When RS485_URA set to 1, RTS# signal will be inverted when assert out.
4	RS485_URA	R/W	0	0: RS232 mode 1: RS485 mode, which will auto assert RTS# (RTS# is low) when receiving is required..
3	RXW4C_IRA	R/W	0	0 : No reception delay when SIR is changed from TX to RX. 1 : Reception delay 4 character-time when SIR is changed from TX to RX.
2	TXW4C_IRA	R/W	0	0 : No transmission delay when SIR is changed from RX to TX. 1 : Transmission delay 4 character-time when SIR is changed from RX to TX.
1-0	SELURACLK1 SELURACLK0	R/W	00	00: UART 1 clock source is 1.8462MHz (24MHz/13) 01: UART 1 clock source is 18MHz. 10: UART 1 clock source is 24MHz. 11: UART 1 clock source is 14MHz.

IR Control Register — Index F1h

Bit	Name	R/W	Default	Description
7-5	Reserved	R	-	Return 010b when read.
4-3	IRA_MODE1 IRA_MODE0	R/W	00	0X: Disable IR1 function. 10 : Enable IR1 function, active pulse is 1.6uS. 11 : Enable IR1 function, active pulse is 3/16 bit time.
2	Half_Full_Duplex	R/W	0	0 : Full Duplex function for IR self test. 1 : Half Duplex function. Return 1 when read.
1	TXINV_IRA	R/W	0	0 : IRTX1 is not inversed. 1 : Inverse the IRTX1.
0	RXINV_IRA	R/W	0	0 : IRRX1 is not inversed. 1 : Inverse the IRRX1.

9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description

7-0	SADDR_URA	R/W	00h	This byte accompanying with SADEN_URA will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN_URA is “0”, then the corresponding bit of SADDR_URA is don’t care. 2. broadcast address: If bit n of ored SADDR_URA and SADEN_URA is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR_URA	0101_1100b
SADEN_URA	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7-0	SADEN_URA	R/W	00h	This byte accompanying with SADDR_URA will determine the given address and broadcast address in 9-bit mode. The UART_URA will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN_URA is “0”, then the corresponding bit of SADDR_URA is don’t care. 1. broadcast address: If bit n of ored SADDR_URA and SADEN_URA is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex.

SADDR_URA	0101_1100b
SADEN_URA	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

6.3. UART2 Registers (CR01)

UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR2_EN	R/W	-	0: disable UART 2. 1: enable UART 2. This bit is determined by SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB. The power value will "1" if an external pull up resistor is attached to SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB. Otherwise, the power on value will be "0".

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	-	The MSB of UART 2 base address. This byte is determined by SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB. The power on default is 0x02 if SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB is pull up. Otherwise, it is 0x00.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	-	The LSB of UART 2 base address. This byte is determined by SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB. The power on default is 0xF8 if SOUT2/PS_2F8_IRQB is pull up. It is 0xE0 if DTR2#/PS_2E0_IRQB is pull up. Otherwise, it is 0x00.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.

5	URBIRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.
4	URBIRQ_SHAR	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.
3-0	SELUR2IRQ	R/W	-	Select the IRQ channel for UART 2. This byte is determined by SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB. The power on default is 0x04 if SOUT2/PS_2F8_IRQB or DTR2#/PS_2E0_IRQB is pull up. Otherwise, it is 0x00.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	9BIT_MODE_URB	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit..
6	AUTO_ADDR_URB	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_URB and SADEN_URB)
5	RTS_Invert	R/W	0	0: Default non function 1: When RS485_URA set to 1, RTS# signal will be inverted when assert out.
4	RS485_URB	R/W	0	0: RS232 mode 1: RS485 mode, which will auto assert RTS# (RTS# is low) when receiving is required..
3-2	Reserved	R/W	0	Dummy Registers
1-0	SELURBCLK1 SELURBCLK0	R/W	00	00: UART 2 clock source is 1.8462MHz (24MHz/13) 01: UART 2 clock source is 18MHz. 10: UART 2 clock source is 24MHz. 11: UART 2 clock source is 14MHz.

9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	SADDR_URB	R/W	00h	This byte accompanying with SADEN_URB will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 3. given address: If bit n of SADEN_URB is "0", then the corresponding bit of SADDR_URB is don't care. 4. broadcast address: If bit n of ored SADDR_URB and SADEN_URB is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR_URB	0101_1100b
SADEN_URB	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7-0	SADEN_URB	R/W	00h	This byte accompanying with SADDR_URB will determine the given address and broadcast address in 9-bit mode. The UART_URB will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN_URB is "0", then the corresponding bit of SADDR_URB is don't care. 2. broadcast address: If bit n of ored SADDR_URB and SADEN_URB is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex.

SADDR_URB	0101_1100b
SADEN_URB	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

6.4. UART3 Registers (CR02)

UART 3 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR3_EN	R/W	-	0: disable UART 3. 1: enable UART 3. This bit is determined by SOUT3/PS_3E8_IRQC. The power value will "1" if an external pull up resistor is attached to SOUT3/PS_3E8_IRQC. Otherwise, the power on value will be "0".

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	-	The MSB of UART 3 base address. This byte is determined by SOUT3/PS_3E8_IRQC. The power on default is 0x03 if SOUT3/PS_3E8_IRQC is pull up. Otherwise, it is 0x00.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	-	The LSB of UART 3 base address. This byte is determined by SOUT3/PS_3E8_IRQC. The power on default is 0xE8 if SOUT3/PS_3E8_IRQC is pull up. Otherwise, it is 0x00.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	URCIRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.

4	URCIRQ_SHAR	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.
3-0	SELUR3IRQ	R/W	-	Select the IRQ channel for UART 3. This byte is determined by SOUT3/PS_3E8_IRQC. The power on default is 0x05 if SOUT3/PS_3E8_IRQC is pull up. Otherwise, it is 0x00.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	9BIT_MODE_URC	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit..
6	AUTO_ADDR_URC	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_URC and SADEN_URC)
5	RTS_Invert	R/W	0	0: Default non function 1: When RS485_URA set to 1, RTS# signal will be inverted when assert out.
4	RS485_URC	R/W	0	0: RS232 mode 1: RS485 mode, which will auto assert RTS# (RTS# is low) when receiving is required..
3-2	Reserved	R/W	0	Dummy Registers
1-0	SELURCCLK1 SELURCCLK0	R/W	00	00: UART 3 clock source is 1.8462MHz (24MHz/13) 01: UART 3 clock source is 18MHz. 10: UART 3 clock source is 24MHz. 11: UART 3 clock source is 14MHz.

9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description

7-0	SADDR_URC	R/W	00h	This byte accompanying with SADEN_URC will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 5. given address: If bit n of SADEN_URC is "0", then the corresponding bit of SADDR_URC is don't care. 6. broadcast address: If bit n of ored SADDR_URC and SADEN_URC is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_URC: 0101_1100b SADEN_URC: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7-0	SADEN_URC	R/W	00h	This byte accompanying with SADDR_URC will determine the given address and broadcast address in 9-bit mode. The UART_URC will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN_URC is "0", then the corresponding bit of SADDR_URC is don't care. 3. broadcast address: If bit n of ored SADDR_URC and SADEN_URC is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_URC: 0101_1100b SADEN_URC: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

6.5. UART4 Registers (CR03)

UART 4 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR4_EN	R/W	-	0: disable UART 4. 1: enable UART 4. This bit is determined by SOUT4/PS_2E8_IRQD. The power value will "1" if an external pull up resistor is attached to SOUT4/PS_2E8_IRQD. Otherwise, the power on value will be "0".

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	-	The MSB of UART 4 base address. This byte is determined by SOUT4/PS_2E8_IRQD. The power on default is 0x02 if SOUT4/PS_2E8_IRQD is pull up. Otherwise, it is 0x00.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	-	The LSB of UART 4 base address. This byte is determined by SOUT4/PS_2E8_IRQD. The power on default is 0xE8 if SOUT4/PS_2E8_IRQD is pull up. Otherwise, it is 0x00.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	URDIRQ_MODE	R/W	0	0 : PCI IRQ sharing mode. 1 : ISA IRQ sharing mode. This bit is effective in IRQ sharing mode.

4	URDIRQ_SHAR	R/W	0	0 : IRQ is not sharing with other device. 1 : IRQ is sharing with other device.
3-0	SELUR4IRQ	R/W	-	Select the IRQ channel for UART 4. This byte is determined by SOUT4/PS_2E8_IRQD. The power on default is 0x09 if SOUT4/PS_2E8_IRQD is pull up. Otherwise, it is 0x00.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	9BIT_MODE_URD	R/W	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit..
6	AUTO_ADDR_URD	R/W	0	This bit works only in 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR_URD and SADEN_URD)
5	RTS_Invert	R/W	0	0: Default non function 1: When RS485_URA set to 1, RTS# signal will be inverted when assert out.
4	RS485_URD	R/W	0	0: RS232 mode 1: RS485 mode, which will auto assert RTS# (RTS# is low) when receiving is required..
3-2	Reserved	R/W	0	Dummy Registers
1-0	SELURDCLK1 SELURDCLK0	R/W	00	00: UART 4 clock source is 1.8462MHz (24MHz/13) 01: UART 4 clock source is 18MHz. 10: UART 4 clock source is 24MHz. 11: UART 4 clock source is 14MHz.

9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Default	Description

7-0	SADDR_URD	R/W	00h	This byte accompanying with SADEN_URD will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 7. given address: If bit n of SADEN_URD is "0", then the corresponding bit of SADDR_URD is don't care. 8. broadcast address: If bit n of ored SADDR_URD and SADEN_URD is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_URD: 0101_1100b SADEN_URD: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Default	Description
7-0	SADEN_URD	R/W	00h	This byte accompanying with SADDR_URD will determine the given address and broadcast address in 9-bit mode. The UART_URD will response to both given and broadcast address. Follow the description to determine the given address and broadcast address: 1. given address: If bit n of SADEN_URD is "0", then the corresponding bit of SADDR_URD is don't care. 4. broadcast address: If bit n of ored SADDR_URD and SADEN_URD is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR_URD: 0101_1100b SADEN_URD: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

6.6. Watchdog Timer Registers (CR08)

Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	WDT_EN	R/W	0	0: disable WDT. 1: enable WDT. This bit is determined by DTR3#/PS_WDT. The power value will “1” if an external pull up resistor is attached to DTR3#/PS_WDT. Otherwise, the power on value will be “0”.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	-	The MSB of UART 3 base address. This byte is determined by DTR3#/PS_WDT. The power on default is 0x04 if SOUT3/PS_3E8_IRQC is pull up. Otherwise, it is 0x00.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	-	The LSB of UART 3 base address. This byte is determined by DTR3#/PS_WDT. The power on default is 0x42 if DTR3#/PS_WDT is pull up. Otherwise, it is 0x00.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	WDTIRQ_EN	R/W	0	0 : Disable WDT IRQ. 1 : Enable WDT IRQ.
3-0	SELWDTIRQ	R/W	0h	Select the IRQ channel for WDT.

Timer Status and Control Register — Index F0h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2-1	WDT_UNIT	R/W	-	00 : Timer Unit is 10ms. 01 : Timer Unit is 1 second 10 : Timer Unit is 1 minute. 11 : reserved. This register is determined by DTR3#/PS_WDT. The power on default is 0x01 if DTR3#/PS_WDT is pull up. Otherwise, it is 0x00.
0	WDT_EVENT	R/W	0	0 : no time out occur. 1 : time out has occurred. Write "1" to this bit will clear the status.

Timer Count Number Register — Index F1h

Bit	Name	R/W	Default	Description
7-0	WDT_CNT	R/W	-	The number of count for watchdog timer. Write the same non-zero value twice to enable the timer, otherwise will disable timer. This register is determined by DTR3#/PS_WDT. The power on default is 0x0A if DTR3#/PS_WDT is pull up. Otherwise, it is 0x00.

7. Electron Characteristic

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 4.0	V
Input Voltage	-0.5 to 5.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 DC Characteristics

((Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL	10	12		mA	VOL = 0.4V
Output High Current	IOH		-12	-10	mA	VOH = 2.4V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Output Low Current	IOL	10	12		mA	VOL = 0.4 V
Output High Current	IOH		-12	-10	mA	VOH = 2.4V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V

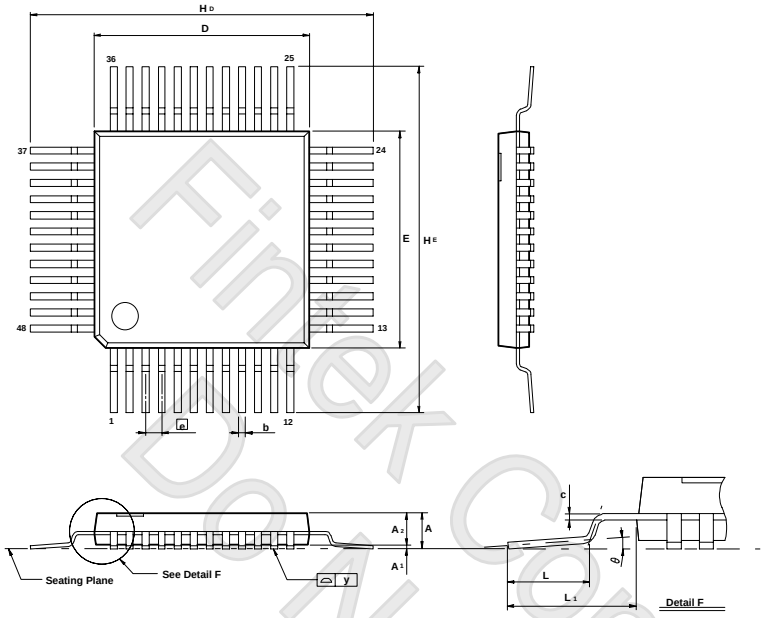
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Current	IOL	12	16		mA	VOL = 0.4V
Output High Current	IOH		-14	-12	mA	VOH = 2.4V
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Current	IOL	6	8		mA	VOL = 0.4V
OD_{16} - Open-drain output pin with sink capability of 16 mA						
Output Low Current	IOL	12	16		mA	VOL = 0.4V
I/OOD_{16ts} - TTL level bi-directional pin, can select to OD or OUT by register, with 16 mA source-sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Output Low Current	IOL	6	8		mA	VOL = 0.4 V
Output High Current	IOH		-16	-12	mA	VOH = 2.4V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0V
IN_t - TTL level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3V
Input High Leakage	ILIH			+10	μA	VIN = VDD
Input Low Leakage	ILIL			-10	μA	VIN = 0 V

8. Ordering Information

Part Number	Package Type	Production Flow
F81216AD	48 pin LQFP (Green Package)	Commercial, 0°C to +70°C

9. Package Dimensions

48pin-LQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

Feature Integration Technology Inc.

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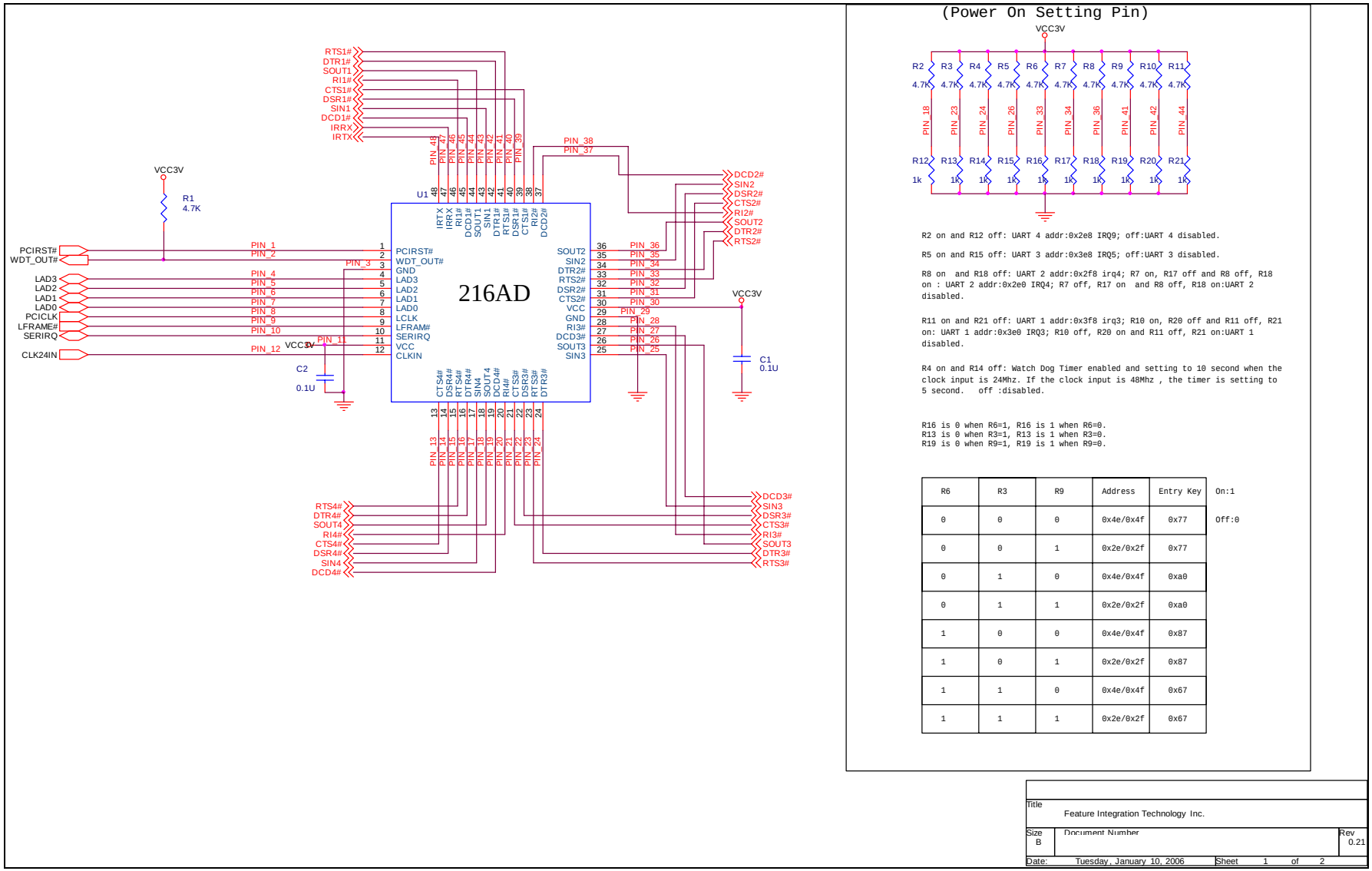
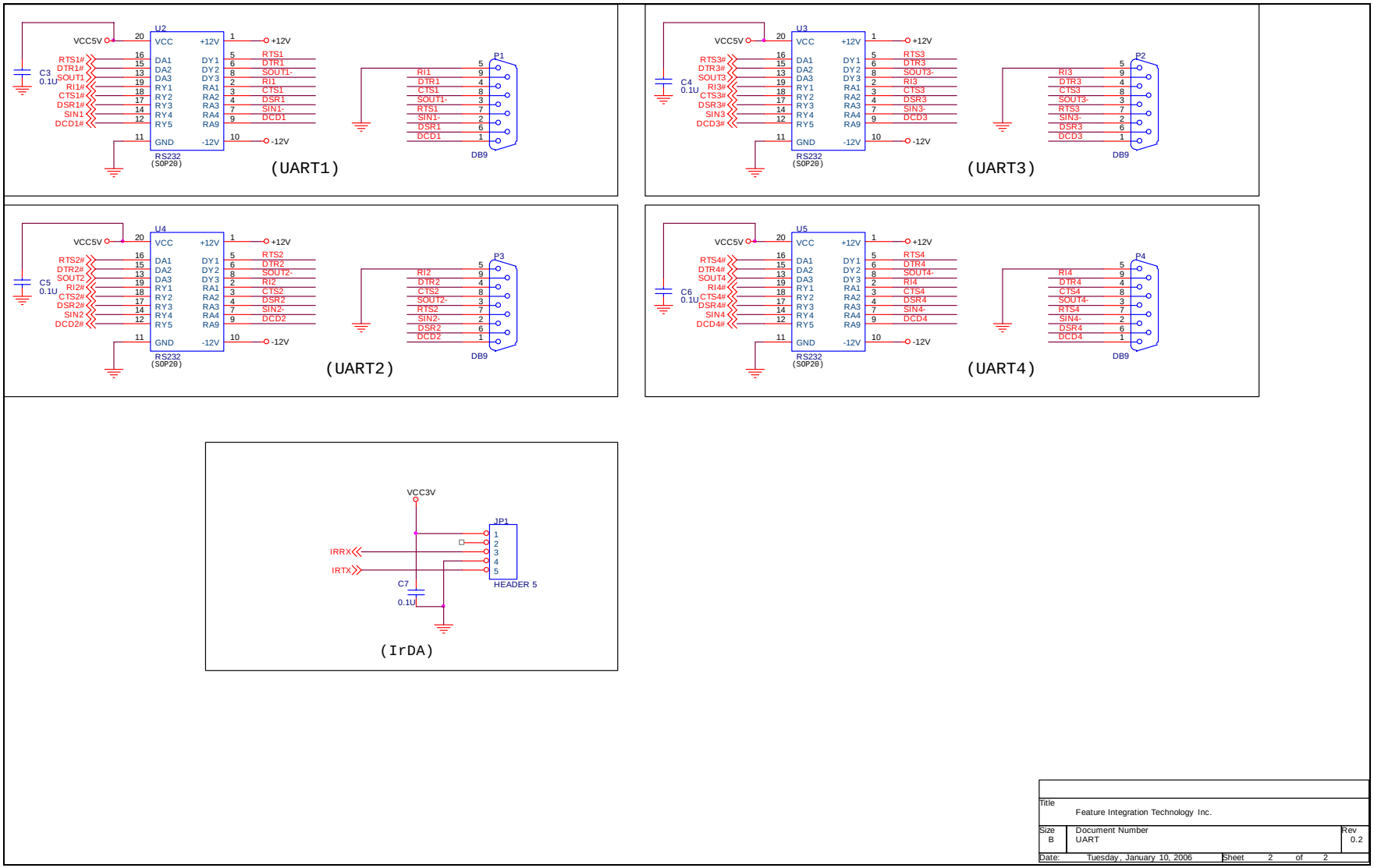
10. Application Circuit





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