

## 7-16GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

*preliminary*

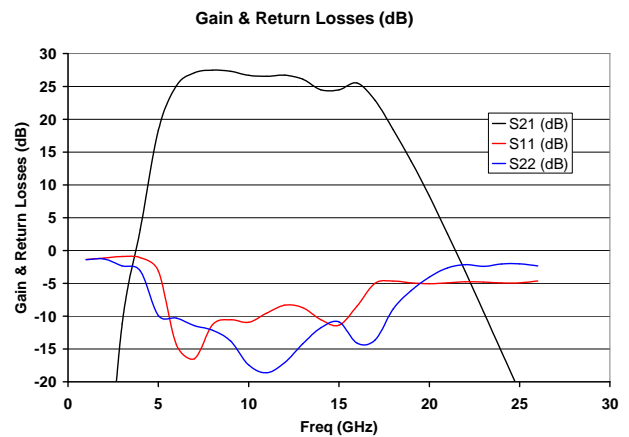
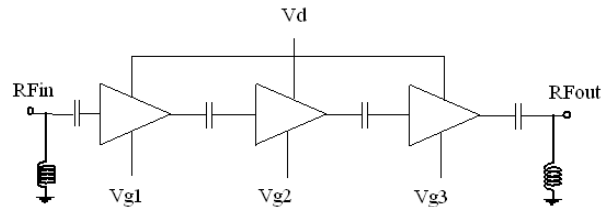
### Description

The CHA5051 is a high gain three-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.15 $\mu$ m gate length, via holes through the substrate. It is available in chip form

### Main Features

- Broadband performance 7-16GHz
- 25dB gain & 3dB noise figure
- RF ports ESD protected (see page 12)
- 25dBm output power @ 1dB compression
- DC power consumption, 310mA @ 4.5V
- Chip size 2.41 x 1.5 x 0.10mm



### Main Characteristics

Tamb.=25°C, Vd=4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		16	GHz
G	Small signal gain		25		dB
NF	Noise figure		3		dB
P1dB	Output power at 1dB gain compression		25		dBm
Id	Bias current		310		mA

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Ref: DSCHA50517152 - 01 Jun 07

1/14

Specifications subject to change without notice

*preliminary***Electrical Characteristics**T<sub>amb.</sub>=25°C, V<sub>d</sub>=4.5V I<sub>d</sub>=310mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		16	GHz
G	Small signal gain		25		dB
P1dB	Pulsed output power at 1dB compression		25		dBm
P03	Output power at 3dB gain compression		26		dBm
NF	Noise Figure		3		dB
VSWR <sub>in</sub>	Input VSWR		2.5:1		
VSWR <sub>out</sub>	Output VSWR		2:1		
IP3	Output IP3 from 7 to 13GHz from 14 to 16GHz		33 29		dBm
V <sub>d</sub>	DC voltage		4.5		V
I <sub>d</sub>	Bias current		310		mA

These values are representative for on-wafer measurements that are made without bonding wires at the RF ports.

**Absolute Maximum Ratings**T<sub>amb.</sub> = 25°C (1)

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Maximum Drain bias voltage	+5	V
I <sub>d</sub>	Drain bias current with V <sub>d</sub> =4.5V	390	mA
V <sub>g</sub>	Gate bias voltage	-2 to +0.4	V
P <sub>in</sub>	Maximum input power overdrive (2)	+10	dBm
T <sub>ch</sub>	Maximum channel temperature	+175	°C
T <sub>a</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +125	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

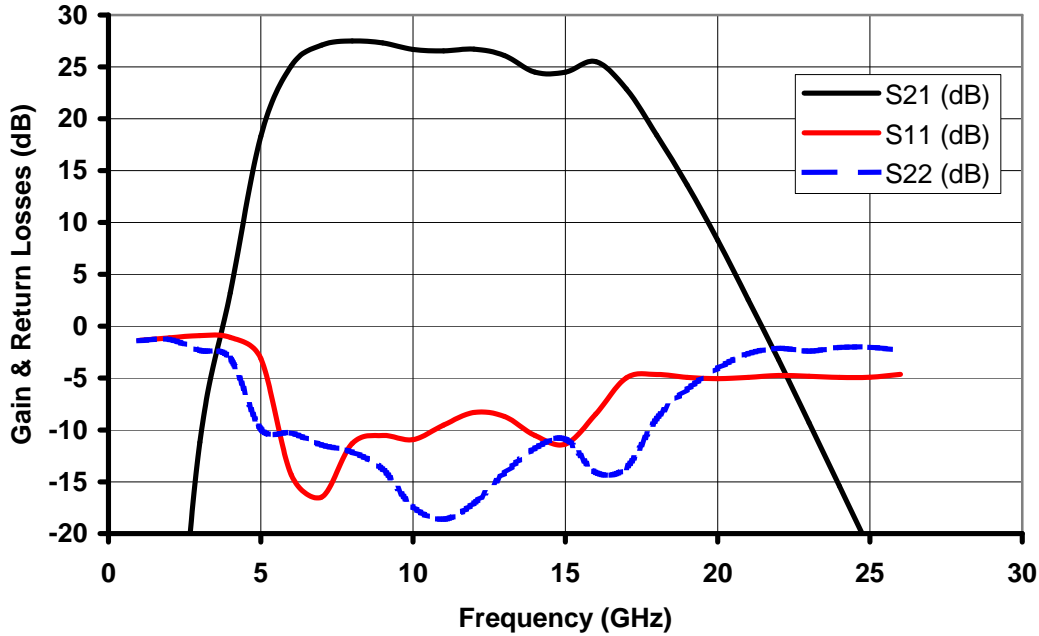
(2) Duration < 1s.

## Typical Measured Performance

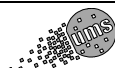
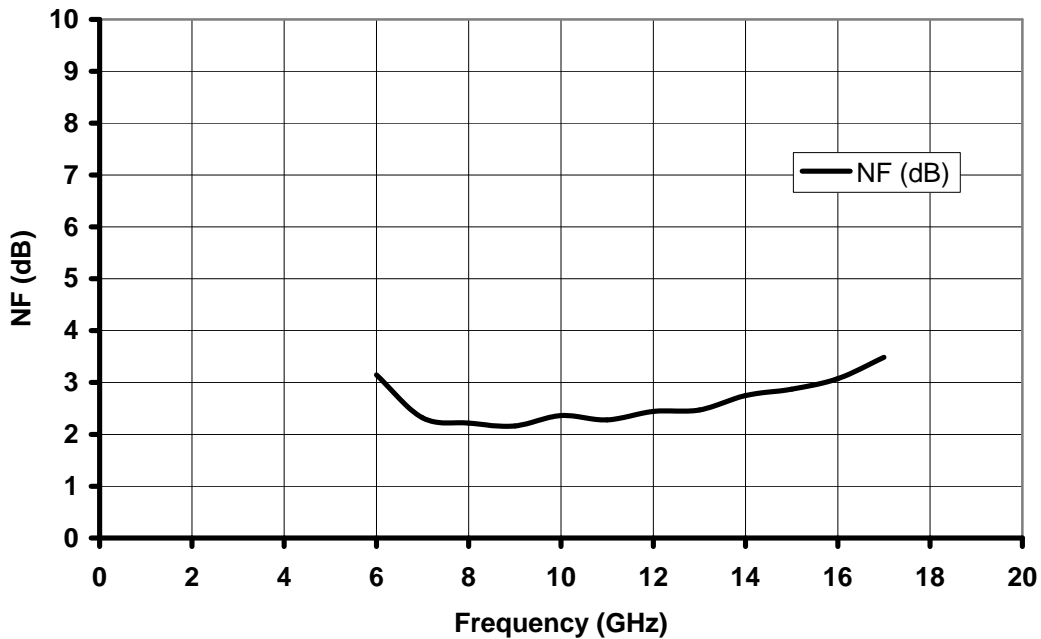
On wafer measurement (without bonding wires at the RF ports)  
Tamb.=+25°C, Vd=+4.5V Id=310mA

*preliminary*

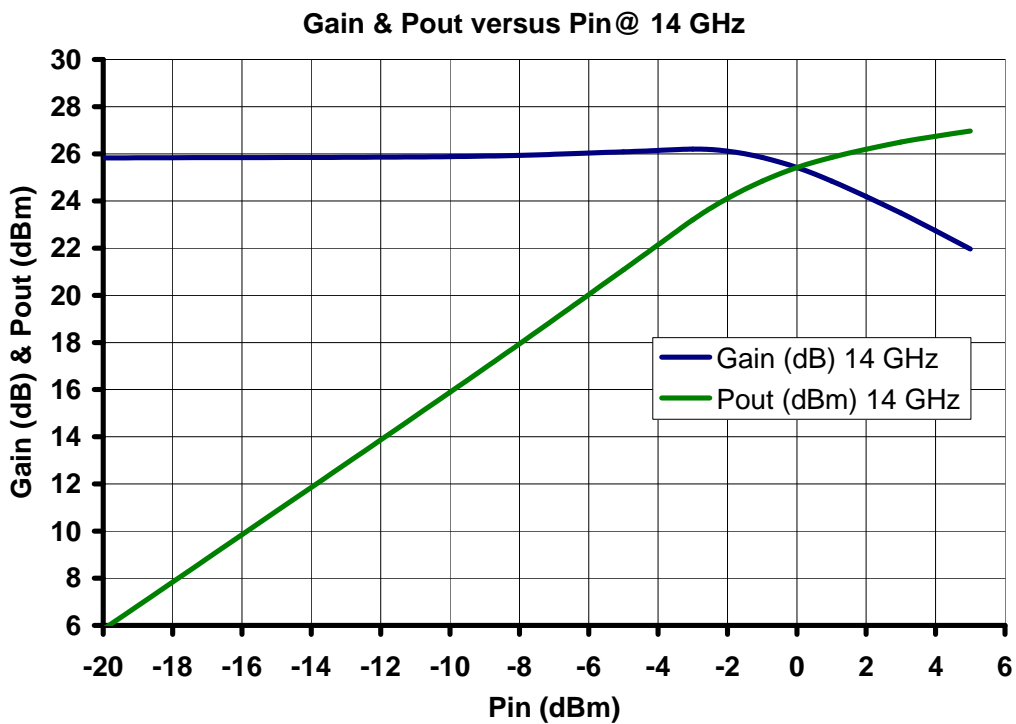
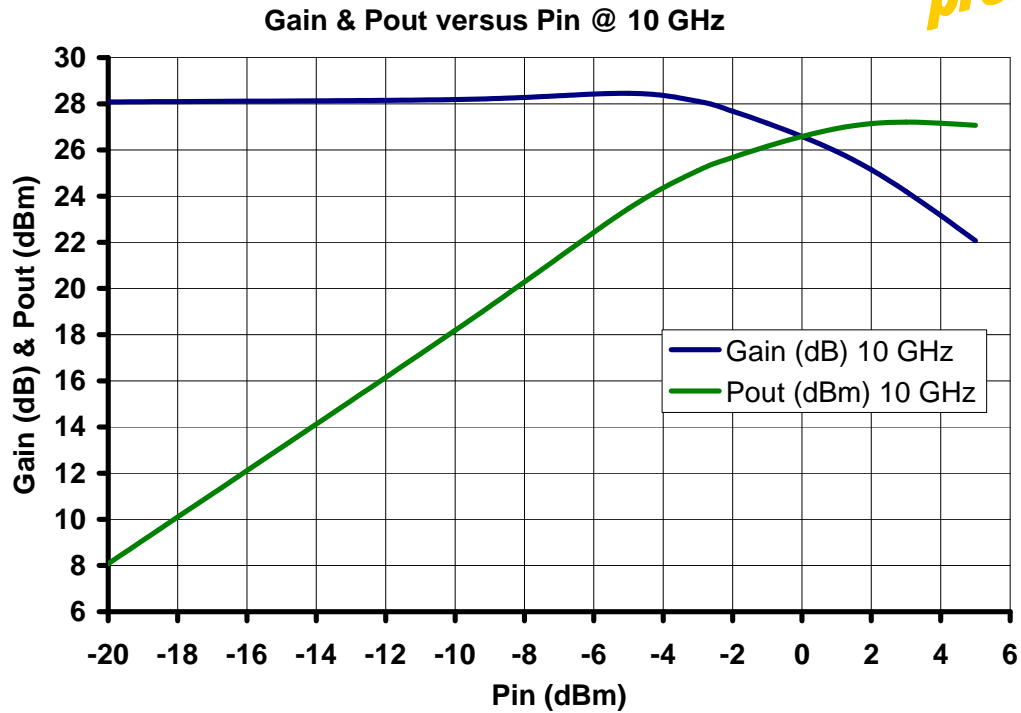
### Gain & Return Losses versus frequency



### Noise figure versus frequency (dB)



*preliminary*



## Typical Chip on wafer Sij parameters

Tamb.=+25°C, Vd1=+4.5V, Id=310mA

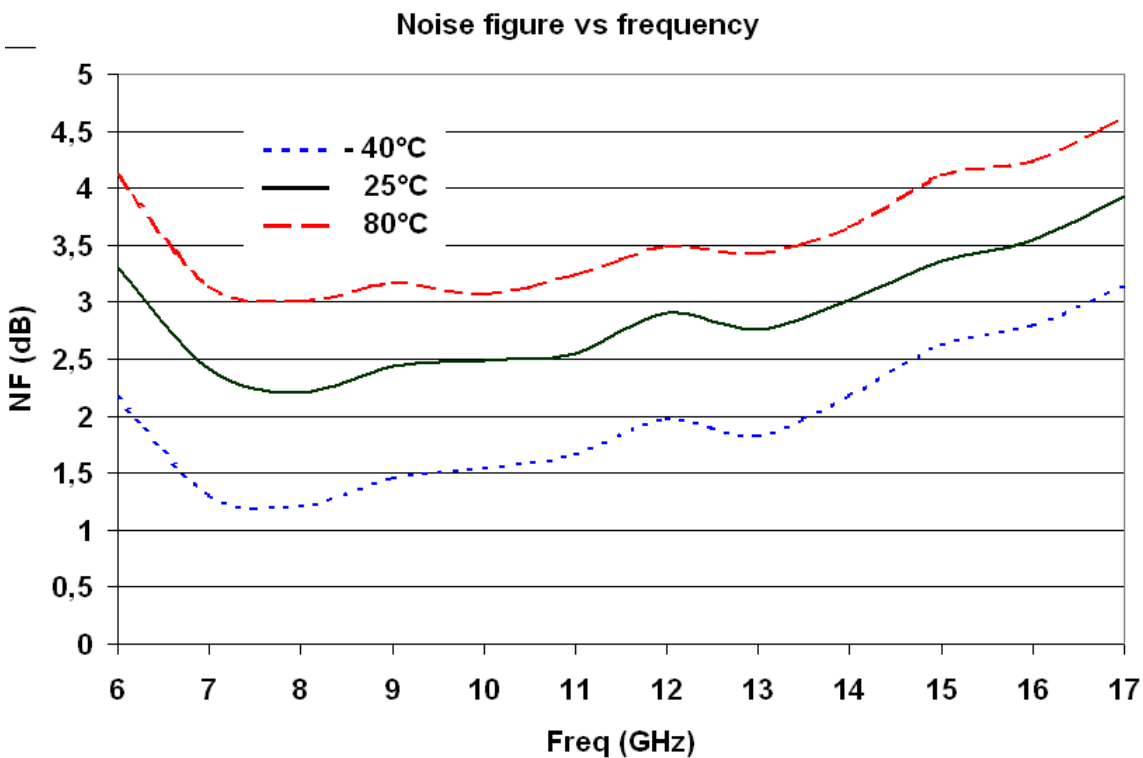
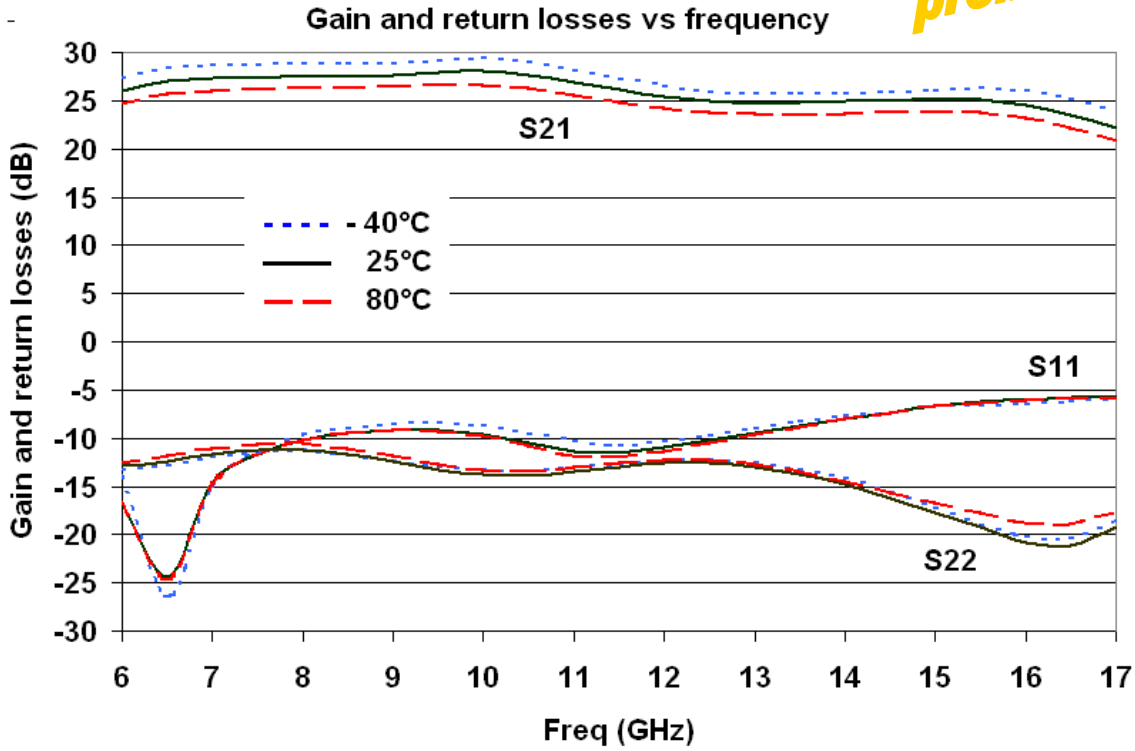
*preliminary*

Freq (GHz)	dB(S11)	P(S11) (°)	dB(S21)	P(S21) (°)	dB(S12)	P(S12) (°)	dB(S22)	P(S22) (°)
1,0	-1,4	118	-57,3	-37	-55,8	-122	-1,4	117
2,0	-1,1	65	-40,7	-48	-62,5	124	-1,3	57
3,0	-0,9	19	-11,2	-137	-81,2	167	-2,3	-0
4,0	-1,1	-25	3,2	111	-58,6	-18	-3,1	-46
5,0	-3,1	-81	18,3	4	-57,6	127	-9,9	-56
6,0	-14,3	-148	25,1	-108	-63,9	-162	-10,3	-77
7,0	-16,5	-11	27,1	154	-60,3	30	-11,4	-93
8,0	-11,3	-45	27,5	72	-62,5	108	-12,1	-117
9,0	-10,5	-72	27,3	2	-60,1	-155	-13,8	-140
10,0	-10,9	-92	26,7	-60	-53,2	-84	-17,4	-161
11,0	-9,5	-113	26,5	-116	-47,5	-113	-18,6	-174
12,0	-8,3	-151	26,7	-174	-47,0	-159	-17,1	145
13,0	-8,7	160	26,1	123	-43,6	170	-14,2	86
14,0	-10,5	116	24,5	71	-37,5	149	-11,8	25
15,0	-11,4	92	24,5	20	-41,4	103	-10,9	-15
16,0	-8,5	79	25,5	-44	-39,2	79	-14,1	-55
17,0	-5,0	37	22,9	-124	-46,3	75	-13,6	-4
18,0	-4,7	4	18,4	170	-75,8	-147	-8,9	-18
19,0	-4,9	-17	13,6	112	-55,6	74	-6,1	-32
20,0	-5,1	-35	8,3	58	-52,8	29	-4,1	-49
21,0	-4,9	-50	2,6	10	-48,1	168	-2,7	-67
22,0	-4,8	-65	-3,2	-32	-47,3	150	-2,1	-85
23,0	-4,8	-80	-9,3	-72	-44,7	117	-2,4	-100
24,0	-4,9	-92	-15,4	-104	-47,0	107	-2,0	-109
25,0	-4,9	-104	-21,5	-132	-55,8	55	-2,0	-121
26,0	-4,6	-120	-26,7	-164	-50,9	170	-2,3	-134

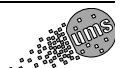
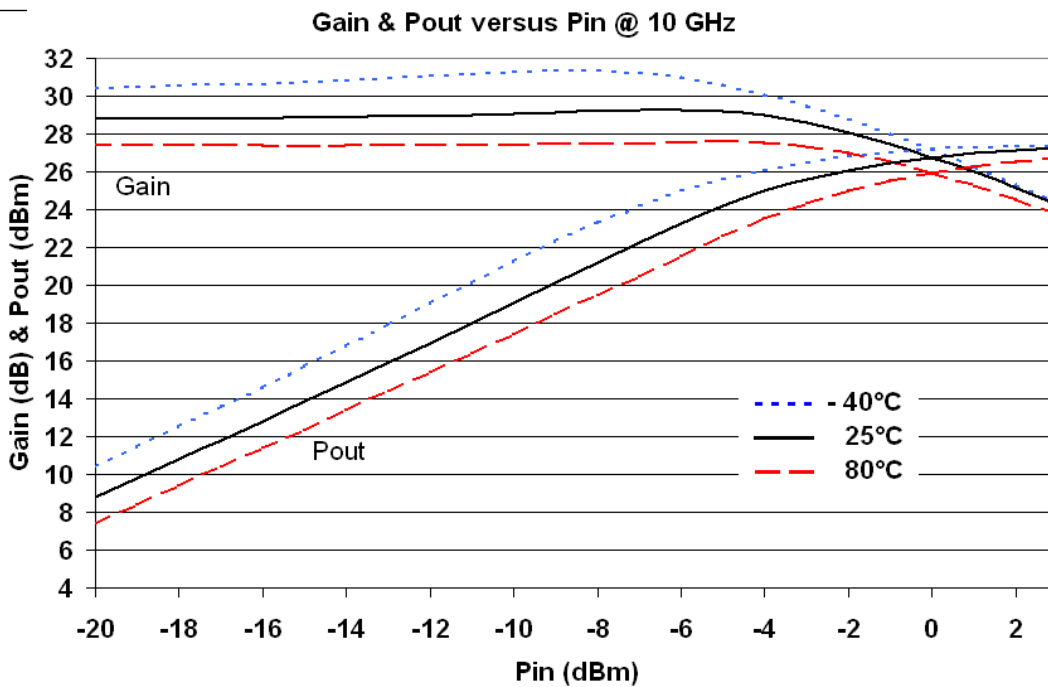
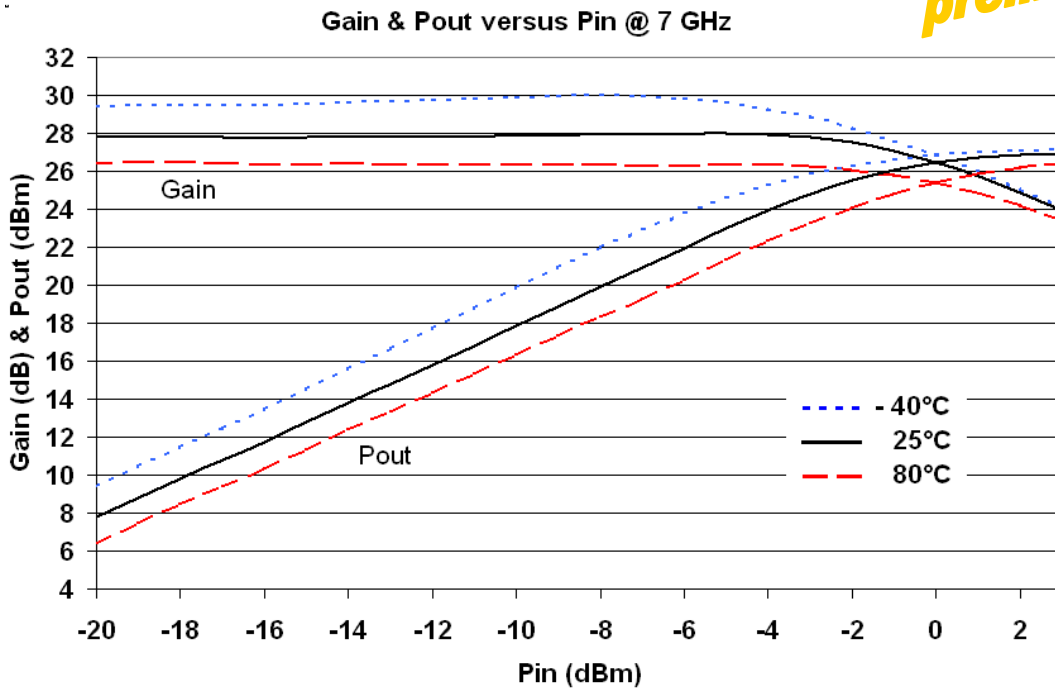
Typical Measured Performance in test fixture

Vd1=+4.5V, Id=310mA

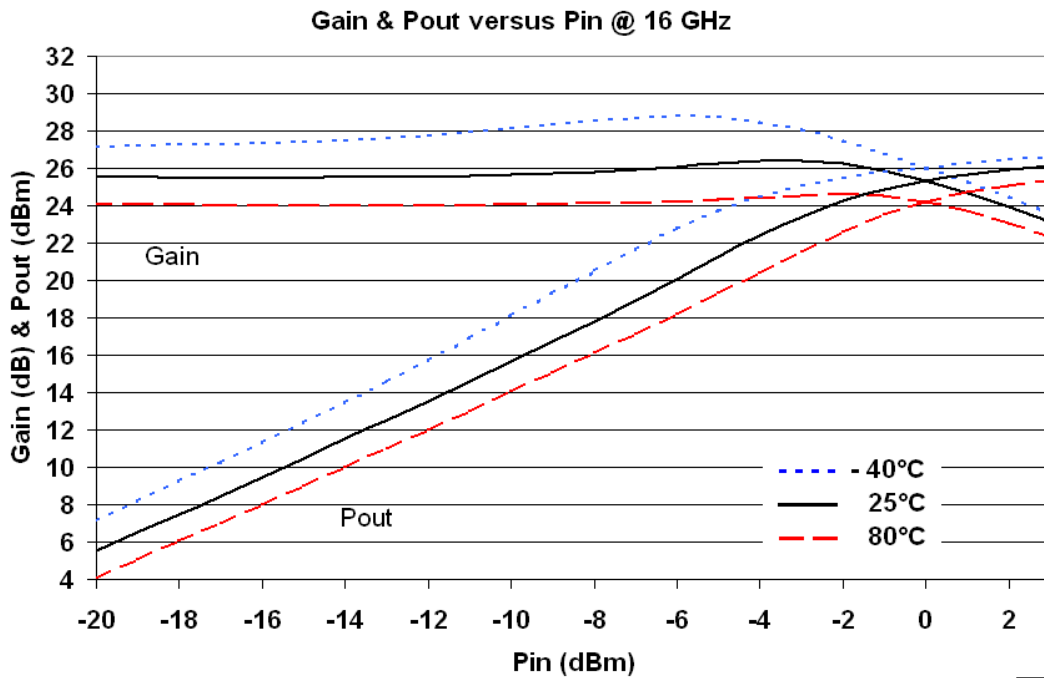
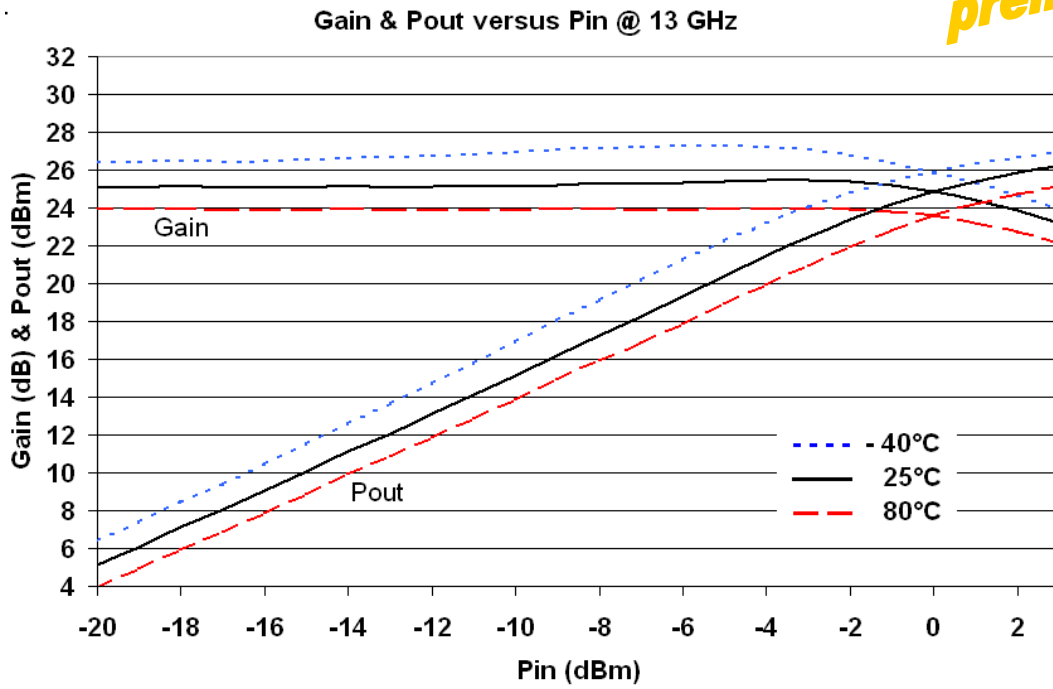
*preliminary*



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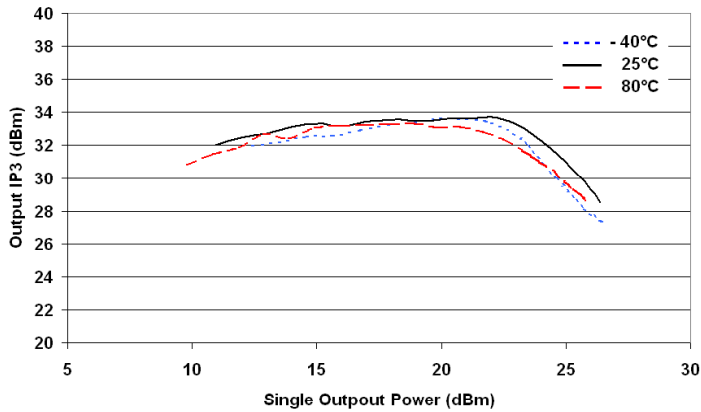
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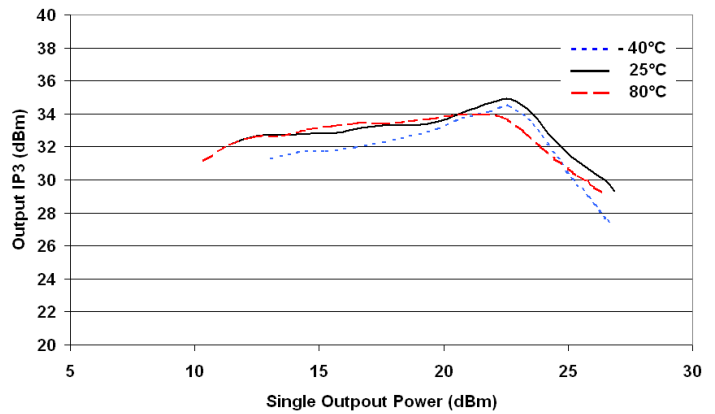


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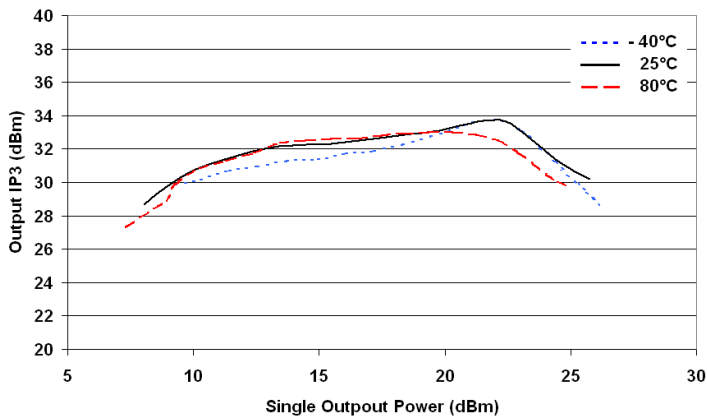
Output IP3 (dBm) vs output power @ 7 GHz



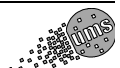
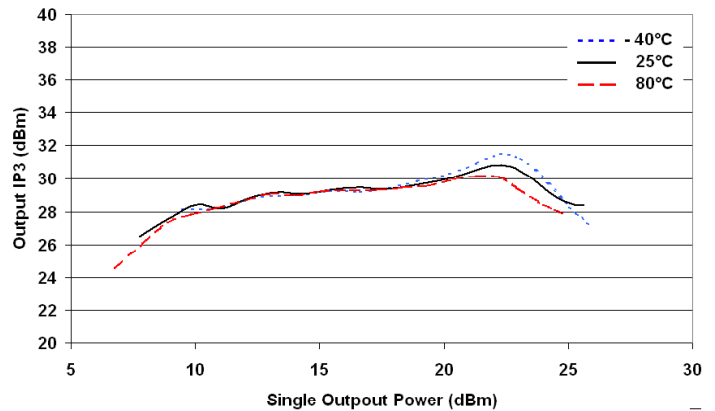
Output IP3 (dBm) vs output power @ 10 GHz



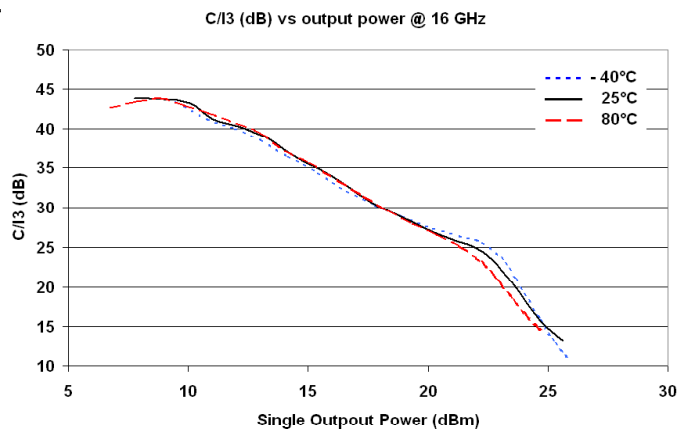
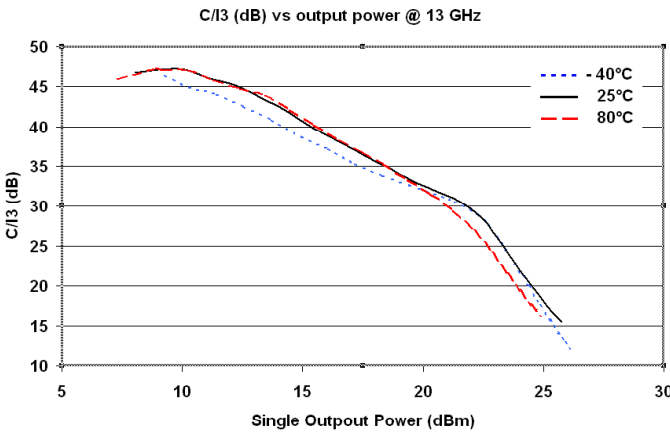
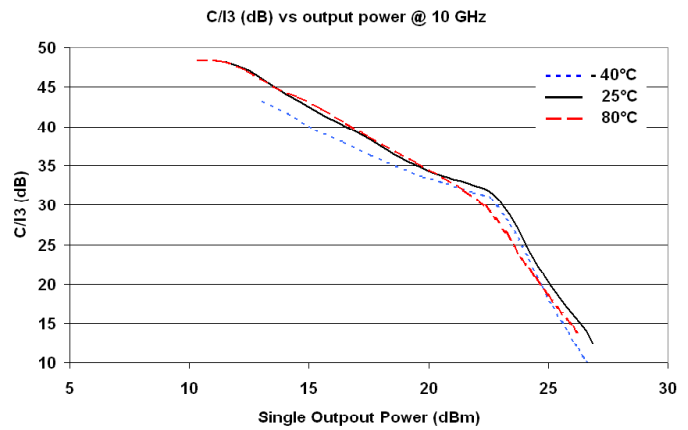
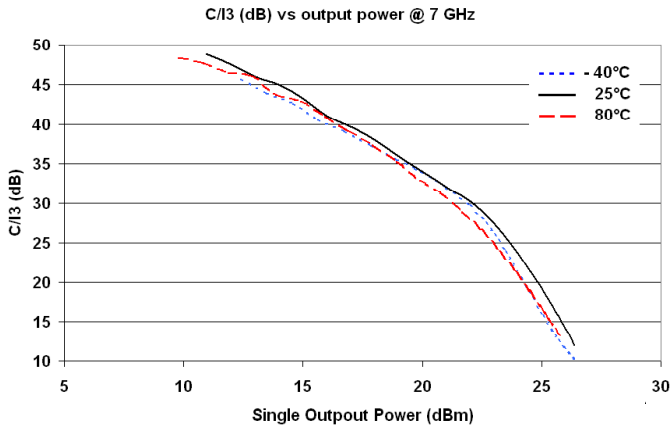
Output IP3 (dBm) vs output power @ 13 GHz



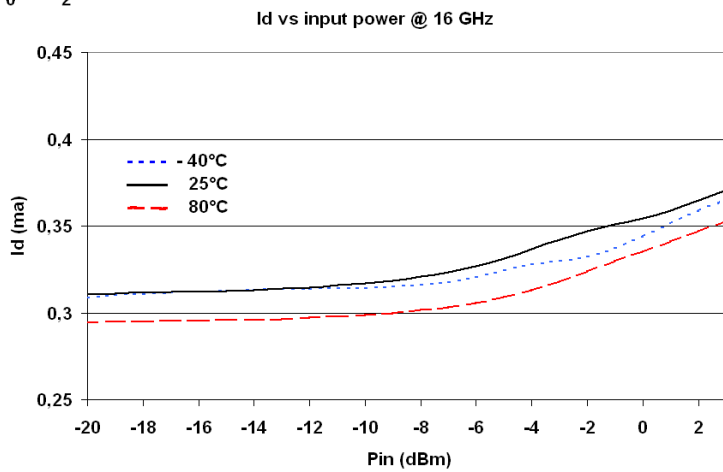
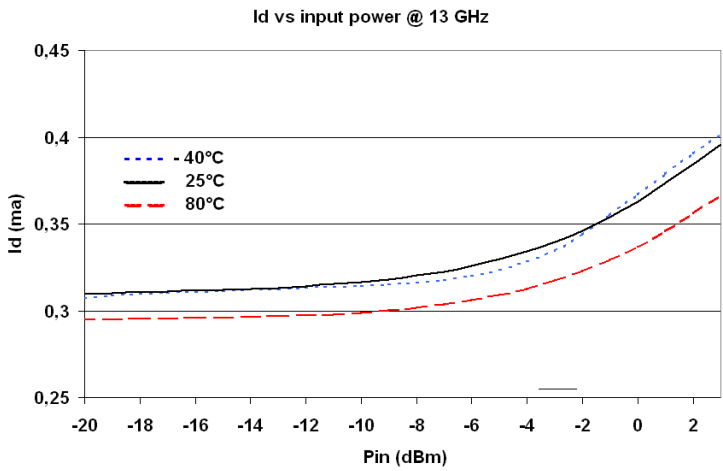
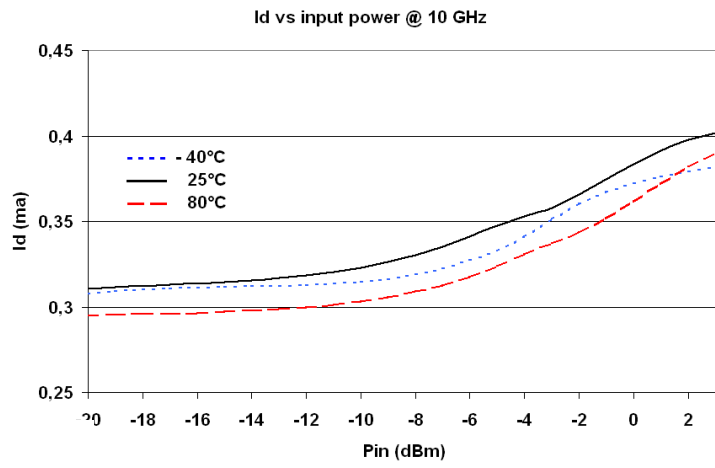
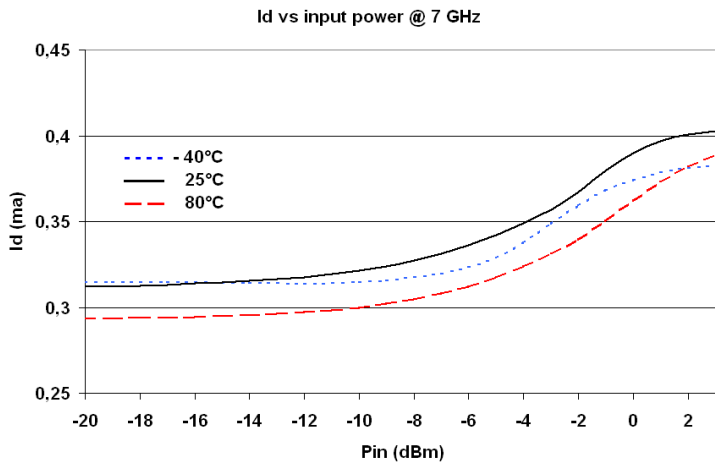
Output IP3 (dBm) vs output power @ 16 GHz



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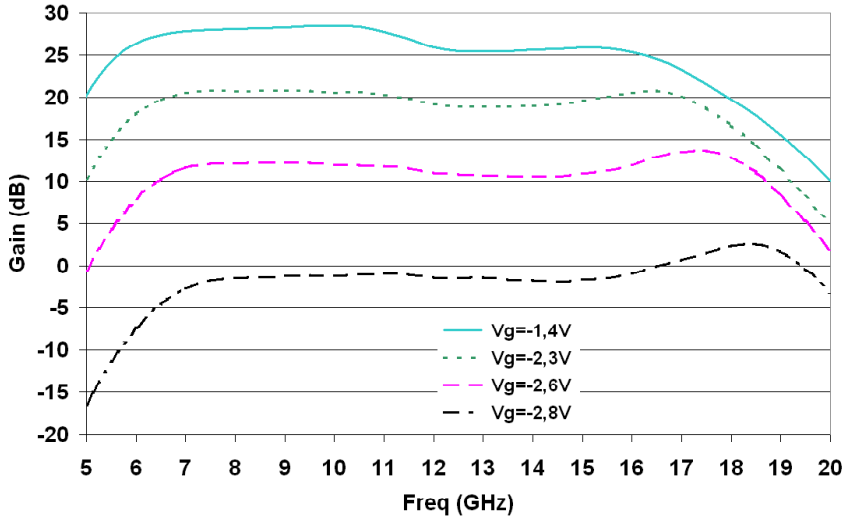


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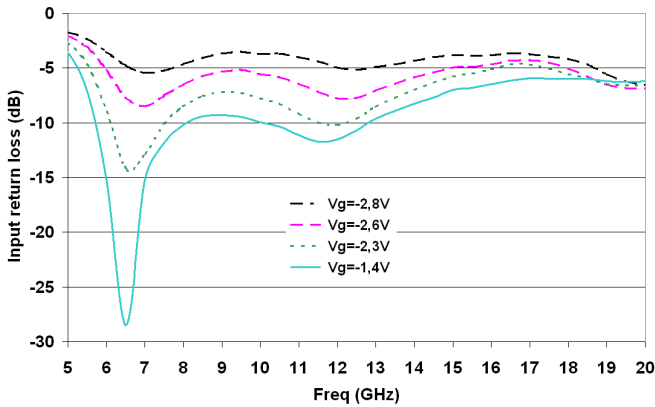
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Gain control with Vg vs frequency

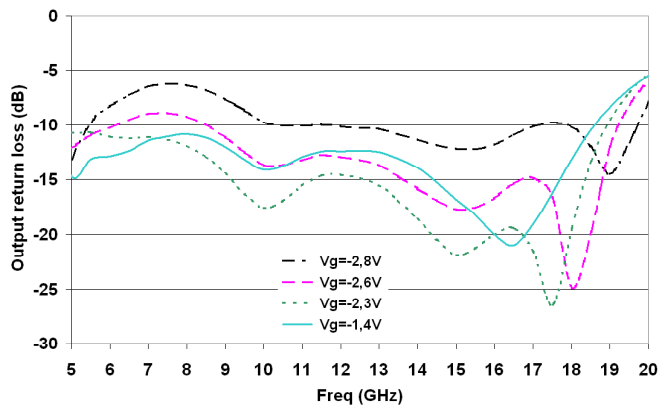


Associated return losses

Input return loss vs frequency

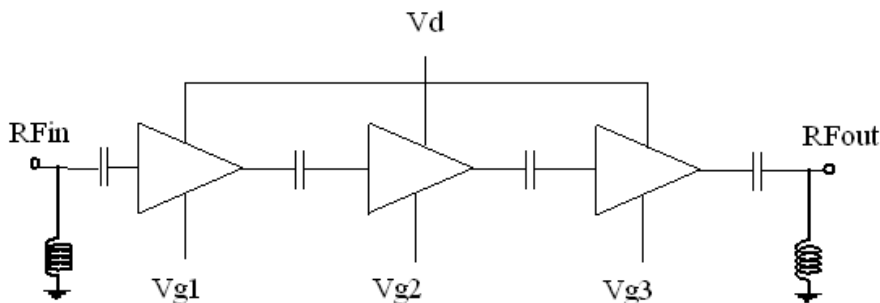


Output return loss vs frequency



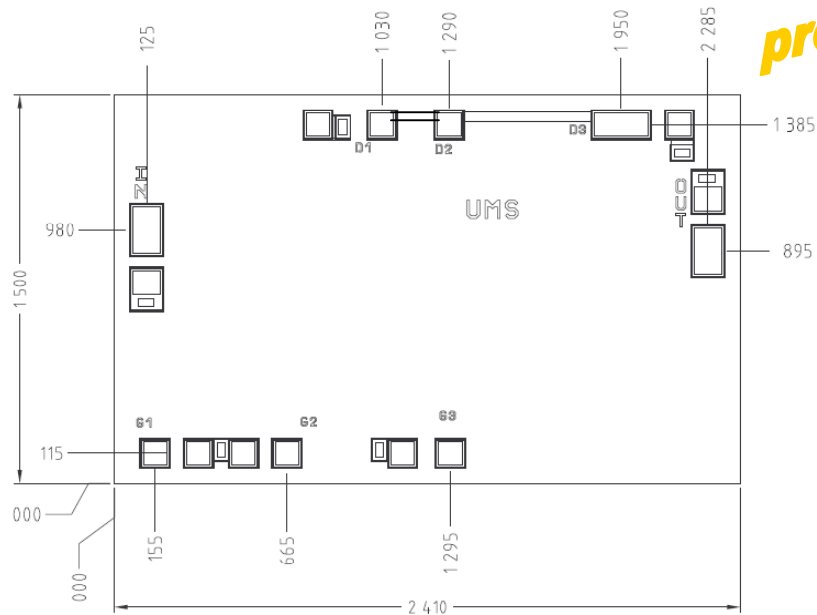
**Note**

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



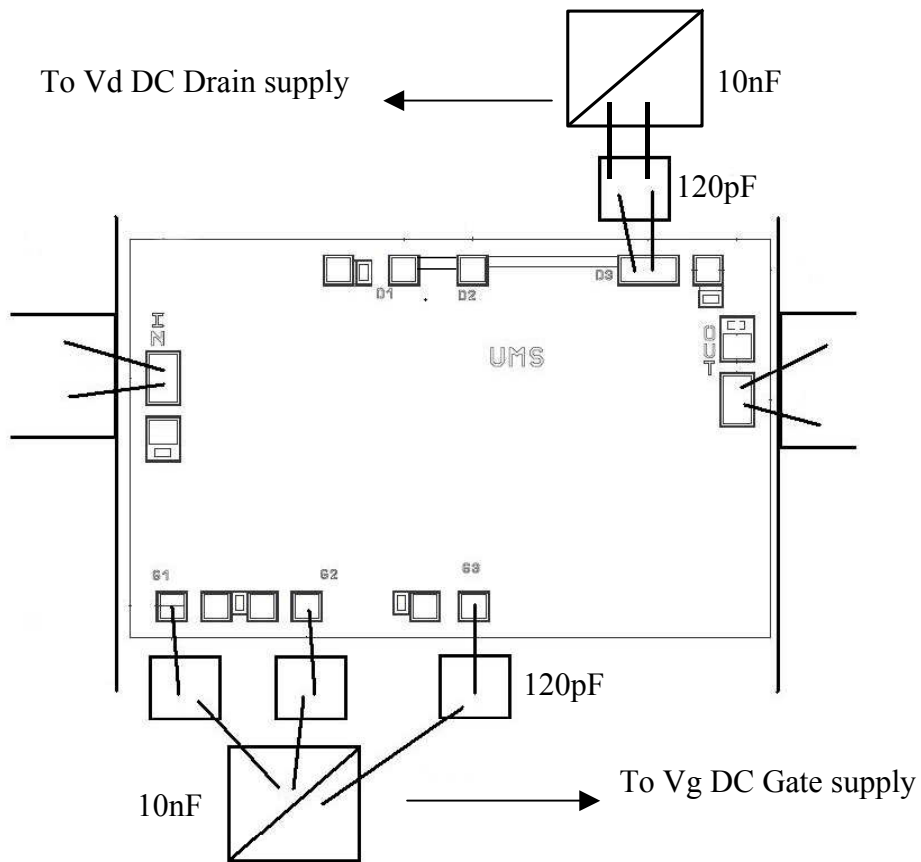
## Chip Assembly and Mechanical Data

*preliminary*



UNITS : μm  
Tol : ±35μm

- Note** : 25μm diameter gold wire is to be preferred.
- DC Pad size : 100/100μm .
- RF wire bondings should be as short as possible, lower than 0.35mm.
- Chip thickness : 100μm.



*preliminary*

## Ordering Information

Chip form: CHA5051-98F/00

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