HD74SSTV16842

11–bit to 22–bit Buffer with SSTL_2 Inputs and Outputs

REJ03D0829-0200
(Previous: ADE-205-602A)
Rev.2.00
Apr 07, 2006

Description

The HD74SSTV16842 is a 11–bit to 22–bit buffer designed for 2.3 V to 2.7 V Vcc operation and SSTL_2 data (A) inputs.

Features

- Supports SSTL_2 data inputs
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16842TEL	TSSOP-64 pin	PTSP0064KA-A (TTP-64DV)	T	EL (1,000 pcs / Reel)

Function Table

Input A	Output Y
L	L
H	H

H : High level

L : Low level

Pin Arrangement

(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	–0.5 to 3.6	V	
Input voltage [*1]	V_I	–0.5 to V_{DDQ}+0.5	V	
Output voltage [*1, 2]	V_O	–0.5 to V_{DDQ}+0.5	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}
V_{CC}, V_{DDQ} or GND current / pin	I_{CC}, I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air)	P_T	1	W	TSSOP
Storage temperature	Tstg	–65 to +150	°C	

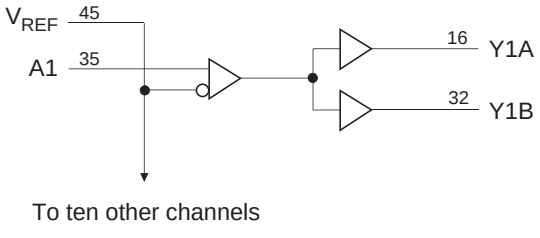
Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage	V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage	V_{TT}	V_{REF}–40 mV	V_{REF}	V_{REF}+40 mV	V	
Input voltage	V_I	0	—	V_{CC}	V	
AC high level input voltage	V_{IH}	V_{REF}+310 mV	—	—	V	A
AC low level input voltage	V_{IL}	—	—	V_{REF}–310 mV	V	A
DC high level input voltage	V_{IH}	V_{REF}+150 mV	—	—	V	A
DC low level input voltage	V_{IL}	—	—	V_{REF}–150 mV	V	A
High level output current	I_{OH}	—	—	–20	mA	
Low level output current	I_{OL}	—	—	20	mA	
Input transition rise or fall time	$\Delta t / \Delta v$	—	—	10	ns/V	
Operating temperature	Ta	0	—	70	°C	

Logic Diagram



Electrical Characteristics

Item		Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage		V_{IK}	2.3	—	—	–1.2	V	I_{IN} = –18 mA
Output voltage		V_{OH}	2.3 to 2.7	V_{CC}–0.2	—	—	V	I_{OH} = –100 µA
			2.3	1.95	—	V_{DDQ}		I_{OH} = –16 mA
		V_{OL}	2.3 to 2.7	—	—	0.2		I_{OL} = 100 µA
			2.3	0	—	0.35		I_{OL} = 16 mA
Input current	(All inputs)	I_{IN}	2.7	—	—	±5	µA	V_{IN} = 2.7 V or 0
Quiescent supply current		I_{CC} *2	2.7	—	—	45	mA	V_{IN} = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0
Dynamic operating per each data input		I_{CCD} *2	2.7	—	—	20	µA/ data input	V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, One data input switching at 50% duty cycle.
Output high *3		r_{OH}	2.3 to 2.7	7	—	20	Ω	I_{OH} = –20 mA
Output low *3		r_{OL}	2.3 to 2.7	7	—	20	Ω	I_{OL} = 20 mA
$\lvert r_{OH} - r_{OL} \rvert$ each separate bit *3		$r_{O(\Delta)}$	2.5	—	—	4	Ω	I_O = 20 mA, Ta = 25°C
Input capacitance	Data inputs	C_{IN}	2.5 *1	2.5	—	3.5	pF	V_I = V_{REF}±310 mV

Notes: 1. All typical values are at V_{CC} = 2.5 V, Ta = 25°C.
2. Total I_{CC} (max) = I_{CC} + {I_{CCD} (Data) × 11}
3. This is effective in the case that it did terminate by resistance.

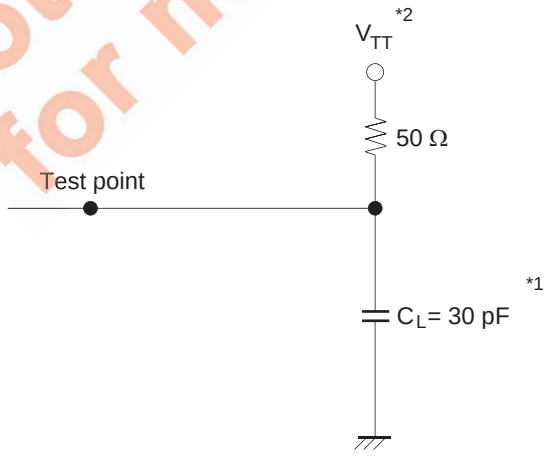
Switching Characteristics

V_{CC} = 1.8 ± 0.15 V

Item	Symbol	V_{CC} = 2.5 ± 0.2 V			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Propagation delay time *1	t_{PLH} t_{PHL}	1.6	—	2.8	ns	A	Y

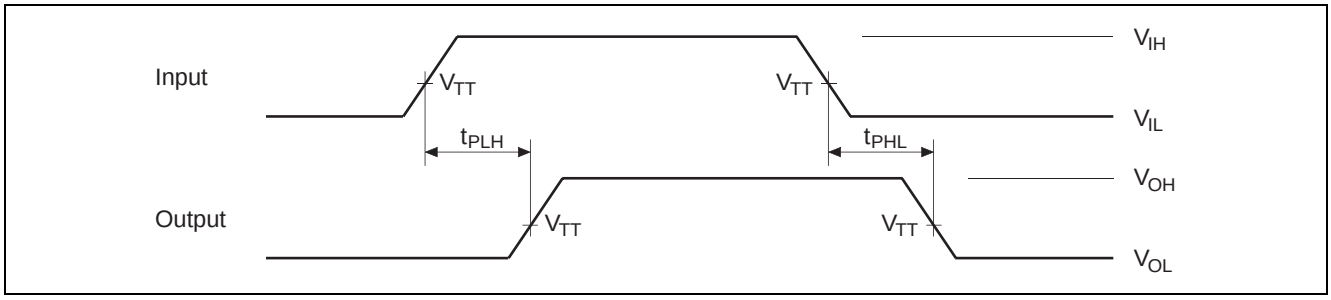
Note: 1. This timing relationship is specified into test load (see waveforms – 1) with all of the outputs switching.

Test Circuit



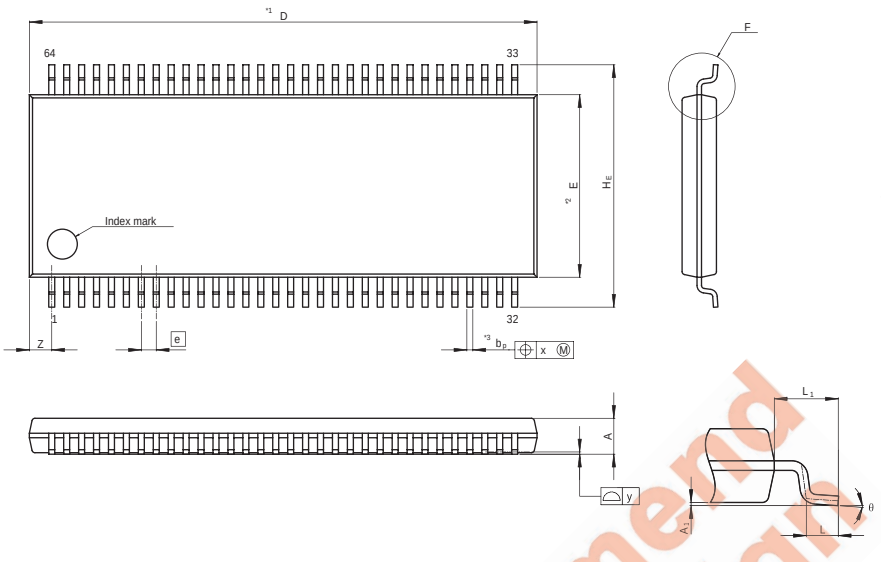
Notes: 1. C_L includes probe and jig capacitance.
2. V_{TT} = V_{REF} = V_{DDQ} × 0.5
3. Input waveform : PRR ≤ 10 MHz, Zo = 50 Ω,
Input slew rate = 1 V/ns ±20% (unless otherwise noted.)

Waveforms

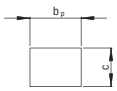


Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP64-6.1x17-0.50	PTSP0064KA-A	TTP-64DV	0.47g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	17.0	17.2
E	—	6.10	—
A_2	—	—	—
A_1	0.00	0.05	0.10
A	—	—	1.20
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	7.90	8.10	8.30
e	—	0.50	—
x	—	—	0.08
y	—	—	0.08
Z	—	—	0.90
L	0.4	0.5	0.6
L_1	—	1.0	—

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