



N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
N-Channel	20	0.052 at V _{GS} = 4.5 V	6.1 ^a	3.9 nc
		0.084 at V _{GS} = 2.5 V	4.8 ^a	
P-Channel	-20	0.090 at V _{GS} = -4.5 V	-4.8 ^a	3.8 nc
		0.160 at V _{GS} = -2.5 V	-3.6 ^a	

FEATURES

- TrenchFET® Power MOSFETs

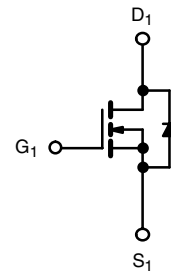
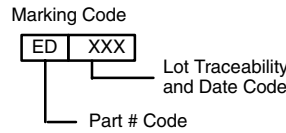
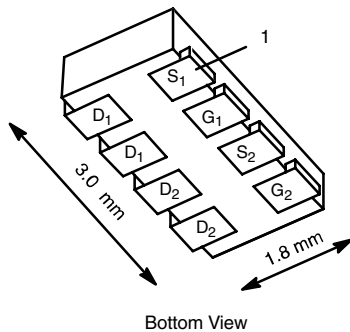
APPLICATIONS

- Complementary MOSFET for Portable Devices
 - Ideal for Buck–Boost Circuits

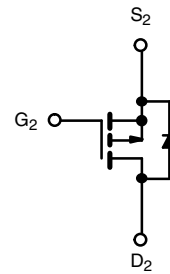


RoHS COMPLIANT

1206-8 ChipFET®



N-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si5509DC-T1-E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6.1 ^a	-4.8 ^a
		T _C = 70 °C	4.9 ^a	-3.8 ^a
		T _A = 25 °C	5.0 ^{b, c}	-3.9 ^{b, c}
		T _A = 70 °C	3.9 ^{b, c}	-3.1 ^{b, c}
Pulsed Drain Current	I _{DM}	10	-15	A
Source-Drain Current Diode Current	I _S	T _C = 25 °C	3.7	
		T _A = 25 °C	1.7 ^{b, c}	-1.7 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	4.5	4.5
		T _C = 70 °C	2.88	2.88
		T _A = 25 °C	2.1 ^{b, c}	2.1 ^{b, c}
		T _A = 70 °C	1.33 ^{b, c}	1.33 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ	Max	Typ	Max		
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 sec	R _{thJA}	50	60	50	60	°C/W
Maximum Junction-to-Foot (Drain)	Steady-State	R _{thJF}	30	40	30	40	

Notes

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 Board.
- t = 5 sec
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W for both channels.



SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Condition		Min	Typ ^a	Max	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	20			mV/°C	
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-20				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		18.4			
		I _D = -250 μA	P-Ch		-15.1			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		-3.4			
		I _D = -250 μA	P-Ch		2.2			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.7		2	V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.7		-2		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch			100	nA	
			P-Ch			-100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA	
			P-Ch			-1		
			V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch				10
				P-Ch				-10
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ 5 V, V _{GS} = 4.5 V	N-Ch	10			A	
			P-Ch	-15				
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.0 A	N-Ch		0.043	0.052	Ω	
			P-Ch		0.074	0.090		
			V _{GS} = 2.5 V, I _D = 3.9 A	N-Ch		0.068		0.084
				P-Ch		0.128		0.160
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 5.0 A	N-Ch		10.4		S	
			P-Ch		8.2			
Dynamic^a								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		455		pF	
			P-Ch		300			
Output Capacitance	C _{oss}		N-Ch		85			
			P-Ch		95			
Reverse Transfer Capacitance	C _{rss}		N-Ch		50			
			P-Ch		65			
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 5 V, I _D = 4.0 A V _{DS} = -10 V, V _{GS} = -5 V, I _D = -3.9 A	N-Ch		4.4	6.6	nC	
			P-Ch		4.1	6.2		
			N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.0 A	N-Ch		3.8		5.7
				P-Ch		3.9		5.9
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -3.9 A	N-Ch		0.9			
			P-Ch		0.7			
Gate-Drain Charge	Q _{gd}	N-Ch		0.95				
		P-Ch		1.25				
Gate Resistance	R _g	f = 1 MHz	N-Ch		1.9		Ω	
			P-Ch		8			



SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Dynamic^a							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 2.5 Ω I _D ≅ 4.0 A, V _{GEN} = 4.5 V, R _g = 1 Ω P-Channel V _{DD} = -10 V, R _L = 3.2 Ω I _D ≅ -3.14 A, V _{GEN} = -4.5 V, R _g = 1 Ω	N-Ch	6	9	ns	
			P-Ch	8	12		
Rise Time	t _r		N-Ch	95	143		
			P-Ch	75	113		
Turn-Off Delay Time	t _{d(off)}		N-Ch	12	18		
			P-Ch	25	38		
Fall Time	t _f		N-Ch	6	9		
			P-Ch	60	90		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch		3.75	A	
			P-Ch		-3.75		
Pulse Diode Forward Current ^a	I _{SM}		N-Ch		10	A	
			P-Ch		-15		
Body Diode Voltage	V _{SD}	I _S = 2.4 A, V _{GS} = 0 V	N-Ch	0.8	1.2	V	
		I _S = -1.5 A, V _{GS} = 0 V	P-Ch	-0.8	-1.2		
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 2.4 A, di/dt = 100 A/μs, T _J = 25 °C P-Channel I _F = -1.5 A, di/dt = -100 A/μs, T _J = 25 °C	N-Ch	12	18	ns	
			P-Ch	18	27		
Body Diode Reverse Recovery Charge	Q _{rr}		N-Ch	5	8	nC	
			P-Ch	8	12		
Reverse Recovery Fall Time	t _a	N-Ch	7.5		ns		
		P-Ch	14				
Reverse Recovery Rise Time	t _b	N-Ch	4.5				
		P-Ch	4				

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

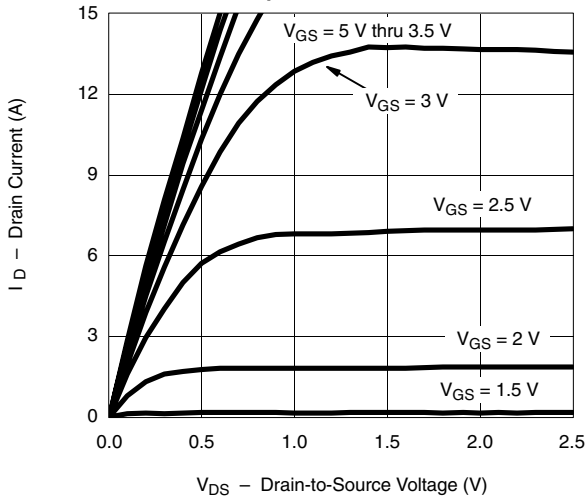
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



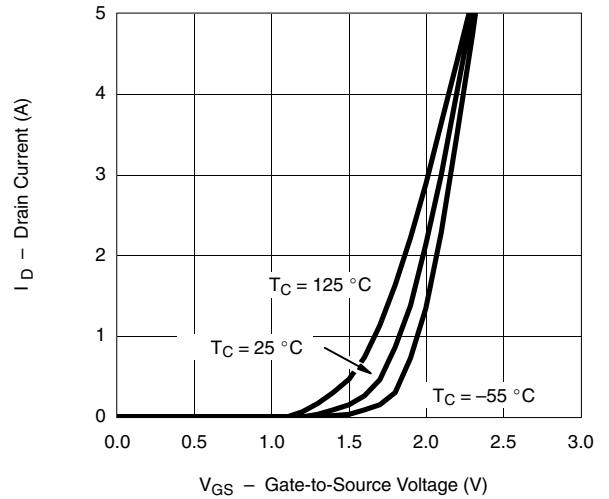
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

N-CHANNEL

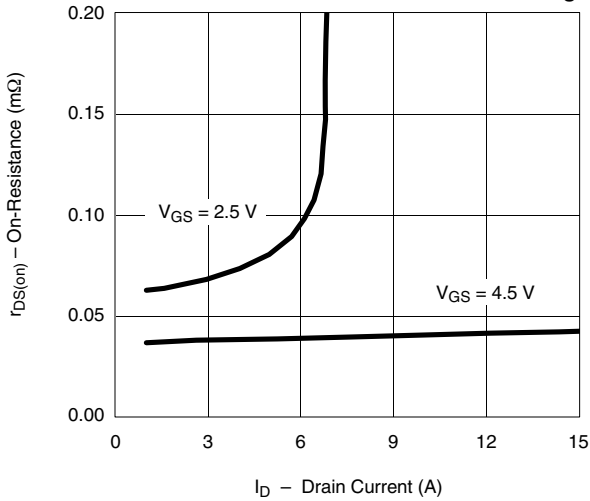
Output Characteristics



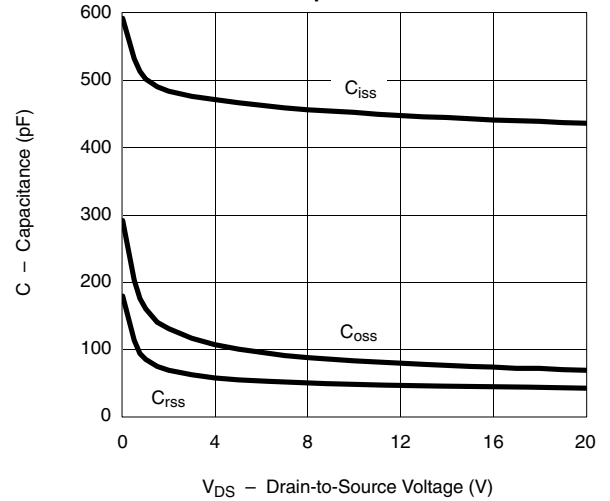
Transfer Characteristics



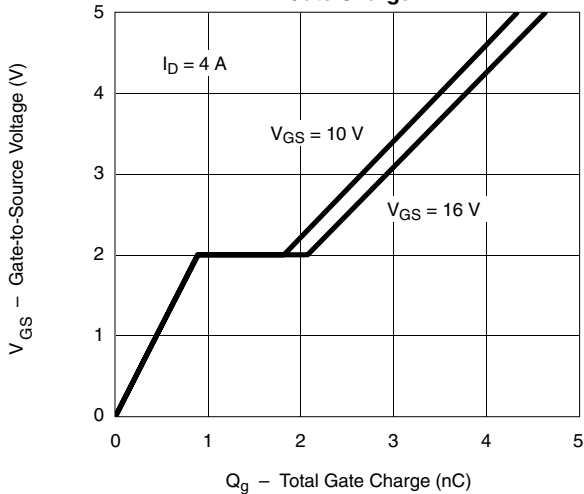
On-Resistance vs. Drain Current and Gate Voltage



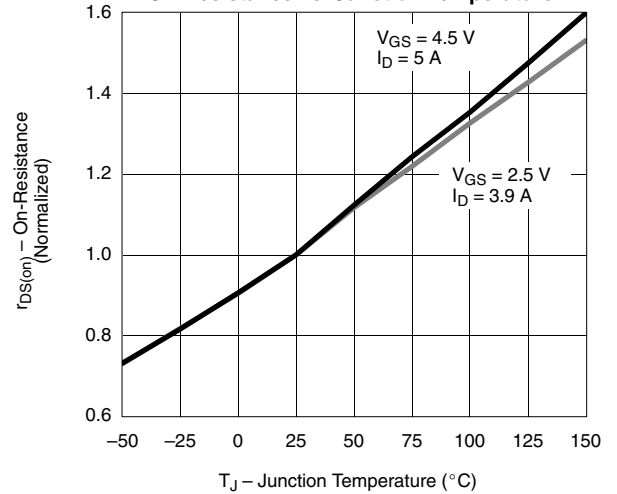
Capacitance



Gate Charge



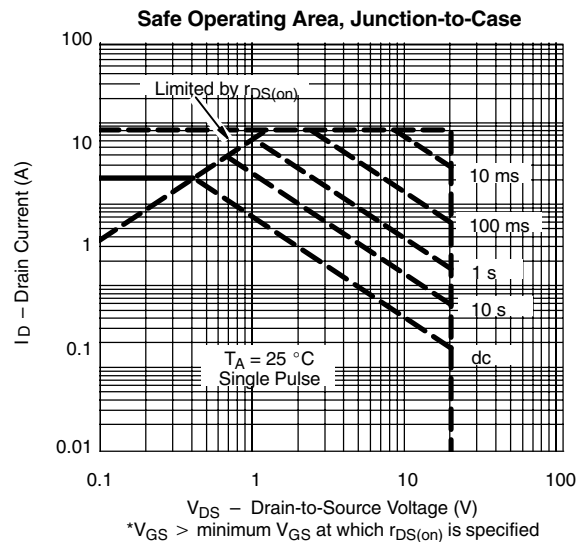
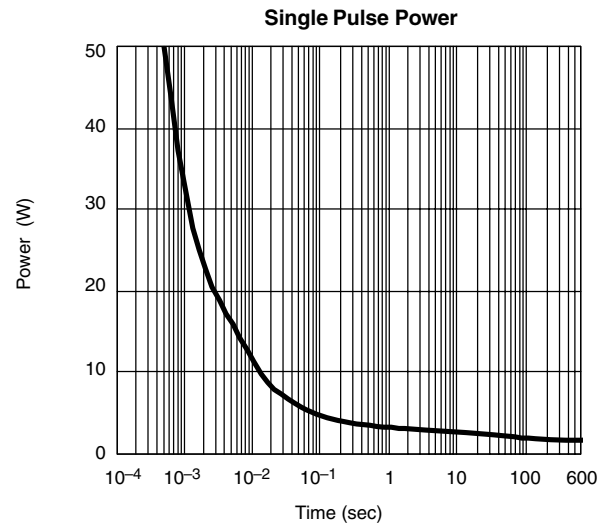
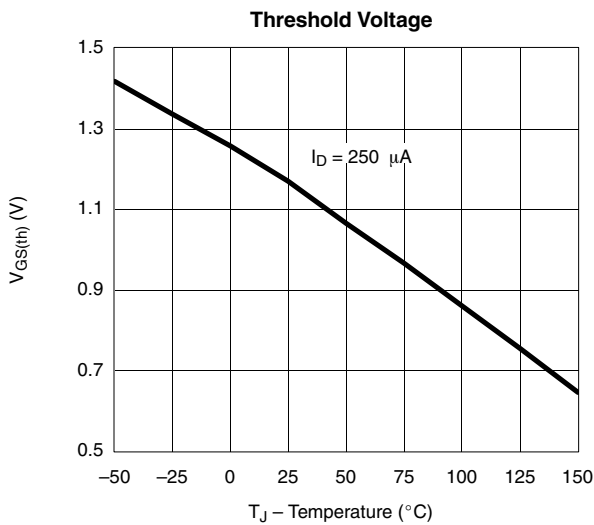
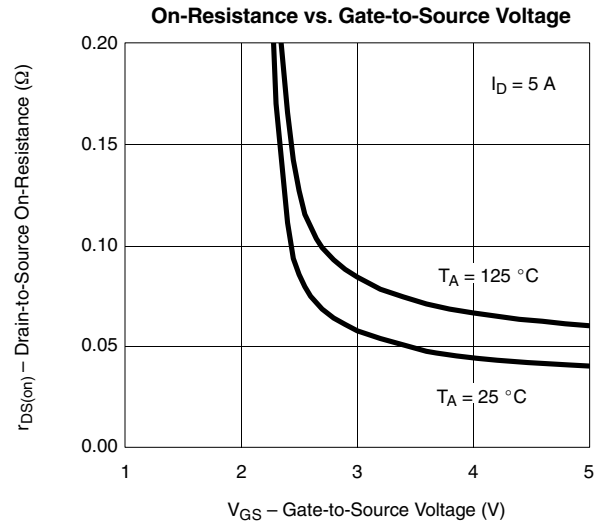
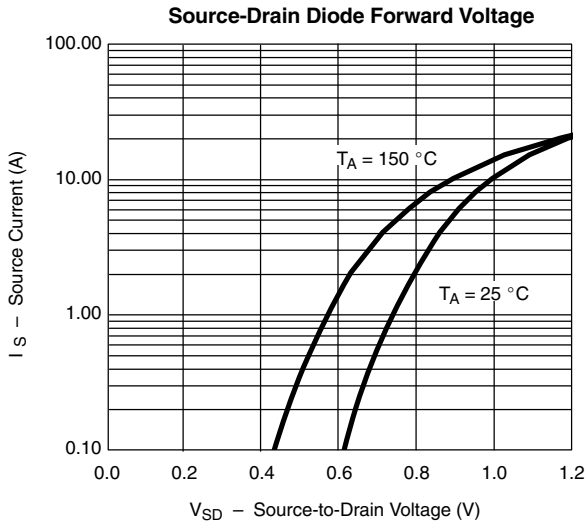
On-Resistance vs. Junction Temperature





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

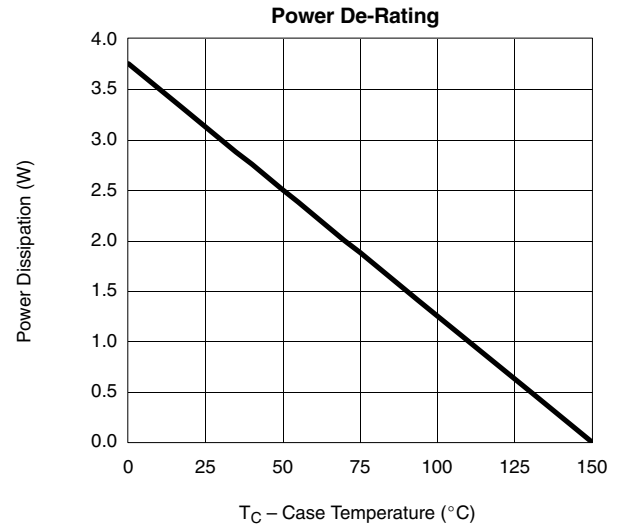
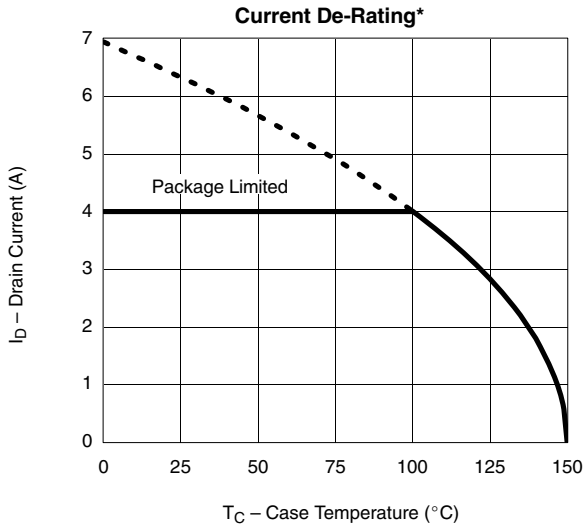
N-CHANNEL





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

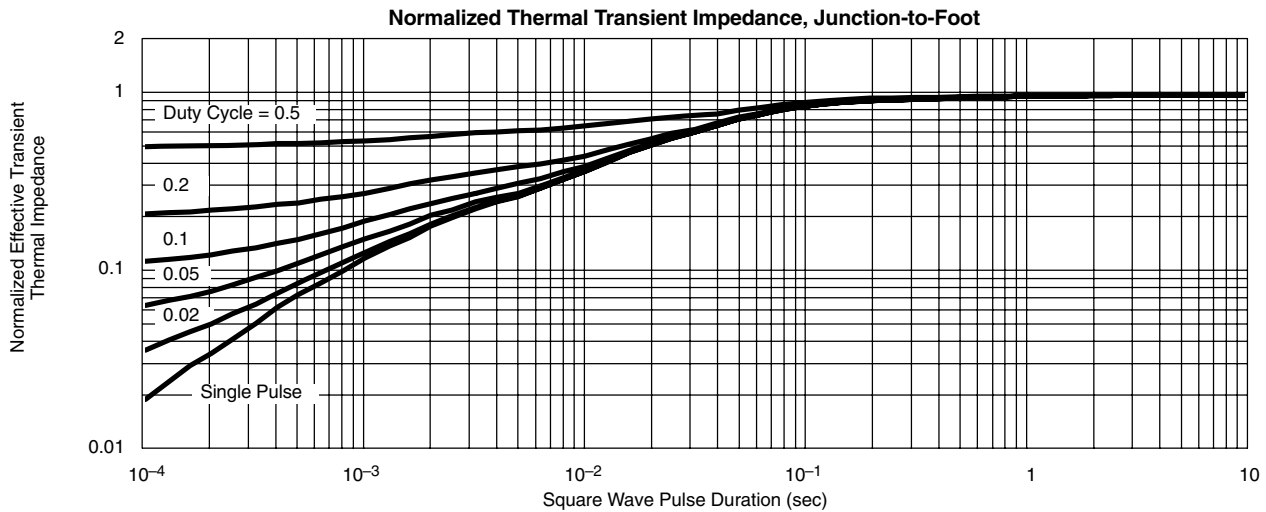
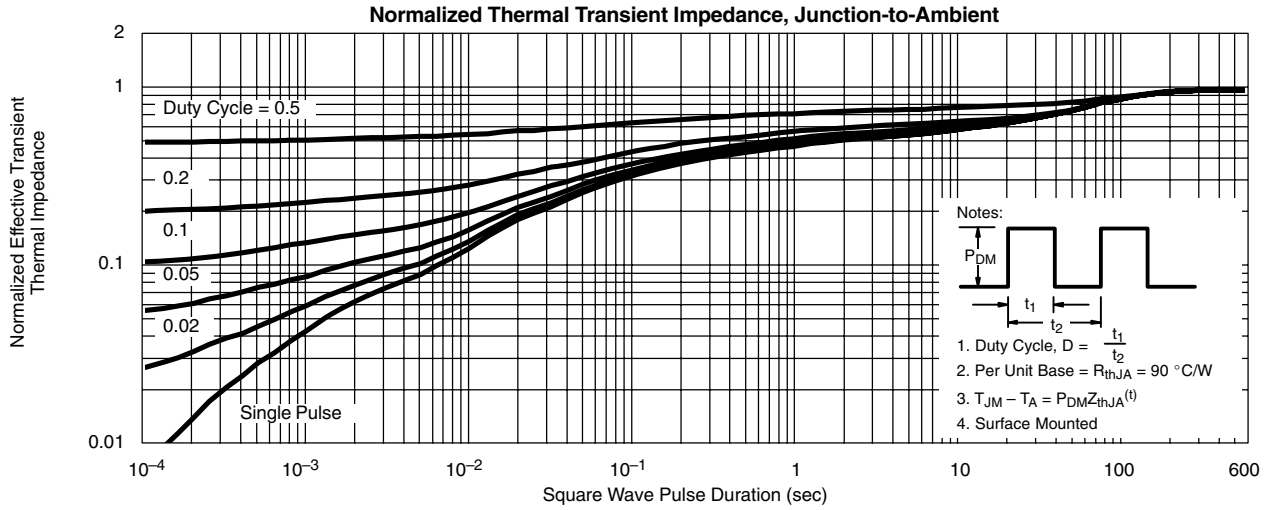
N-CHANNEL



*The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



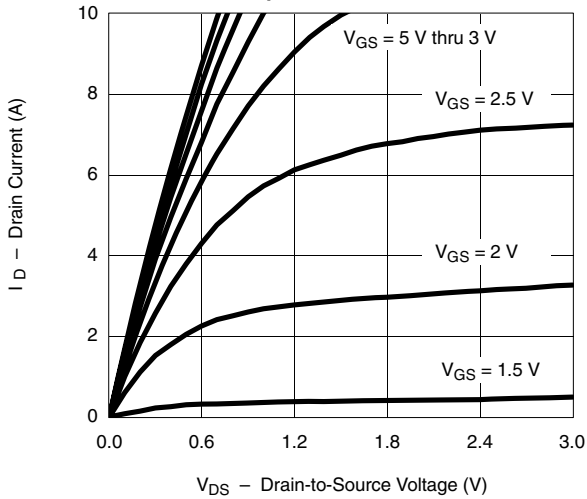
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) N-CHANNEL



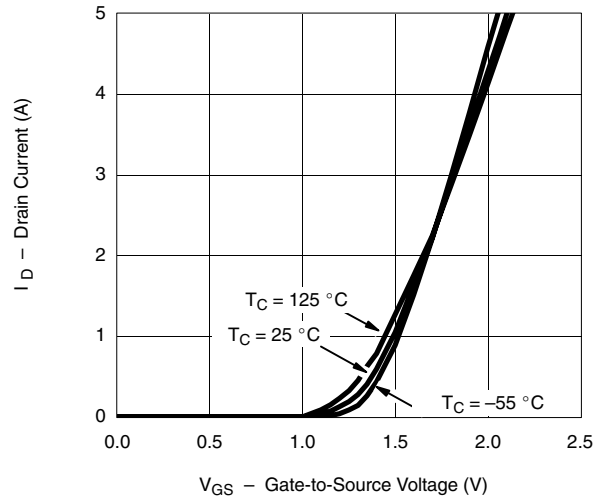
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL

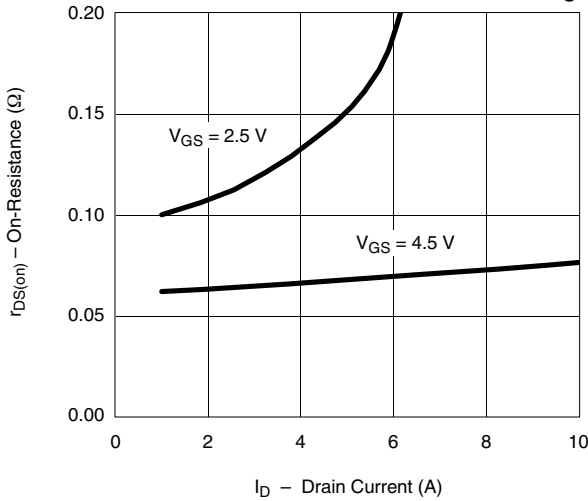
Output Characteristics



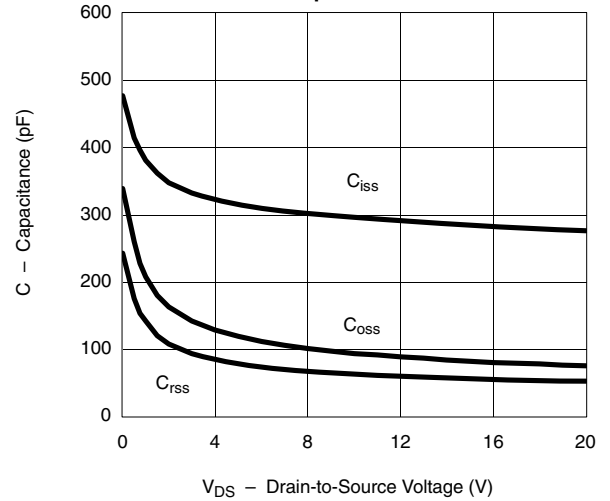
Transfer Characteristics



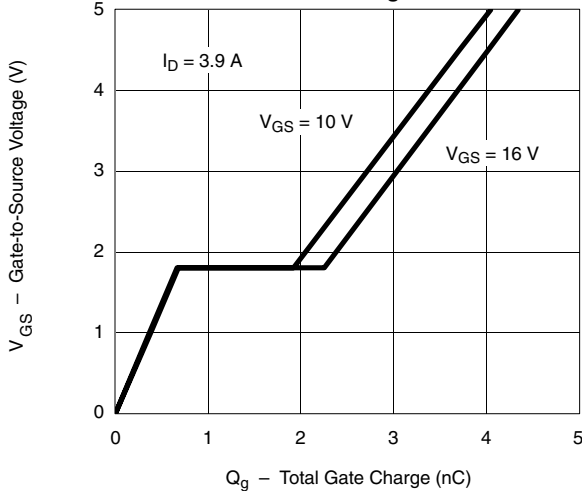
On-Resistance vs. Drain Current and Gate Voltage



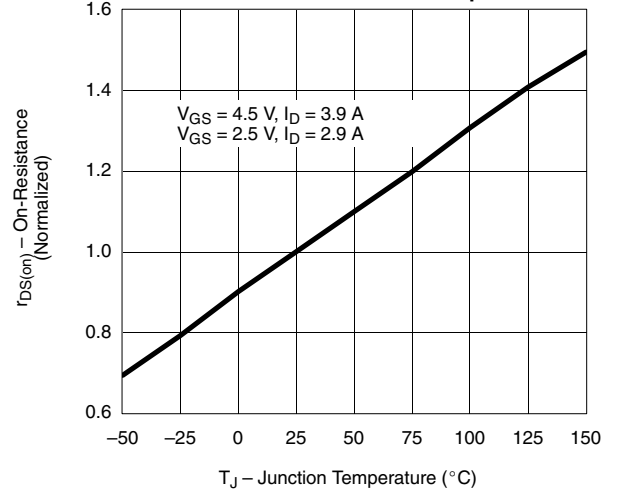
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

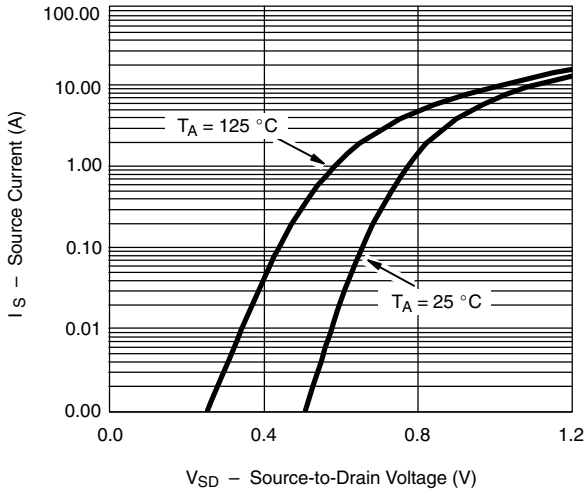




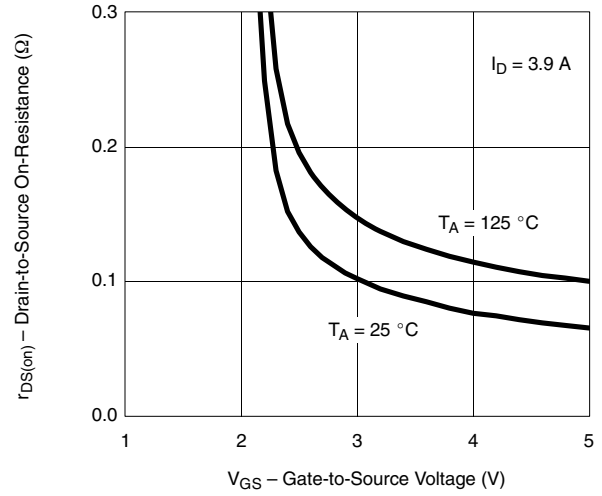
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL

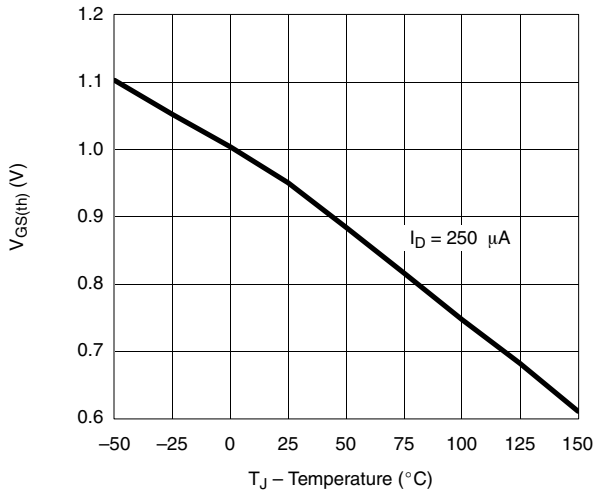
Source-Drain Diode Forward Voltage



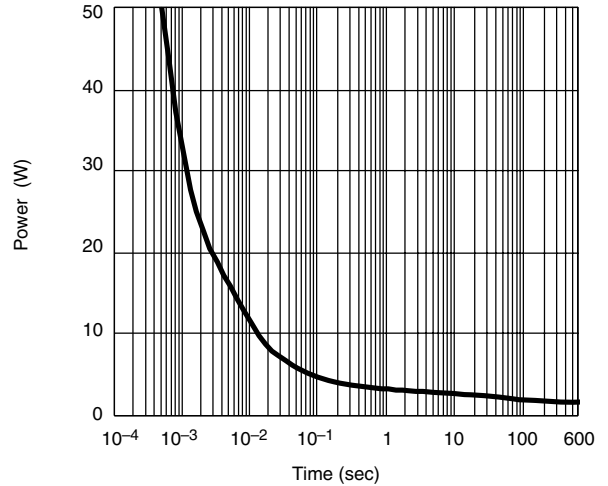
On-Resistance vs. Gate-to-Source Voltage



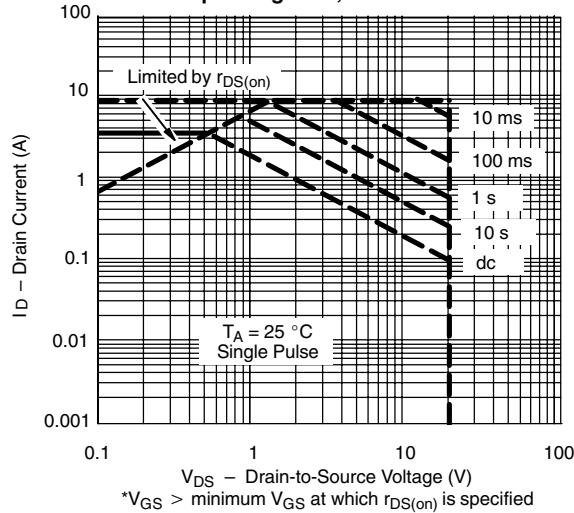
Threshold Voltage



Single Pulse Power



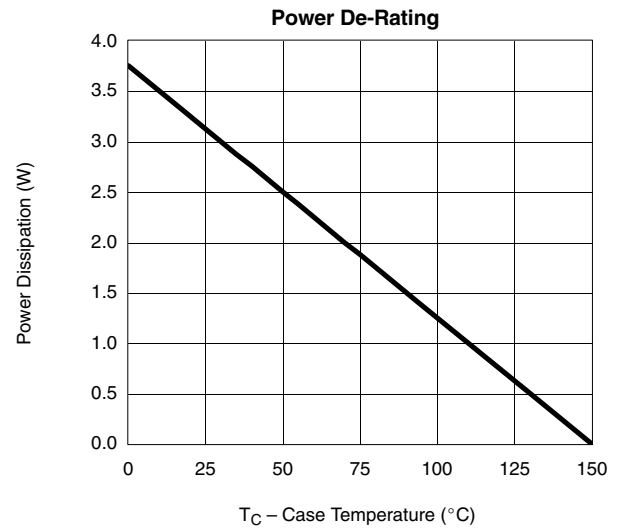
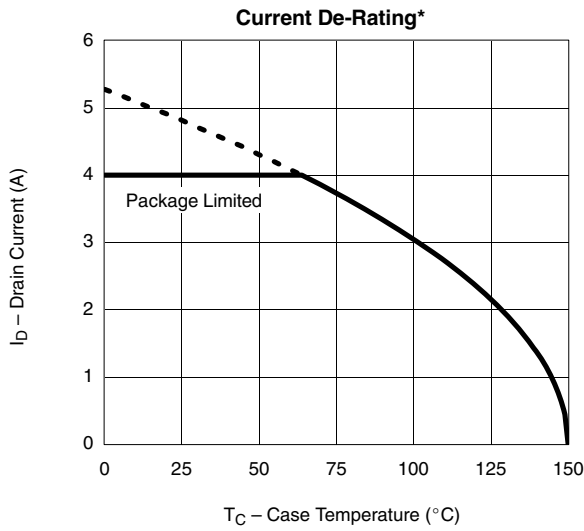
Safe Operating Area, Junction-to-Case





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL

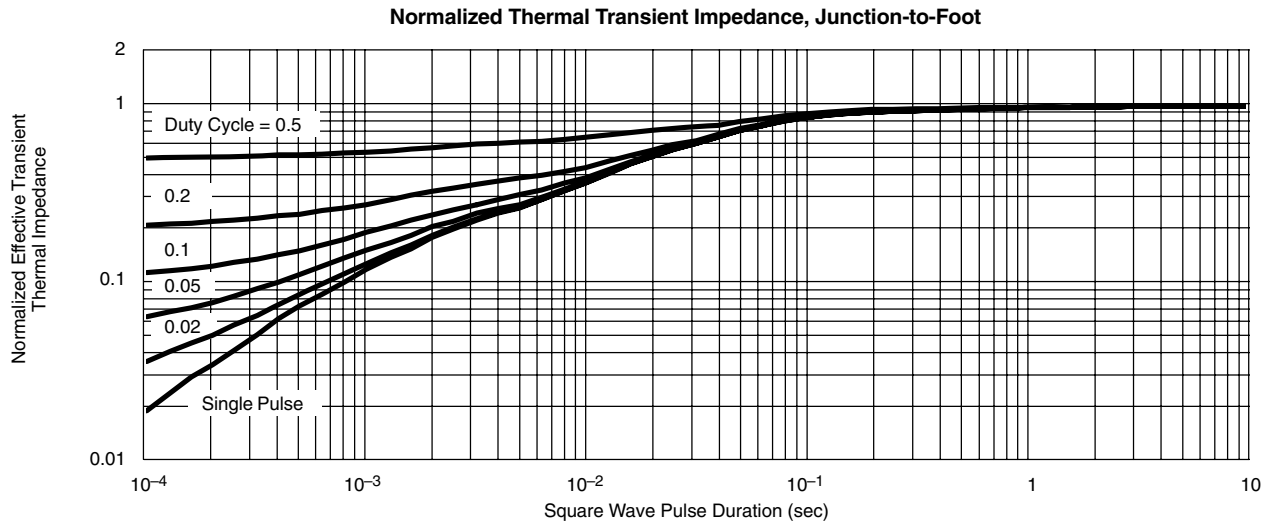
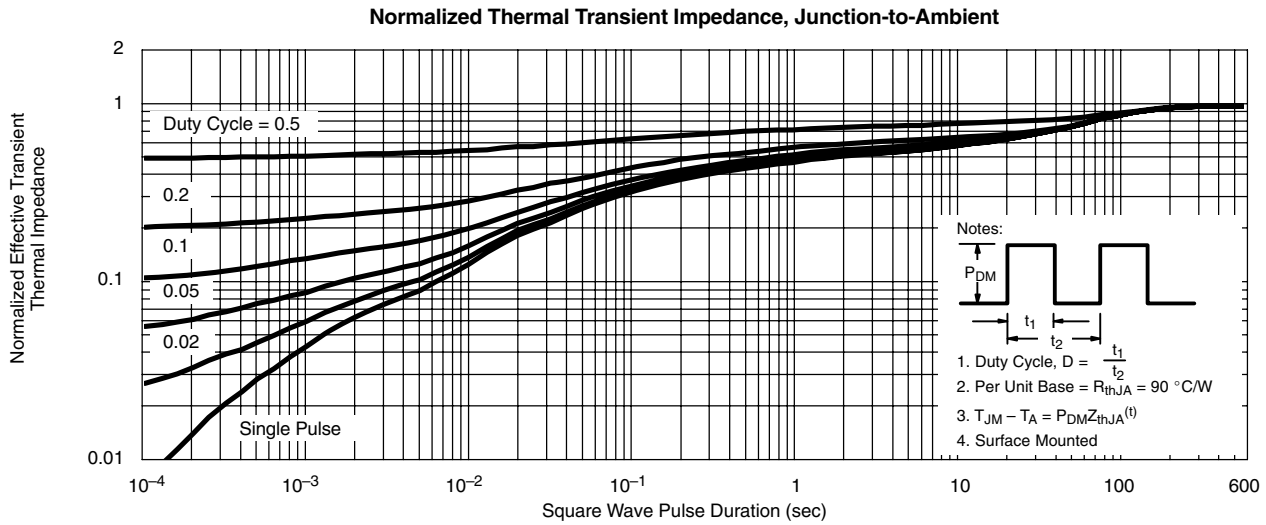


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TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL



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