



SANYO Semiconductors

DATA SHEET

LV5044V

Bi-CMOS IC
2ch step-down circuit
DC-DC Converter Controller

Overview

The LV5044V is a high efficiency, 2-channel, step-down, DC-DC converter controller IC adopting a synchronous rectifying system. Incorporating numerous functions on a single chip with easy external setting, it can be used for a wide variety of applications. The device is optimal for use in multi-output power supply systems which are used in LCD-TVs, DVD recorders, game machines, high-end office products, etc.

Features

- Provides dual step-down DC-DC converter controller circuits integrated on the same chip.
- Provides an input UVLO circuit, an overcurrent detection function, an overtemperature detection function, soft start/soft stop functions, and a startup delay circuit.
- Output voltage monitoring functions (power good as well as OVP and UVP with timer latch functions)
- 180° interleaved operation between phase 1 and phase 2 (supports multiphase drive in 2-phase parallel operation mode).
- Supports synchronous operation between different devices (supports master/slave operation when multiple devices are used).

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|-------------------|------------|-------------|------------------|
| Supply voltage | V_{IN} | | 18 | V |
| Peak output current | I_{OUT} | | ± 1.0 | A |
| Allowable power dissipation | $P_d \text{ max}$ | *1 | 1 | W |
| Operating temperature | T_{opr} | | -20 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

*1 Board size: $114.3 \times 76.1 \times 1.6 \text{ mm}^3$, glass epoxy board.

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LV5044V

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| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------|--|------------|-----------|------|
| Allowable pin voltage *2 | | | | |
| 1 | HDRV1,2 CBOOT1,2 | | 18 | V |
| 2 | HDRV1,2 ,CBOOT1,2 to SW | | 6.5 | V |
| 3 | V _{IN} , ILIM1,2 RSNS1,2, SW1,2 PGOOD1,2 | | 18 | V |
| 4 | VLIN5 V _{DD} , LDRV1,2 | | 6.5 | V |
| 5 | COMP1,2, FB1,2 SS1,2, UV_DELAY TD1,2, CT CLKO | | VLIN5+0.3 | V |

*2 Allowable pin voltages are referenced to the SGND and PGND pins, excluding No.2. No.2 Voltages are referenced to the SW pin.

Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------|-----------------|---------------------------------|------------|------|
| Supply voltage | V _{IN} | V _{IN} and VLIN open. | 7.5 to 16 | V |
| | V _{IN} | V _{IN} and VLIN short. | 4.5 to 6.0 | V |

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---------------------|---|---------|-------|-------|------|
| | | | min | typ | max | |
| System | | | | | | |
| Comparator reference voltage | V _{REF} | | 0.818 | 0.826 | 0.834 | V |
| Current drain 1 | I _{CC1} | TD1, TD2 = 5V (Excluding Ciss charge.) | 2 | 4 | 6 | mA |
| Current drain 2 | I _{CC2} | TD1, TD2 = 0V | 0.3 | 0.6 | 1.2 | mA |
| 5V supply voltage | VLIN5 | I _{VLIN5} = 0 to 10mA | 4.75 | 5.00 | 5.25 | V |
| Overcurrent detection comparator offset | V _{CLOS} | | -5 | | +5 | mV |
| Overcurrent detection reference current | I _{CL} | V _{IN} = 10 to 14V | 7.47 | 8.30 | 9.13 | μA |
| Soft start source current | I _{SSSC} | TD1, TD2 = 5V | -1.8 | -3.5 | -7.0 | μA |
| Soft start sink current | I _{SSSK} | TD1, TD2 = 0V | 0.2 | 1.0 | | mA |
| Soft start clamp voltage | V _{SSTO} | | 1.2 | 1.6 | 2.0 | V |
| UV_DELAY source current | I _{SCUVD} | UV_DELAY = 2V | -4.3 | -8.6 | -17.2 | μA |
| UV_DELAY sink current | I _{SKUVD} | UV_DELAY = 2V | 0.2 | 1.0 | | mA |
| UV_DELAY threshold voltage | V _{UVD} | | 1.5 | 2.4 | 3.5 | V |
| UV_DELAY operating voltage | V _{UVD op} | 100% at V _{FB} = V _{REF} | 87 | 92 | 97 | % |
| VUVP detection hysteresis | ΔV _{UVP} | | | 2 | | % |
| Overvoltage detection | V _{OVP} | 100% at V _{FB} = V _{REF} | 112 | 117 | 122 | % |
| Overvoltage detection delay time | V _{ODLY} | | | 1.0 | | μS |
| Output discharge transistor on-resistance | V _{SWON} | | 5 | 10 | 20 | Ω |
| Output Block | | | | | | |
| CBOOT leakage current | I _{CBOOT} | V _{CBOOT} = V _{SW} + 6.5V | | | 10 | μA |
| HDRVx and LDRVx source current | I _{SCDRV} | | | 1.0 | | A |
| HDRVx and LDRVx sink current | I _{SKDRV} | | | 1.0 | | A |
| HDRVx low side on-resistance | R _{HDRV} | I _{OUT} =500mA | | 1.5 | 2.5 | Ω |
| LDRVx low side on-resistance | R _{LDRV} | I _{OUT} =500mA | | 1.5 | 2.5 | Ω |
| Simultaneous on prevention dead time 1 | T _{dead1} | LDRV off → HDRV on | | 50 | | nS |
| Simultaneous on prevention dead time 2 | T _{dead2} | HDRV off → LDRV on | | 120 | | nS |

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LV5044V

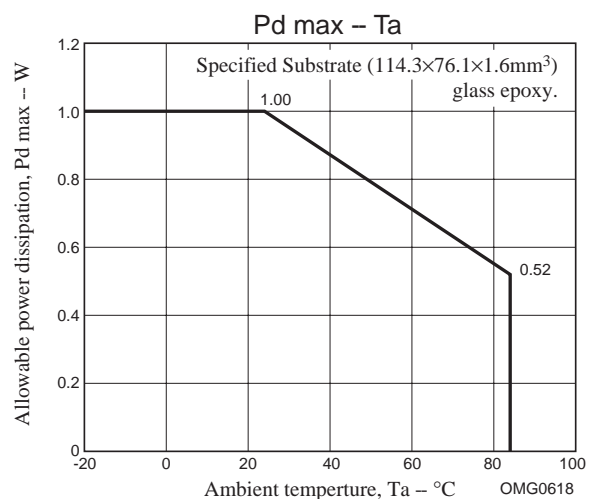
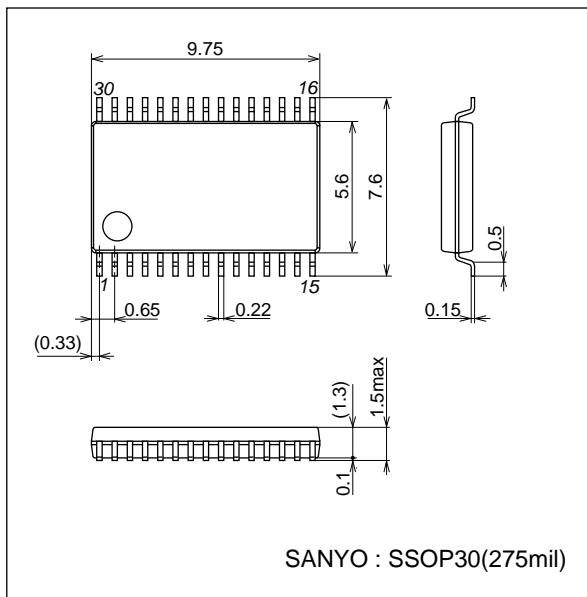
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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------|-------------------------------|----------------------|------|----------------------|-----------|
| | | | min | typ | max | |
| Oscillator | | | | | | |
| Oscillator frequency | f_{OSC} | CT = 130pF | 280 | 330 | 380 | kHz |
| Oscillator frequency range | $f_{OSC\ op}$ | | 250 | | 1100 | kHz |
| Maximum on duty | $D_{ON\ max}$ | CT = 130pF | 82 | | | % |
| Minimum on time | $T_{ON\ min}$ | CT = 130pF | | 100 | | nS |
| Sawtooth wave high side voltage | V_{sawH} | $f_{OSC} = 300kHz$ | | 2.2 | 2.6 | V |
| Sawtooth wave low side voltage | V_{sawL} | $f_{OSC} = 300kHz$ | | 1 | 1.2 | V |
| On time difference between channels 1 and 2 | ΔT_{dead} | | | 5 | | % |
| Error Amplifier | | | | | | |
| Error amplifier input current | I_{FB} | | -200 | -100 | 200 | nA |
| COMP pin source current | I_{COMPSC} | | | -100 | -18 | μA |
| COMP pin sink current | $I_{COMP SK}$ | | 18 | 100 | | μA |
| Error amplifier gm | gm | | 500 | 700 | 900 | μmho |
| Current detection amplifier gain | $G_{I\ SNS}$ | | 1.5 | 2.0 | 2.5 | dB |
| Logic Output | | | | | | |
| Sink current in the power good low state | I_{pwrgdL} | $V_{PGOOD} = 0.4V$ | 0.5 | 1.0 | | mA |
| Leakage current in the power good high state | I_{pwrgdH} | $V_{PGOOD} = 12V$ | | | 10 | μA |
| TD pin threshold level | V_{ONTD} | When the TD pin is stepped up | 1.5 | 2.4 | 3.5 | V |
| TD pin open voltage | V_{TDH} | $V_{IN} - V_{LIN5\ open}$. | 4.5 | 5.0 | 5.5 | V |
| TD pin source current during charge | I_{TDSC} | | -1.8 | -3.5 | -7.0 | μA |
| TD pin sink current during discharge | I_{TDSK} | | 0.8 | 2 | 5 | mA |
| CLKO high-level voltage | V_{CLKOH} | $I_{CLKO} = 1mA$ | 0.7V _{LIN5} | | | V |
| CLKO low-level voltage | V_{CLKOL} | $I_{CLKO} = 1mA$ | | | 0.3V _{LIN5} | V |
| Protection Functions | | | | | | |
| V_{IN} UVLO release voltage | V_{UVLO} | | 3.5 | 4.1 | 4.3 | V |
| UVLO hysteresis | ΔV_{UVLO} | | | 0.2 | | V |

Package Dimensions

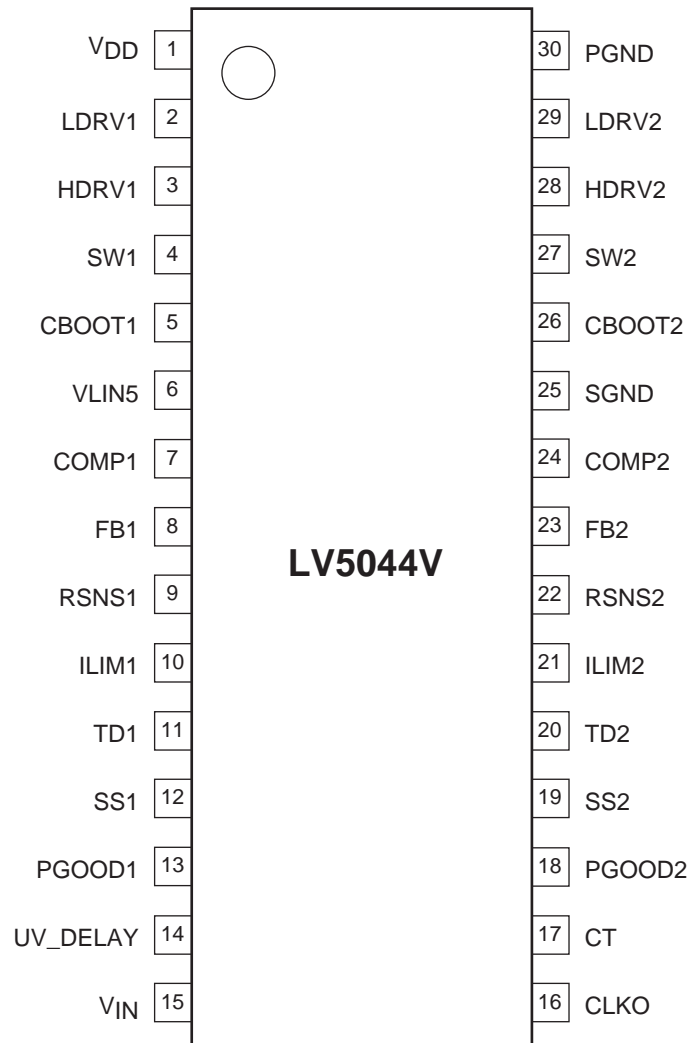
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LV5044V

Pin Assignment



Top view

LV5044V

Pin Functions

| Pin No. | Pin | Function |
|---------|-----------------|---|
| 1 | V _{DD} | Gate drive power supply for the external low side MOSFETs. Connect this pin to VLIN5 through a filter. |
| 2 | LDRV1 | Channel 1 external low side MOSFET gate drive. This pin is also used as the signal input for short through prevention for the high and low side MOSFETs. HDRV cannot be turned on unless this pin's voltage goes below 1V. |
| 3 | HDRV1 | Channel 1 external high side MOSFET gate drive. |
| 4 | SW1 | This pin is connected to the channel 1 switching node. The external high side MOSFET source and the low side MOSFET drain are connected to this pin. This pin becomes the return current route of pin HDRV. The drain of the discharging MOSFET used for the soft stop function is connected internal in the IC (typ.15Ω). This pin is also used as the signal input for short through prevention for the high and low side MOSFETs. LDRV cannot be turned on unless this pin's voltage goes below 1V referenced to PGND. |
| 5 | CBOOT1 | Channel 1 bootstrap capacitor connection. The high side MOSFET gate drive power is supplied from this pin. This pin is connected to V _{DD} through a diode and to SW1 through the bootstrap capacitor. |
| 6 | VLIN5 | Internal 5V regulator output. The current is supplied from V _{IN} . The power supply for the IC internal control circuits is also supplied from this pin. A bypass capacitor (6.8μF) is required between this pin and SGND. This pin is monitored by the UVLO function and the IC starts operating when it first rises above 4.0V. (After starting, the IC will only stop if this voltage falls below 3.8V.) |
| 7 | COMP1 | Channel 1 phase compensation. The output of the internal transconductance amplifier is connected to this pin. The external phase compensation circuit between this pin and SGND. |
| 8 | FB1 | Channel 1 feedback input. The transconductance amplifier inverting (-) input is connected to this pin. Provide the feedback potential to this pin by voltage dividing the output voltage. The converter operates so that this pin goes to the internal reference voltage VREF, 0.8V. This pin is also monitored by both the UVP comparator and the OVP comparator. If this pin voltage falls to under 87% of the set voltage, the PGOOD1 pin will go low and the UV_TIMER will operate. If this pin voltage rises to over 117% of the set voltage, the IC will latch in the off state. |
| 9 | RSNS1 | Input for the channel 1 side overcurrent detection comparator and current detection amplifier. When resistor detection is used, connect the low side of the current detection resistor inserted between V _{IN} and the drain of the external high side MOSFET to this pin. These connections must be wired independently so that the shared impedance with the main current with respect to the detected voltage does not affect this circuit. |
| 10 | ILIM1 | Connection to the channel 1 overcurrent detection trip point. A 8.3μA (ILIM) sink constant-current supply is connected internal in the IC, and the overcurrent detection voltage ILIM × RLIM is generated by connecting the resistor RLIM between this pin and V _{IN} . The voltage between V _{IN} and ILIM is compared to the voltage across the terminals of either the current detection resistor RSNS or the high side MOSFET to detect the overcurrent state. |
| 11 | TD1 | Channel 1 startup delay connection. The time until the IC starts up after the power-on reset (POR) is cleared is set by the capacitor connected between this pin and SGND. After the POR state is cleared, the external capacitor is charged by a 3.5μA constant current supplied internally by the IC. The IC starts operation when the voltage on this pin exceeds 2.4V. The IC goes to the standby state when the voltage on this pin is under 2.4V. If no external capacitor is connected to this pin, the IC will start as soon as the power-on reset is cleared. |
| 12 | SS1 | Channel 1 soft start capacitor connection. After the power-on reset (POR) is cleared and the TD pin voltage exceeds 2.4V, this capacitor is charged by a 3.5μA internal constant current supply from the SS1 pin. This pin is connected to the transconductance amplifier's noninverting (+) input, and the ramp waveform of the SS1 pin is reflected in the ramped-up output waveform. After the UV_DELAY time out and the POR operates, this capacitor is discharged by the SS pin. |
| 13 | PGOOD1 | Channel 1 power good pin. An IC internal 28V MOSFET open drain is connected to this pin. This pin outputs a low level if the channel 1 output voltage falls more than -13% relative to the set voltage. There is a hysteresis of about VREF × 1.5%. |
| 14 | UV_DELAY | Channel 1 and channel 2 common UVP delay connection. The time until the IC switches off after the UVP state is detected is set by the capacitor connected between this pin and SGND. If either the channel 1 or channel 2 output voltage falls under -80% of the set voltage, an IC internal 8.6μA constant current source charges the external capacitor connected to this pin. When the voltage on this pin exceeds 2.4V, the IC switches off. If no external capacitor is connected, the IC turns off immediately upon detection of the UVP state. |
| 15 | V _{IN} | IC power supply. |
| 16 | CLKO | Clock output. This pin outputs a clock signal synchronized with the CT pin oscillator waveform. When two or more LV5044V chips are operated in synchronization, connect the CT pin of the slave device to the SLKO pin of the master device. If two or more devices are operated in synchronization and the Td pin is used to change the startup timing between the devices, the device that starts the soonest will be the master. |

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LV5044V

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| Pin No. | Pin | Function |
|---------|--------|--|
| 17 | CT | Connection for the oscillator circuit's external capacitor. Connect that capacitor between this pin and ground. When CT is 130pF, f_{OSC} will be 330kHz. If an external clock is applied to this pin, the PWM control functions will operate at that clock frequency. If an external clock is provided, that signal must be a square wave with a low level of 0V and a high level between 3.3 and 5.0V. The square wave generator must have a fanout drive capacity of at least 1mA, and UV_DELAY function doesn't operate when this pin is grounded. |
| 18 | PGOOD2 | Channel 2 power good pin. |
| 19 | SS2 | Channel 2 soft start function capacitor connection. |
| 20 | TD2 | Channel 2 startup delay connection. |
| 21 | ILIM2 | Channel 2 overcurrent detection trip point setting. |
| 22 | RSENS1 | Channel 2 overcurrent detection comparator input. |
| 23 | FB2 | Channel 2 feedback input. |
| 24 | COMP2 | Channel 2 phase compensation. |
| 25 | SGND | IC system ground. The reference voltage is generated referenced to this pin. The system ground must be connected to this pin. |
| 26 | CBOOT2 | Channel 2 bootstrap capacitor connection. |
| 27 | SW2 | This pin is connected to the channel 2 switching node. |
| 28 | HDRV2 | Channel 2 external high side MOSFET gate drive. |
| 29 | LDRV2 | Channel 2 external low side MOSFET gate drive. |
| 30 | PGND | Power system ground. This pin is used as the current return path for the LDRV pin. |

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