HD74SSTV32852

24-bit to 48-bit Registered Buffer with SSTL_2 Inputs and Outputs

REJ03D0833-0400
(Previous: ADE-205-687C)
Rev.4.00
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Description

The HD74SSTV32852 is a 24-bit to 48-bit registered buffer designed for 2.3 V to 2.7 V Vcc operation and LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to QA, QB is controlled by differential clock pins (CLK, $\overline{\text{CLK}}$) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Features

- Supports LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Pinout optimizes DIMM PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV32852LBEL	LFBGA-114pin	PLBG0114GA-A (BP-114V)	LB	EL (1,000 pcs / Reel)

Function Table

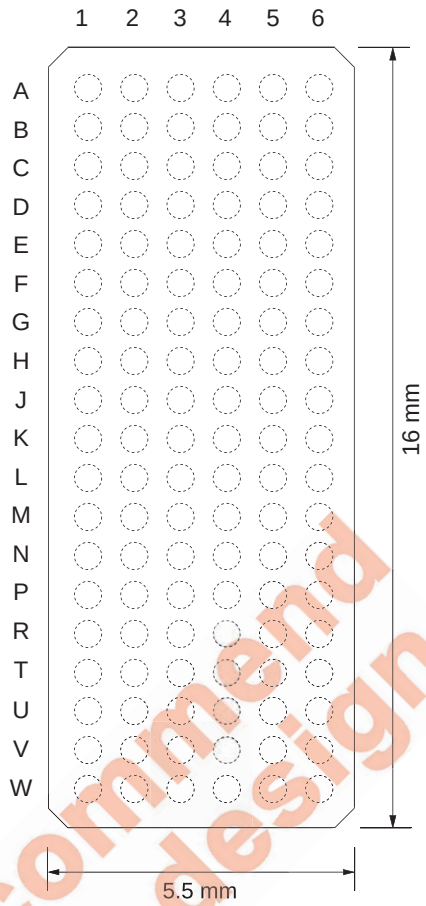
Inputs				Outputs	
$\overline{\text{RESET}}$ *2	$\overline{\text{CLK}}$	CLK	D	QA	QB
L	X or floating	X or floating	X or floating	L	L
H	↓	↑	H	H	H
H	↓	↑	L	L	L
H	L or H	H or L	X	Q_0 *1	Q_0 *1

H : High level
L : Low level
X : Immaterial
↑ : Low to high transition
↓ : High to low transition

Notes: 1. Output level before the indicated steady state input conditions were established.
2. See under the figure.

Pin Arrangement

Height 1.4 mm
0.8 mm pitch
0.5 mm 114-Ball



(Top view)

Terminal Assignment

	1	2	3	4	5	6
A	Q2A	Q1A	CLK	$\overline{CLK}$	Q1B	Q2B
B	Q3A	V_{DDQ}	GND	GND	V_{DDQ}	Q3B
C	Q5A	Q4A	V_{DDQ}	V_{DDQ}	Q4B	Q5B
D	Q7A	Q6A	GND	GND	Q6B	Q7B
E	Q8A	GND	V_{DDQ}	V_{DDQ}	GND	Q8B
F	Q10A	Q9A	V_{DDQ}	V_{DDQ}	Q9B	Q10B
G	Q12A	Q11A	GND	GND	Q11B	Q12B
H	Q13A	V_{CC}	V_{DDQ}	V_{DDQ}	V_{CC}	Q13B
J	Q14A	Q15A	GND	GND	Q15B	Q14B
K	Q17A	Q16A	V_{DDQ}	V_{DDQ}	Q16B	Q17B
L	Q18A	Q19A	GND	GND	Q19B	Q18B
M	Q20A	V_{DDQ}	GND	GND	V_{DDQ}	Q20B
N	Q22A	Q21A	V_{DDQ}	V_{DDQ}	Q21B	Q22B
P	Q23A	V_{DDQ}	GND	GND	V_{DDQ}	Q23B
R	Q24A	V_{CC}	$\overline{RESET}$	V_{REF}	V_{CC}	Q24B
T	D2	D1	D6	D18	D13	D14
U	D4	D3	D10	D22	D15	D16
V	D5	D7	D11	D23	D19	D17
W	D8	D9	D12	D24	D21	D20

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	–0.5 to 3.6	V	
Input voltage [*1]	V_I	–0.5 to V_{DDQ}+0.5	V	
Output voltage [*1]	V_O	–0.5 to V_{DDQ}+0.5	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}
V_{CC}, V_{DDQ} or GND current / pin	I_{CC}, I_{DDQ} or I_{GND}	±100	mA	
Package thermal impedance	θ_{JA}	36	°C/W	
Storage temperature	Tstg	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

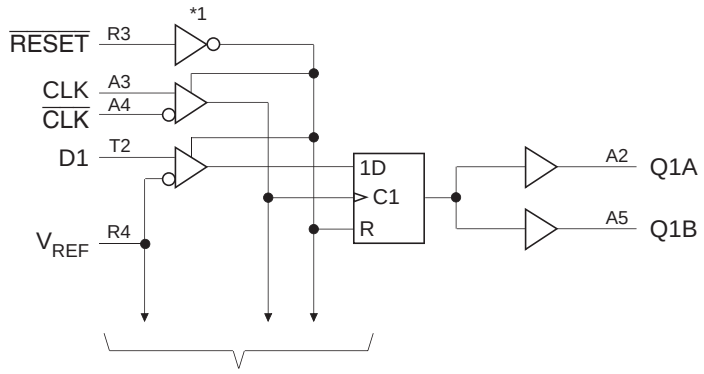
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage		V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage		V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage		V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage		V_{TT}	V_{REF}–40 mV	V_{REF}	V_{REF}+40 mV	V	
Input voltage		V_I	0	—	V_{CC}	V	
AC high level input voltage		V_{IH}	V_{REF}+310 mV	—	—	V	D
AC low level input voltage		V_{IL}	—	—	V_{REF}–310 mV	V	D
DC high level input voltage		V_{IH}	V_{REF}+150 mV	—	—	V	D
DC low level input voltage		V_{IL}	—	—	V_{REF}–150 mV	V	D
High level input voltage		V_{IH}	1.7	—	V_{DDQ}+0.3	V	$\overline{\text{RESET}}$
Low level input voltage		V_{IL}	–0.3	—	0.7	V	$\overline{\text{RESET}}$
Differential input voltage	(Common mode range)	V_{CMR}	0.97	—	1.53	V	CLK, $\overline{\text{CLK}}$
	(Minimum peak to peak input)	V_{PP}	360	—	—	mV	CLK, $\overline{\text{CLK}}$
High level output current		I_{OH}	—	—	–20	mA	
Low level output current		I_{OL}	—	—	20	mA	
Operating temperature		Ta	0	—	70	°C	

Note: The $\overline{\text{RESET}}$ input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

Logic Diagram



Note: 1. $\overline{\text{RESET}}$ input gate is connected to V_{DDQ}.

Electrical Characteristics

Item		Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage		V_{IK}	2.3	—	—	–1.2	V	I_{IN} = –18 mA
Output voltage		V_{OH}	2.3 to 2.7	V_{CC}–0.2	—	—	V	I_{OH} = –100 µA
			2.3	1.95	—	V_{DDQ}		I_{OH} = –16 mA
		V_{OL}	2.3 to 2.7	—	—	0.2		I_{OL} = 100 µA
			2.3	0	—	0.35		I_{OL} = 16 mA
Input current	(All inputs)	I_{IN}	2.7	—	—	±5	µA	V_{IN} = 2.7 V or 0
Quiescent supply current		I_{CC} *2	2.7	—	—	35	mA	V_{IN} = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0
Standby current		$I_{CC\ (stdy)}$	2.7	—	—	10	µA	$\overline{\text{RESET}}$ = GND
Dynamic operating clock only		I_{CCD} *2	2.7	—	80	—	µA/ clock MHz	$\overline{\text{RESET}}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle
Dynamic operating per each data input		I_{CCD} *2	2.7	—	14	—	µA/ clock MHz/ data input	$\overline{\text{RESET}}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.
Output high *3		r_{OH}	2.3 to 2.7	7	—	20	Ω	I_{OH} = –20 mA
Output low *3		r_{OL}	2.3 to 2.7	7	—	20	Ω	I_{OL} = 20 mA
$\lvert r_{OH} - r_{OL} \rvert$ each separate bit *3		$r_{O(\Delta)}$	2.5	—	—	4	Ω	I_O = 20 mA, Ta = 25°C
Input capacitance	Data inputs	C_{IN}	2.5 *1	4.0	—	5.0	pF	V_I = V_{REF}±310 mV
	CLK and $\overline{\text{CLK}}$			3.0	—	4.0		V_{CMR} = 1.25 V, V_{PP} = 360 mV
	$\overline{\text{RESET}}$			3.5	—	5.0		V_I = V_{CC} or GND

Notes: 1. All typical values are at V_{CC} = 2.5 V, Ta = 25°C.
2. Total I_{CC} (max) = I_{CC} + {I_{CCD} (clock)×f(clock)} + {I_{CCD} (Data)×1/2f(clock)×24}
3. This is effective in the case that it did terminate by resistance.

Switching Characteristics

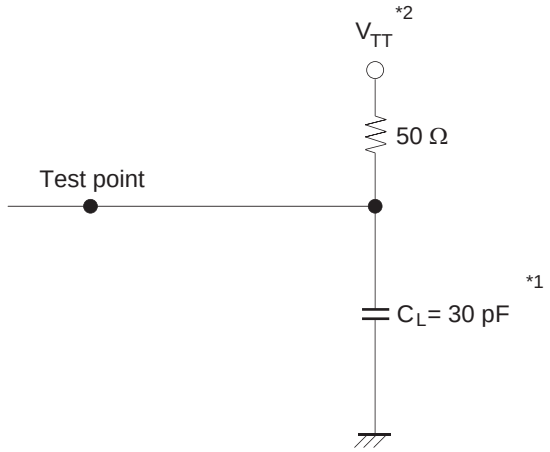
Item		Symbol	V_{CC} = 2.5 ± 0.2 V		Unit	Test Condition
			Min	Max		
Clock frequency *1		f_{clock}	—	200	MHz	
Setup time	Fast slew rate *4, 6	t_{su}	0.75	—	ns	Data before CLK↑, $\overline{CLK}$↓
	Slow slew rate *5, 6		0.9	—		
Hold time	Fast slew rate *4, 6	t_h	0.75	—	ns	Data after CLK↑, $\overline{CLK}$↓
	Slow slew rate *5, 6		0.9	—		
Differential inputs active time		t_{act}	22	—	ns	Data inputs must be low after $\overline{RESET}$ high.
Differential inputs inactive time		t_{inact}	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ low.
Pulse width		t_w	2.5	—	ns	CLK, $\overline{CLK}$ "H" or "L"
Output slew *3		t_{SL}	1	4	volt/ns	

(C_L = 30 pF, R_L = 50 Ω, V_{REF} = V_{TT} = V_{DDQ} × 0.5)

Item	Symbol	V_{CC} = 2.5 ± 0.2 V			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f_{max}	200	—	—	MHz		
Propagation delay time *2	t_{PLH}, t_{PHL}	1.1	—	3.1	ns	CLK, $\overline{CLK}$	QA, QB
	t_{PHL}	—	—	5.0		$\overline{RESET}$	QA, QB

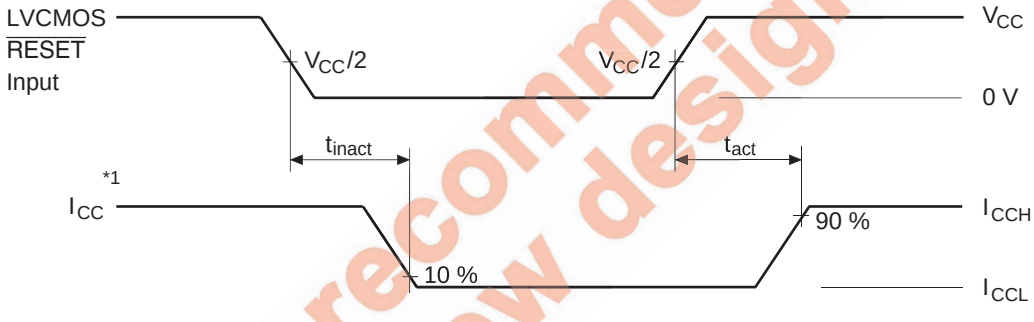
Notes: 1. Although the clock is differential, all timing is relative to CLK going high and $\overline{CLK}$ going low.
2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
6. CLK, $\overline{CLK}$ signals input slew rates are ≥ 1 V/ns.

Test Circuit

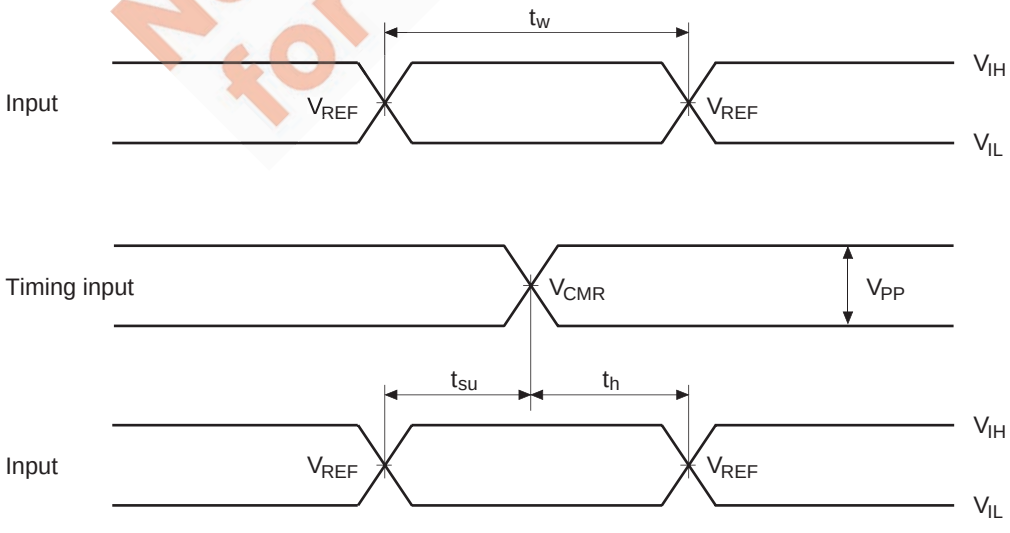


Notes: 1. C_L includes probe and jig capacitance.
2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

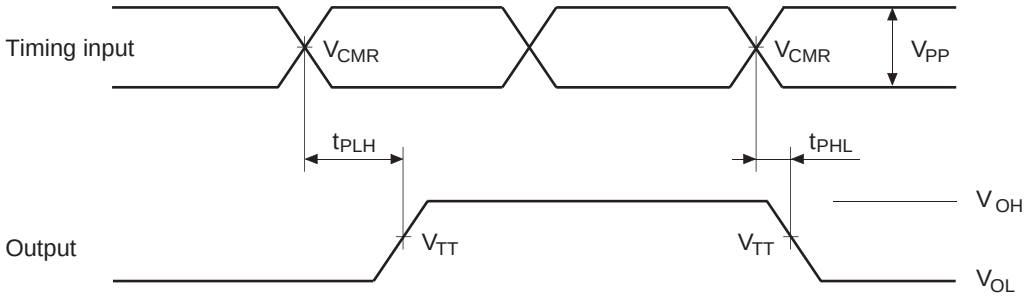
Waveforms – 1



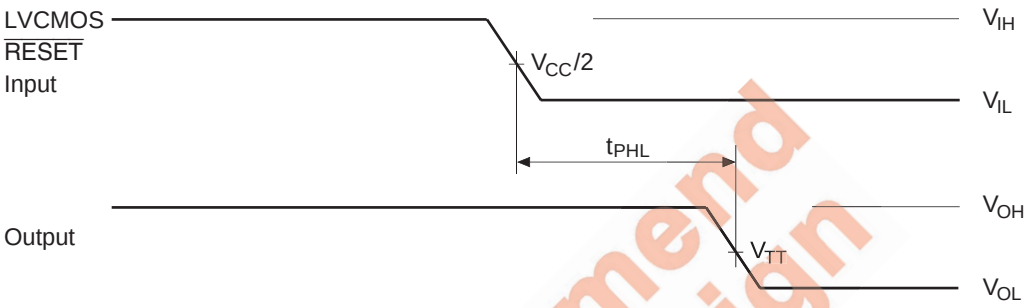
Waveforms – 2



Waveforms – 3



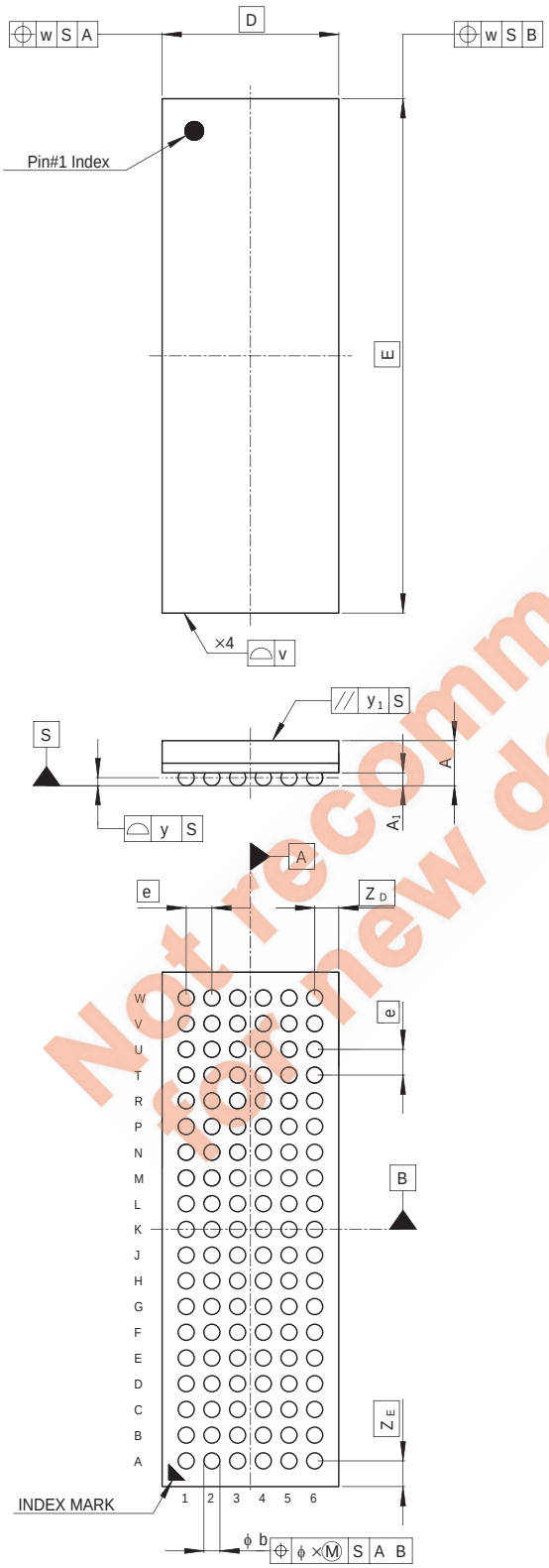
Waveforms – 4



Notes:
1. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
2. All input pulses are supplied by generators having the following characteristics : PRR ≤ 10 MHz, Zo = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
3. The outputs are measured one at a time with one transition per measurement.
4. $V_{TT} = V_{REF} = V_{DDQ}/2$
5. $V_{IH} = V_{REF}$+310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
6. $V_{IL} = V_{REF}$–310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
7. t_{PLH} and t_{PHL} are the same as t_{pd}

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA114-5.5x16-0.80	PLBG0114GA-A	BP-114/BP-114V	0.22g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.50	—
E	—	16.00	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.40	0.50	0.60
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.75	—
Z_E	—	0.80	—

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