CVLD-025 Model
5X7 mm SMD, **2.5V, LVDS**

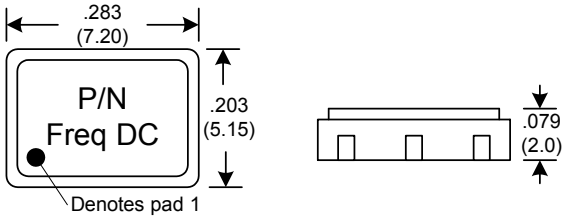
Lead Free RoHS Compliant

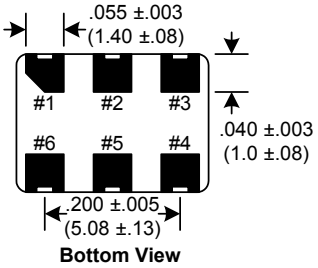
Differential LVDS Voltage Controlled Clock Oscillator

Frequency Range:		50MHz to 200MHz
Temperature Range:		0°C to 70°C
Storage:		-45°C to 90°C
Input Voltage:		2.5V ± 0.125V
Control Voltage:		1.25V ± 1.25V
Input Current:		50mA Typ, 80mA Max
Output:		Differential LVDS
Symmetry:		40/60% Max @ 50% Vdd
Rise/Fall Time:		1ns Max
Pulling Range:		±50ppm APR Min. (std)
Linearity:		± 10% Max
Logic:	Terminated 100ohms	(Offset 1.25V Typ.)
	Temp. 0°C to 70°C	"0" = 1.10 Typical
		"1" = 1.43 Typical
Jitter:	12KHz to 20MHz	0.5psec Typ., 1psec RMS Max
Aging:		<5ppm 1st/yr, <2ppm every year thereafter

Designed to meet today's requirements for 2.5V Differential LVDS applications. The CVLD-025 provides very low phase noise & jitter for demanding applications. Available on 16mm tape and reel in quantities of 1,000pcs..

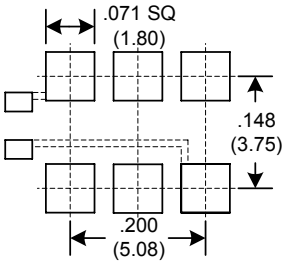
Dimensions inches (mm)
All dimensions are Max unless otherwise specified.





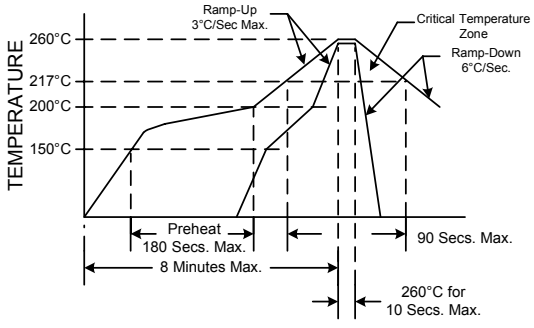
Bottom View

SUGGESTED PAD LAYOUT



Bypass Capacitor Recommended

RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

Crystek Part Number Guide

CVLD-025 _ - 50 - 155.520
#1 #2 #3 #4 #5

#1 Crystek 5x7 SMD PECL VCXO
#2 Model 025 = 2.5V
#3 Temp. Range: Blank = 0/70°C
#4 Pulling: (see Table 1)
#5 Frequency in MHz: 3 or 6 decimal places

Pulling (APR) Min.	
Blank	± 100ppm
50 (std)	± 50ppm

Table 1

Example:
CVLD-025-50-155.520 = 2.5V, 40.60, 0/70°C, 50ppm APR, 155.520 MHz

Pad	Connection
1	Volt Cont.
2	E/D
3	GND
4	OUT
5	COUT
6	Vdd

Enable/Disable Function	
E/D pin	Output pin
Open	Active
"1" level 2.2V Min	Active
"0" level 0.4V Max	High Z

Specifications subject to change without notice. TD-070301 Rev.A

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