P4C1024L
LOW POWER 128K x 8
CMOS STATIC RAM

FEATURES

- **V_{CC} Current (Commercial/Industrial)**
  - **— Operating: 70mA/85mA**
  - **— CMOS Standby: 100µA/100µA**
- **Access Times**
  - **—55/70 (Commercial or Industrial)**
- **Single 5 Volts ±10% Power Supply**
- **Easy Memory Expansion Using $\overline{CE}_1$, CE_2 and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
  - **—32-Pin 600 mil Plastic and Ceramic DIP**
  - **—32-Pin 445 mil SOP**
  - **—32-Pin TSOP**

DESCRIPTION

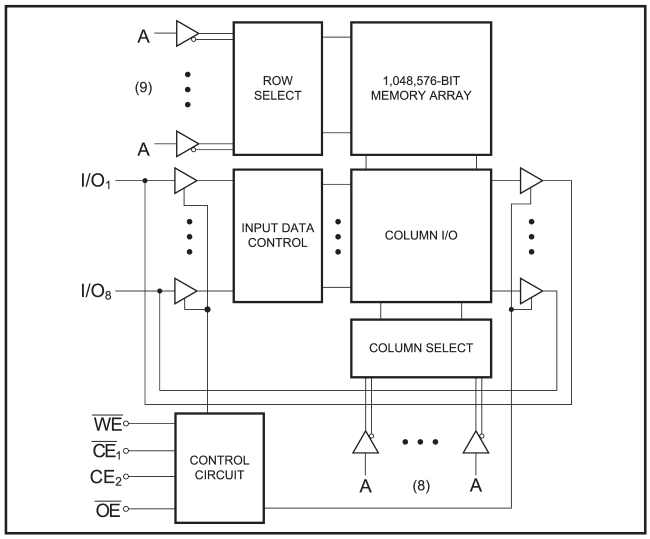
The P4C1024L is a 1,048,576-bit low power CMOS static RAM organized as 128Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

Access times of 55 ns and 70 ns are availale. CMOS is utilized to reduce power consumption to a low level.

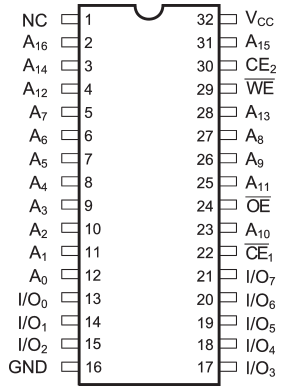
The P4C1024L device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{16}. Reading is accomplished by device selection ($\overline{CE}_1$ low and CE_2 high) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}_1$ or $\overline{OE}$ is HIGH or $\overline{WE}$ or CE_2 is LOW.

The P4C1024L is packaged in a 32-pin TSOP, 445 mil SOP, and a 600 mil PDIP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP (P600, C10), SOP (S12)
TOP VIEW

See end of datasheet for TSOP pin configuration.

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Temperature Range (Ambient)	Supply Voltage
Commercial (0°C to 70°C)	$4.5V \le V_{CC} \le 5.5V$
Industrial (-40°C to 85°C)	$4.5 \le V_{CC} \le 5.5V$

MAXIMUM RATINGS[1]

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage with Respect to GND	-0.5	7.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	V_{CC} + 0.5	V
T_A	Operating Ambient Temperature	-55	125	°C
S_{TG}	Storage Temperature	-65	150	°C
I_{OUT}	Output Current into Low Outputs		25	mA
I_{LAT}	Latch-up Current	>200		mA

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output High Voltage (I/O_0 - I/O_7)	I_{OH} = –1mA, V_{CC} = 4.5V	2.4		V
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 2.1mA		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$ Ind'l. Com'l.	-5 -2	+5 +2	µA
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$ Ind'l. $\overline{CE}_1 \ge V_{IH}$ or $CE_2 \le V_{IL}$ Com'l.	-5 -2	+5 +2	µA
I_{SB}	V_{CC} Current TTL Standby Current (TTL Input Levels)	V_{CC} = 5.5V, I_{OUT} = 0 mA $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$		3	mA
I_{SB1}	V_{CC} Current CMOS Standby Current (CMOS Input Levels)	V_{CC} = 5.5V, I_{OUT} = 0 mA $\overline{CE}_1 \ge V_{CC}$-0.2V, $CE_2 \le 0.2V$		100	µA

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	*		**		Unit
			-55	-70	-55	-70	
I_{CC}	Dynamic Operating Current	Commercial	70	70	15	15	mA
		Industrial	85	85	25	25	mA

*Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate.
The device is continuously enabled for writing, i.e., $CE_2 \geq V_{IH}$ (min), $\overline{CE}_1$ and $\overline{WE} \leq V_{IL}$ (max), $\overline{OE}$ is high. Switching inputs are 0V and 3V.

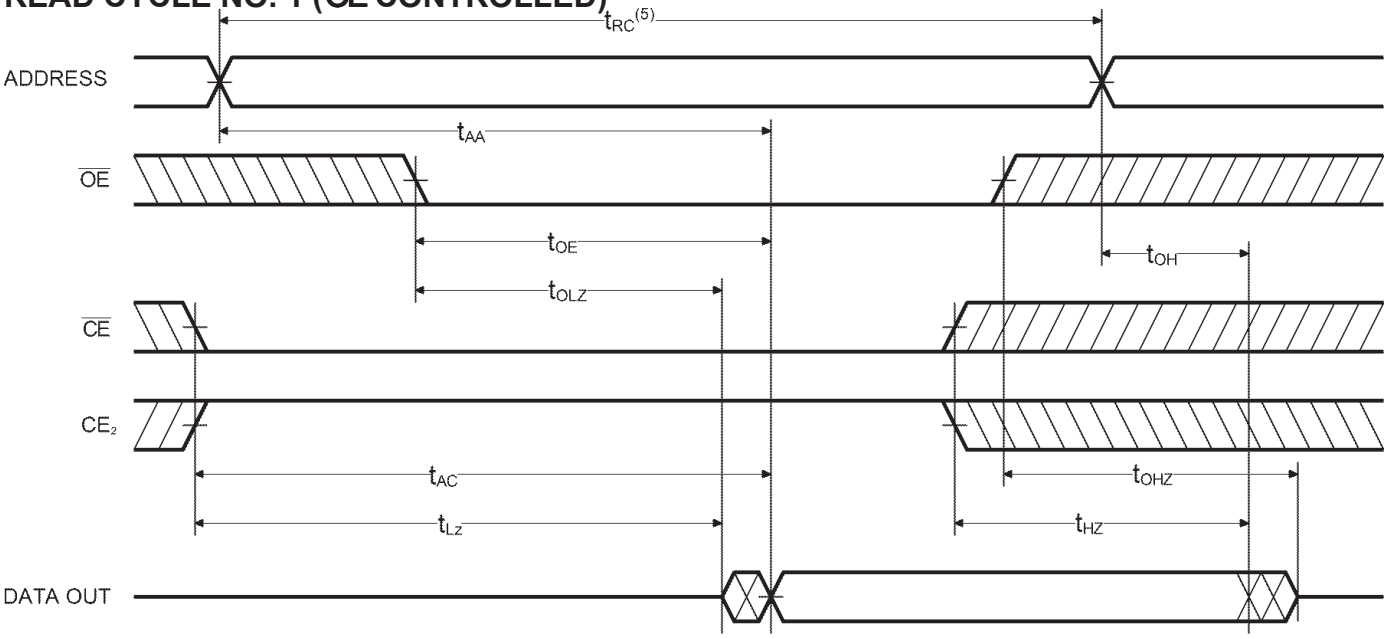
**As above but @ f=1 MHz and V_{IL}/ V_{IH} = 0V/ V_{CC}.

AC ELECTRICAL CHARACTERISTICS - READ CYCLE

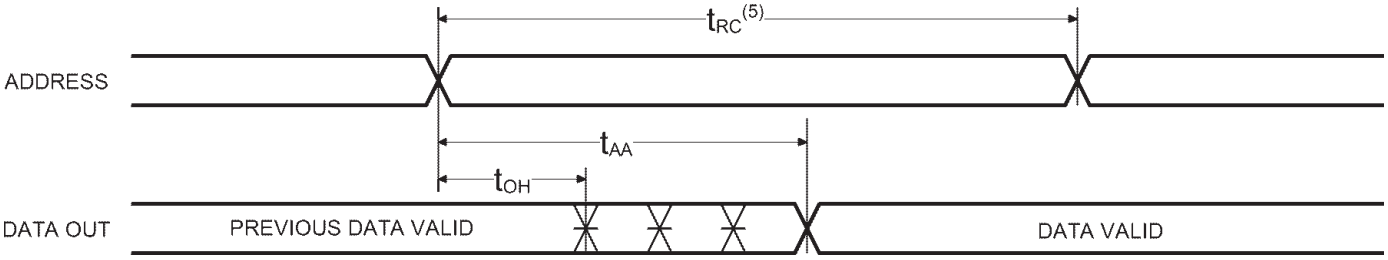
(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-55		-70		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address Access Time		55		70	ns
t_{AC}	Chip Enable Access Time		55		70	ns
t_{OH}	Output Hold from Address Change	5		5		ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		ns
t_{HZ}	Chip Disable to Output in High Z		20		25	ns
t_{OE}	Output Enable Low to Data Valid		30		35	ns
t_{OLZ}	Output Enable Low to Low Z	5		5		ns
t_{OHZ}	Output Enable High to High Z		20		25	ns
t_{PU}	Chip Enable to Power Up Time	0		0		ns
t_{PD}	Chip Disable to Power Down Time		55		70	ns

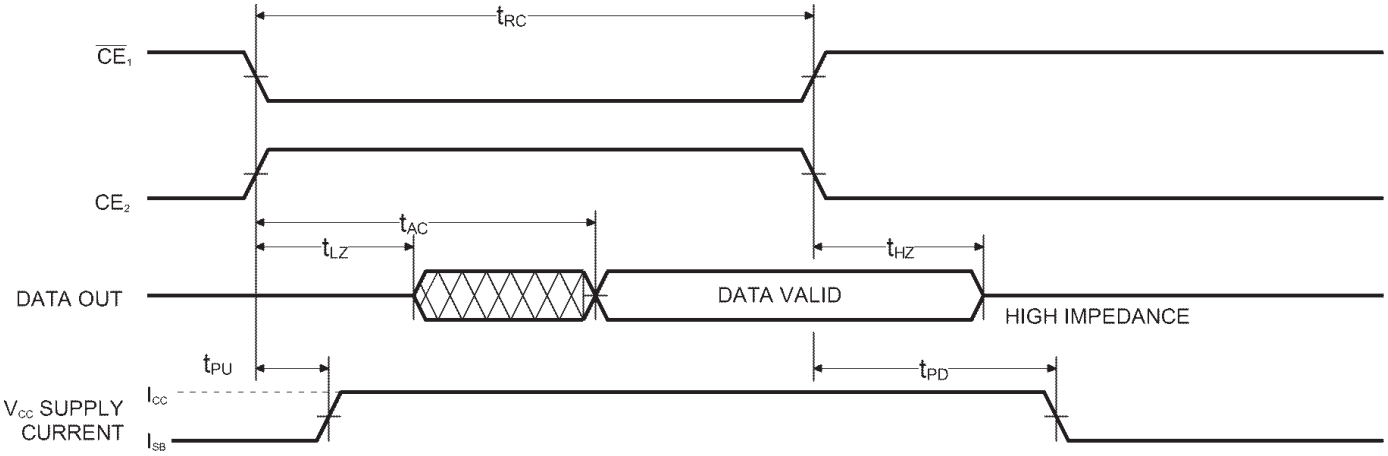
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[1]



READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)



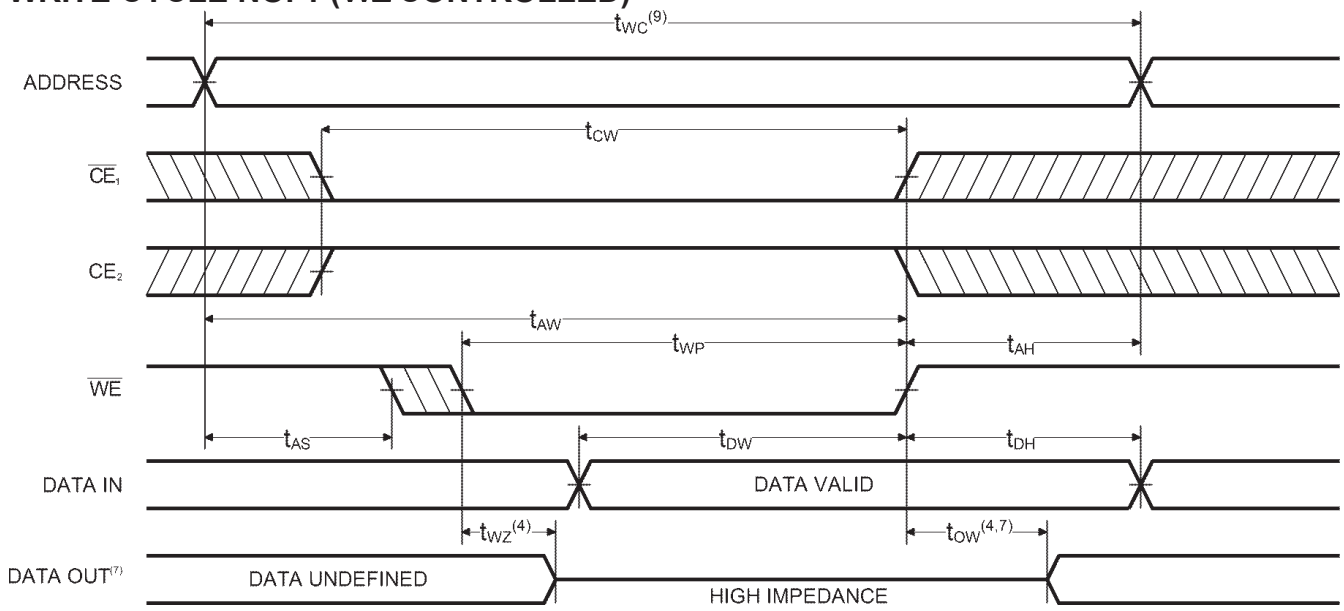
Notes:
1. $\overline{WE}$ is HIGH for READ cycle.
2. $\overline{CE_1}$ and $\overline{OE}$ is LOW, and CE_2 is HIGH for READ cycle.
3. ADDRESS must be valid prior to, or coincident with later of $\overline{CE_1}$ transition LOW or CE_2 transition HIGH.
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS - WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-55		-70		Unit
		Min	Max	Min	Max	
t_{WC}	Write Cycle Time	55		70		ns
t_{CW}	Chip Enable Time to End of Write	50		60		ns
t_{AW}	Address Valid to End of Write	50		60		ns
t_{AS}	Address Set-up Time	0		0		ns
t_{WP}	Write Pulse Width	40		50		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DW}	Data Valid to End of Write	25		30		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WZ}	Write Enable to Output in High Z		25		30	ns
t_{OW}	Output Active from End of Write	5		5		ns

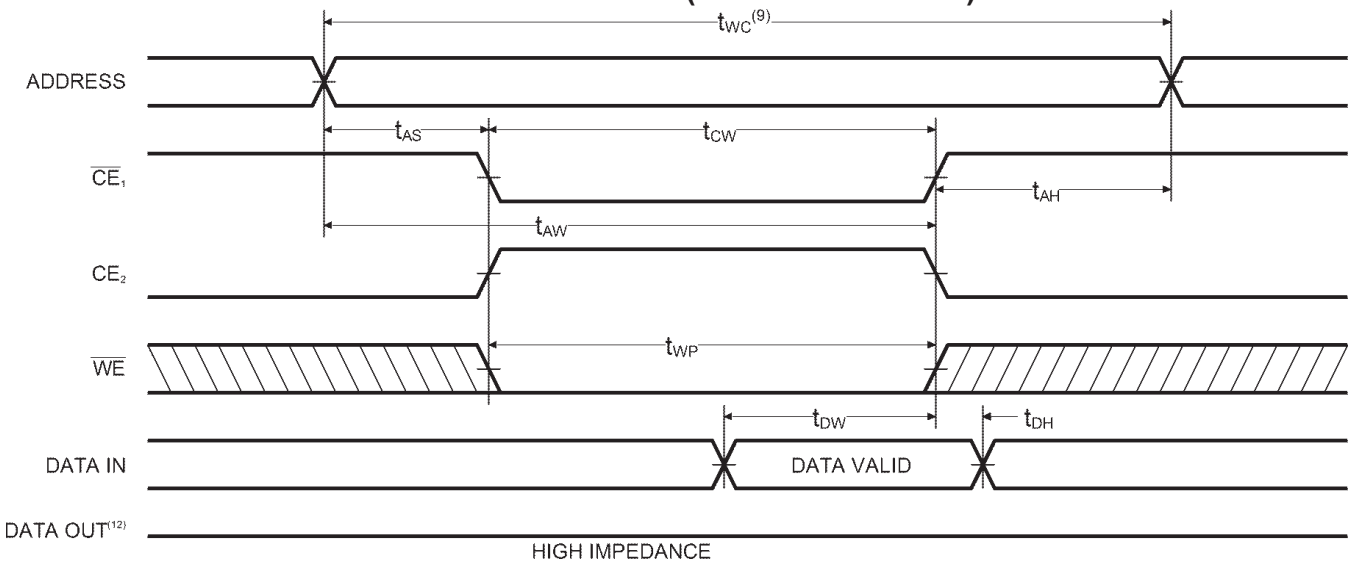
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[6]



Notes:

6. $\overline{CE_1}$ and $\overline{WE}$ are LOW and CE_2 is HIGH for WRITE cycle.
7. $\overline{OE}$ is LOW for this WRITE cycle to show twz and tow.
8. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
9. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CE}$ CONTROLLED)[6]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Fig. 1 and 2

TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

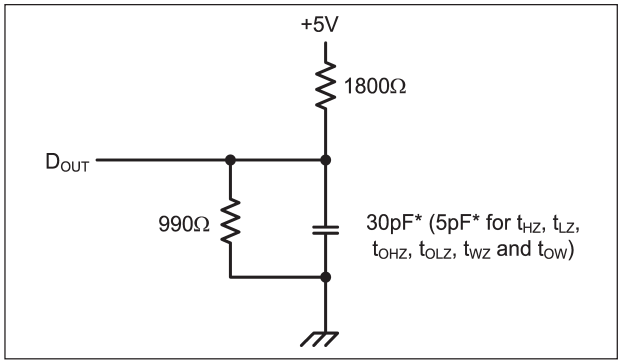


Figure 1. Output Load

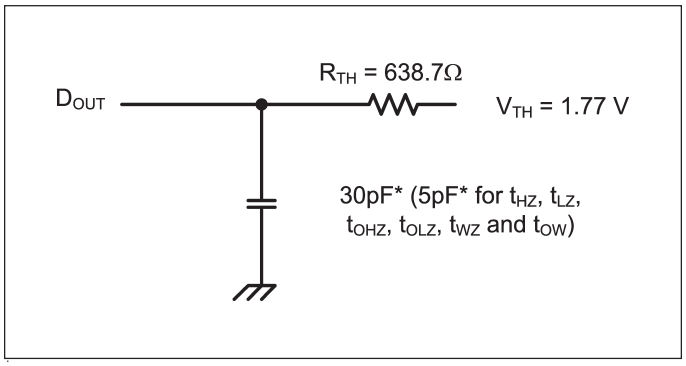


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the high speed of the P4C1024L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground.

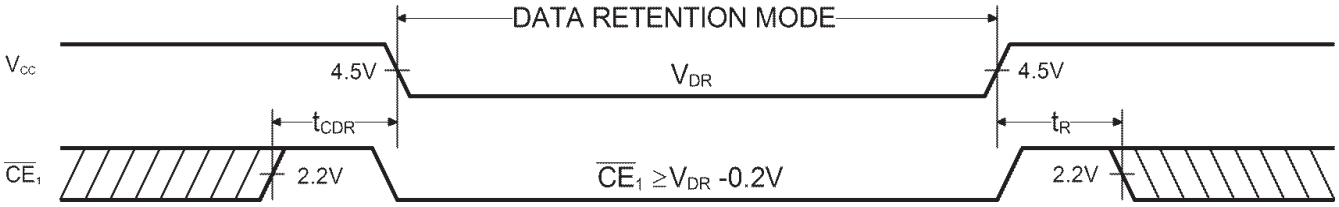
To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589Ω resistor must be used in series with D_{OUT} to match 639Ω (Thevenin Resistance).

DATA RETENTION

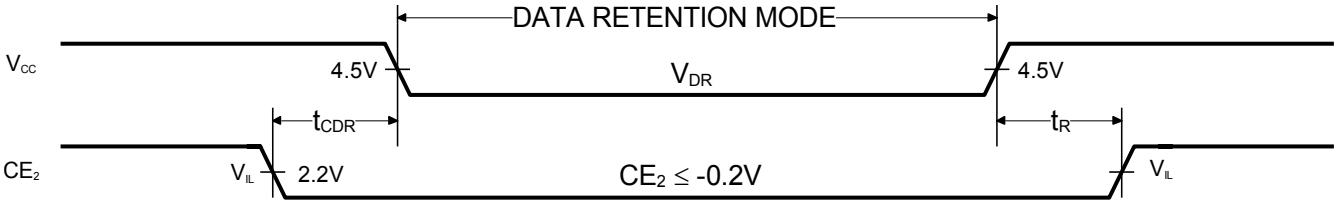
Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CE_1} \geq V_{CC}$ -0.2V, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$	2.0	5.5	V
I_{CCDR} (1)	Data Retention Current	V_{DR} = 2.0V		30	µA
		V_{DR} = 3.0V		50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operating Recovery Time		5		ms

1. $\overline{CE_1} \geq V_{DR}$ -0.2V, $CE_2 \geq V_{DR}$ -0.2V or $CE_2 \leq 0.2V$; or $\overline{CE_1} \leq 0.2V$, CE_2 - 0.2V; $V_{IN} \geq V_{DR}$ -0.2V or $V_{IN} \leq 0.2V$

LOW V_{CC} DATA RETENTION WAVEFORM 1 ($\overline{CE_1}$ CONTROLLED)



LOW V_{CC} DATA RETENTION WAVEFORM 2 (CE_2 CONTROLLED)



ORDERING INFORMATION

P4C1024L — Device Type

xx — Speed
- 55, 70 ns

x — Package
- CW Ceramic DIP (600 mil)
- P Plastic DIP (600 mil)
- S SOP (445 mil)
- T TSOP

x — Processing
- C 0°C to +70°C
- I -40°C to +85°C

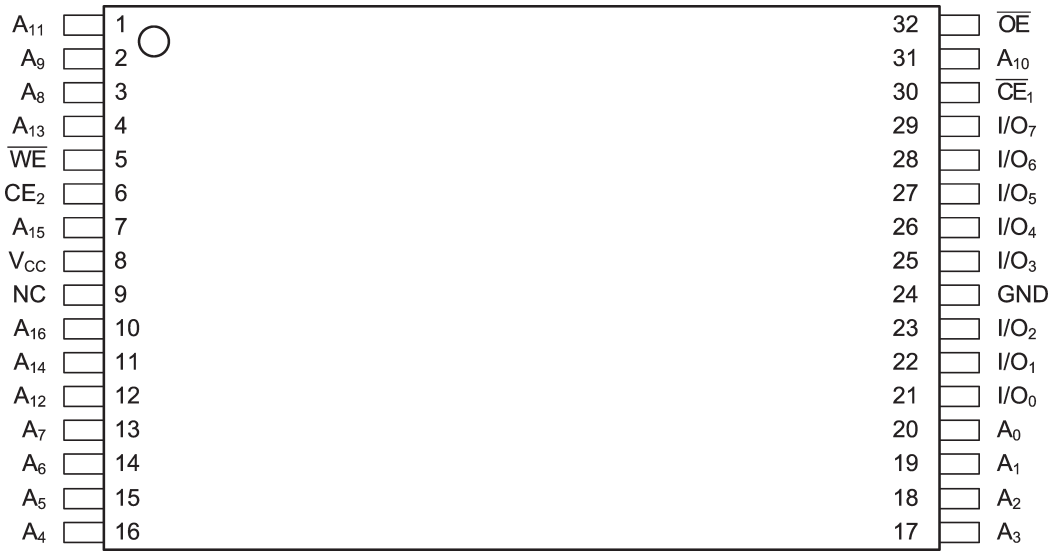
128K x 8 SRAM

SELECTION GUIDE

The P4C1024L is available in the following temperature, speed and package options.

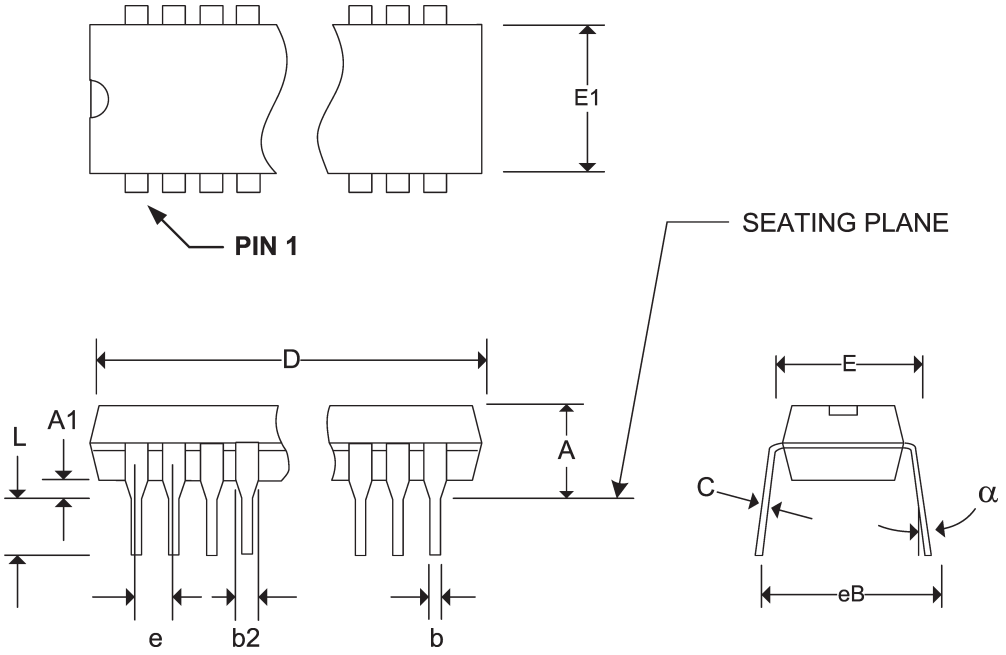
Temperature Range	Package	Speed	
		-55	-70
Commercial	Plastic DIP (600 mil)	-55PC	-70PC
	Plastic SOP (445 mil)	-55SC	-70SC
	TSOP	-55TC	-70TC
	Ceramic DIP (600 mil)	-55CWC	-70CWC
Industrial	Plastic DIP (600 mil)	-55PI	-70PI
	Plastic SOP (445 mil)	-55SI	-70SI
	TSOP	-55TI	-70TI
	Ceramic DIP (600 mil)	-55CWI	-70CWI

TSOP PIN CONFIGURATION



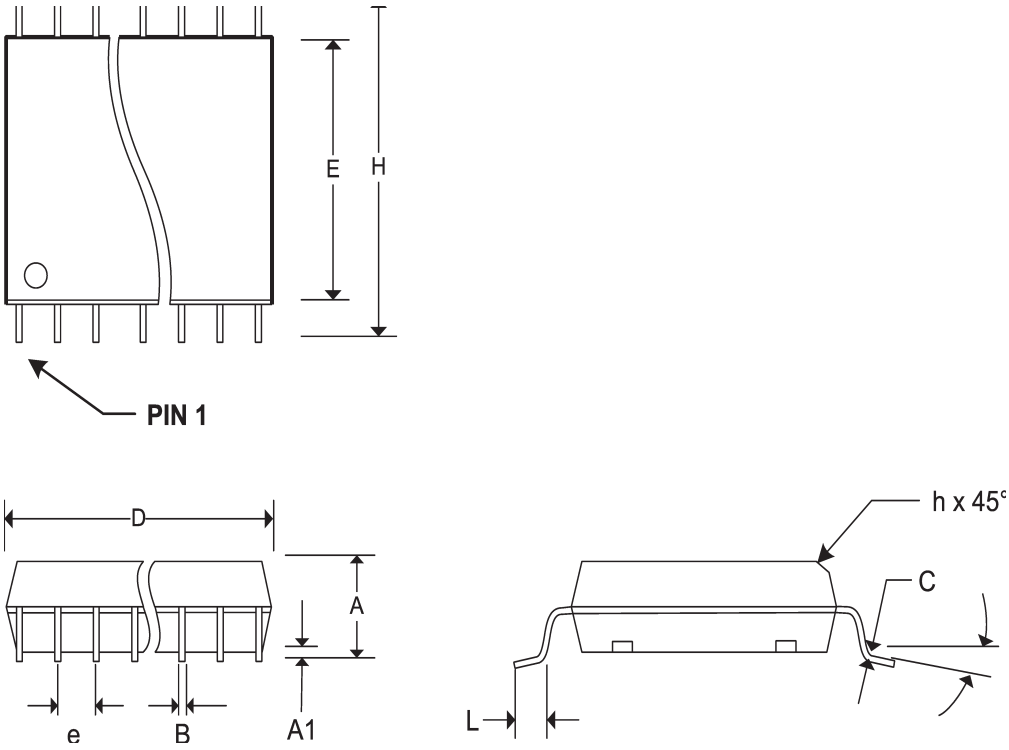
Pkg #	P600	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	0.170	0.210
A1	0.015	-
b	0.014	0.023
b2	0.045	0.070
C	0.009	0.014
D	1.600	1.400
E1	0.530	0.300
E	0.600	0.380
e	0.100 BSC	
eB	0.600 BSC	
L	0.120	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



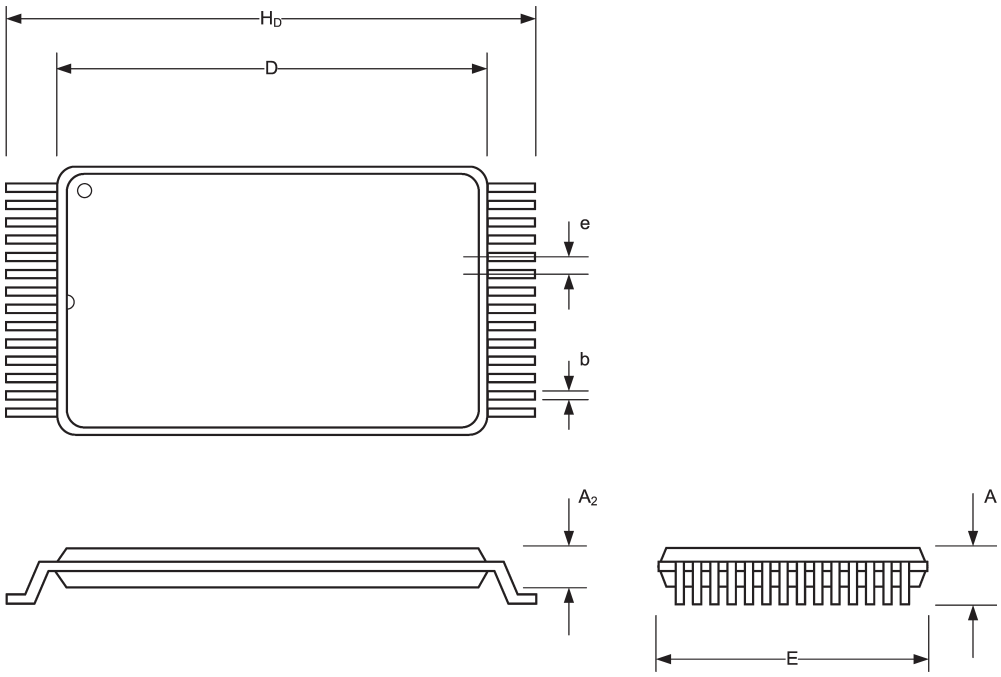
Pkg #	S12	
# Pins	32 (445 Mil)	
Symbol	**Min**	**Max**
A	-	0.118
A1	0.004	-
b2	0.014	0.020
C	0.006	0.012
D	0.790	0.820
e	0.050 BSC	
E	0.435	0.455
H	0.546	0.566
h	0.010	0.029
L	0.023	0.039
α	0°	8°

SOIC/SOP SMALL OUTLINE IC PACKAGE



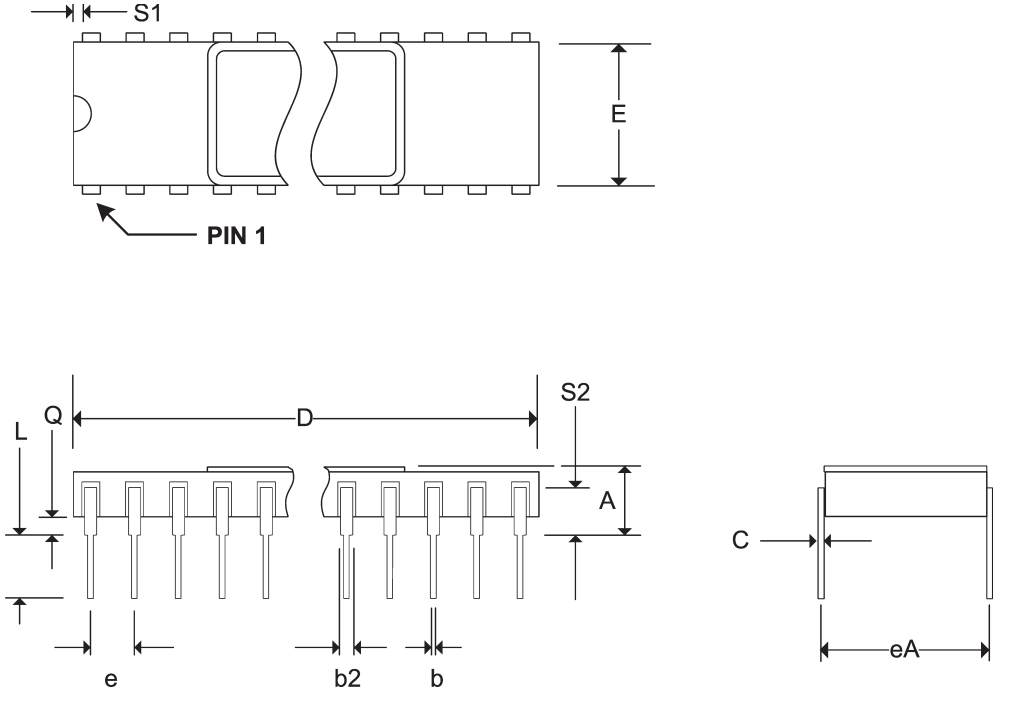
Pkg #	T3	
# Pins	32	
Symbol	**Min**	**Max**
A	-	0.048
A_2	0.037	0.042
b	0.006	0.011
D	0.720	0.729
E	0.307	0.323
e	0.050 BSC	
H_D	0.779	0.796

TSOP THIN SMALL OUTLINE PACKAGE (8 x 20 mm)



Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGES



REVISIONS

DOCUMENT NUMBER: SRAM125 **DOCUMENT TITLE**: P4C1024L LOW POWER 128K x 8 CMOS STATIC RAM			
REV.	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
OR	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid
B	Feb-06	JDB	Added TSOP package
C	Sep-06	JDB	Added Ceramic DIP package