

[Document Title](#)

**256K x8 bit Low Power and Low Voltage Full CMOS Static RAM**

[Revision History](#)

<b>Revision No.</b>	<b>History</b>	<b>Draft Date</b>	<b>Remark</b>
0.0	Initial Draft	June 7, 2007	
0.1	0.1 Revision Remove BYTE option information	June 15, 2007	
0.2	0.2 Revision Remove $\overline{UB}$ , $\overline{LB}$ information	June 21, 2007	
0.3	0.3 Revision Revised V <sub>OH</sub> (2.2v to 2.4v), t <sub>OH</sub> (15ns to 10ns), t <sub>OE</sub> -55(30ns to 25ns), t <sub>WP</sub> -55(45ns to 40ns), t <sub>WP</sub> -70(55ns to 50ns), t <sub>WHZ</sub> -70(25ns to 20ns), ICC(2mA to 3mA), ICC1(2mA to 3mA)	July 2, 2007	
0.4	0.4 Revision V <sub>IH</sub> level change from 2.0V to 2.2V	Aug. 16, 2007	

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The attached data sheets are provided by EMLSI reserve the right to change the specifications and products. EMLSI will answer to your questions about device. If you have any questions, please contact the EMLSI office.

**256K x8 Bit Low Power and Low Voltage CMOS Static RAM**

**FEATURES**

- Process Technology : 0.15µm Full CMOS
- Organization :256K x8
- Power Supply Voltage  
=> EM620FV8B : 2.7~3.6V
- Low Data Retention Voltage : 1.5V
- Three state output and TTL Compatible
- Packaged product designed for 45/55/70ns

**GENERAL PHYSICAL SPECIFICATIONS**

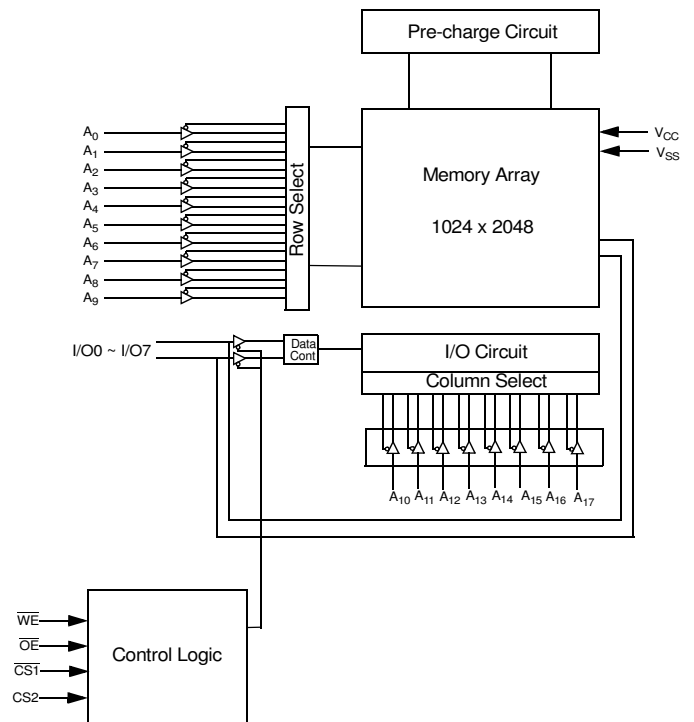
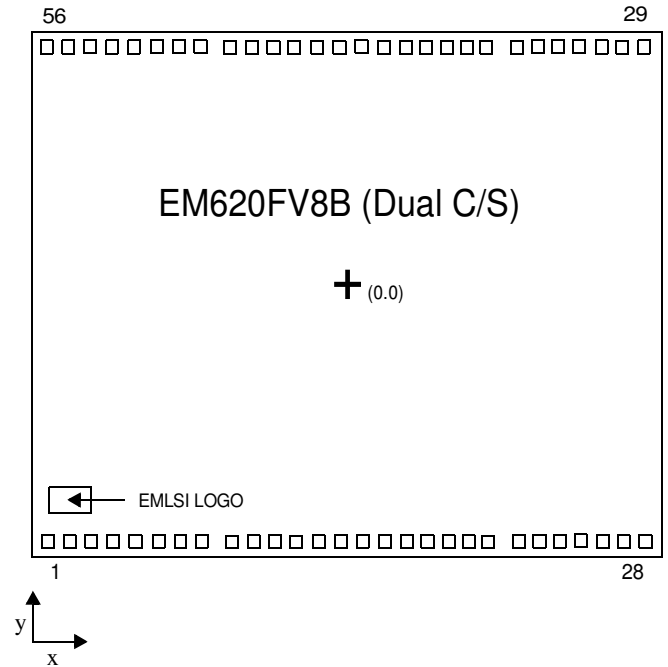
- Backside die surface of polished bare silicon
- Typical Die Thickness = 725um +/-15um
- Typical top-level metallization :  
=> Metal (Ti/AICu/TiN/ARC SiON/SiO2) : 5.2K Angstroms
- Topside Passivation :  
=> Passivation (HDP/pNIT/PIQ) : 5.4K Angstroms
- Wafer diameter : 8 inch

**OPTIONS**

- C1/W1 : DC Probed Die/Wafer @ Hot Temp
- C2/W2 : DC/AC Probed Die/Wafer @ Hot Temp

**PAD DESCRIPTIONS**

Name	Function	Name	Function
$\overline{CS1}, CS2$	Chip select inputs	Vcc	Power Supply
$\overline{OE}$	Output Enable input	Vss	Ground
$\overline{WE}$	Write Enable input	NC	No Connection
A0~A17	Address Inputs		
I/O0~I/O7	Data Inputs/Outputs		



**BONDING INSTRUCTIONS**

The 2M full CMOS SRAM die has total 56pads. Refer to the bond pad location and identification table for X, Y coordinates. EMLSI recommends using a bond wire on back side of die onto Vss bond pad for improved noise immunity.

## FUNCTIONAL SPECIFICATIONS

There are 3 classifications for EMLSI die and wafers products, which are C1 and C2 for die and W1 and W2 for wafer, respectively. Each die and wafer support dedicated characteristics and probe the electrical parameters within their specifications. Followings are brief information for die and wafer classifications. Please refer to packaged specifications for more information but these parameters are not guaranteed at bare die and wafer.

### – C1 LEVEL DIE OR W1 LEVEL WAFER

The DC parameters are measured by specification for C1 level die or W1 level wafer. The DC parameters measured at 70°C temperature, which called ‘Hot DC Sorting’ Other parameters are not guaranteed and warranted including device reliability. Please refer to qualification report for device reliability and package level datasheets for electrical parameters.

### – C2 LEVEL DIE OR W2 LEVEL WAFER

The DC parameters and selected AC parameters are measured with for C2 level die or W2 level wafer. The DC characteristics of C2 die and W2 wafer is tested based on DC specifications of C1 level die and W1 level wafer. The DC and specified AC parameters are tested at 70°C temperature, which called ‘Hot DC & Selective AC Sorting’. Other parameters are not guaranteed and warranted including device reliability. Please refer to qualification report for device reliability and package level datasheets for electrical parameters.

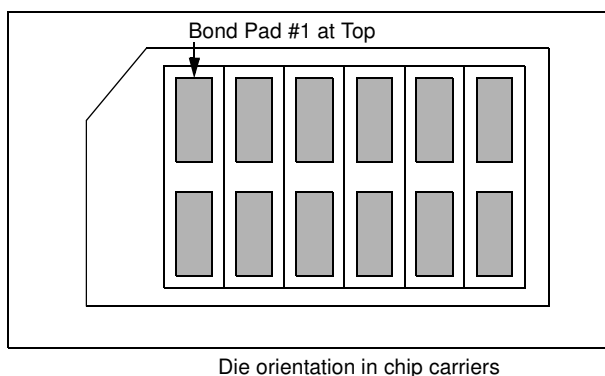
C2 level die and W2 level wafer probe following AC parameter.

- tRC, tAA, tCO
- tWC, tCW

## PACKAGING

Individual device will be packed in anti-static trays.

- Chip Trays : A 2-inch square waffle style carrier for die with separate compartments for each die. Commonly referred to as a waffle pack, each tray has a cavity size selected for the device that allows for easy loading and unloading and prevents rotation. The tray itself is made of conductive material to reduce the danger of damage to the die from electrostatic discharge. The chip carriers will be labeled with the following information :
  - EMLSI wafer lot number
  - EMLSI part number
  - Quantity
- Jar Packing : Jar packing is made by EMLSI and used by many customers that we deliver the requested die as wafer. The pack is consisted of clean paper to wrap the wafer, high cushioned sponge between wafers and hardly fragile plastic box with sponge. Each pack has typically 24 wafers and then several packs are put into larger box depending on amounts of wafers.



## STORAGE AND HANDLING

EMLSI recommends the die stored in a controlled environment with filtered nitrogen. The carrier must be opened at ESD safe environment when inspection and assembly.

**ABSOLUTE MAXIMUM RATINGS \***

Parameter	Symbol	Minimum	Unit
Voltage on Any Pin Relative to Vss	$V_{IN}, V_{OUT}$	-0.2 to 4.0V	V
Voltage on Vcc supply relative to Vss	$V_{CC}$	-0.2 to 4.0V	V
Power Dissipation	$P_D$	1.0	W
Operating Temperature	$T_A$	-40 to 85	°C

\* Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**FUNCTIONAL DESCRIPTION**

$\overline{CS1}$	$CS2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0-7</sub>	Mode	Power
H	X	X	X	High-Z	Deselected	Stand by
X	L	X	X	High-Z	Deselected	Stand by
X	X	X	X	High-Z	Deselected	Stand by
L	H	H	H	High-Z	Output Disabled	Active
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Data Out	Read	Active
L	H	X	L	Data In	Write	Active

Note: X means don't care. (Must be low or high state)

## RECOMMENDED DC OPERATING CONDITIONS <sup>1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	2.7	3.3	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.2	-	$V_{CC} + 0.2^{2)}$	V
Input low voltage	$V_{IL}$	$-0.2^{3)}$	-	0.6	V

1.  $T_A = -40$  to  $85^\circ\text{C}$ , otherwise specified
2. Overshoot:  $V_{CC} + 2.0$  V in case of pulse width  $\leq 20$ ns
3. Undershoot:  $-2.0$  V in case of pulse width  $\leq 20$ ns
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE <sup>1)</sup> ( $f = 1\text{MHz}$ , $T_A = 25^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	-	8	pF
Input/Output capacitance	$C_{IO}$	$V_{IO} = 0\text{V}$	-	10	pF

1. Capacitance is sampled, not 100% tested.

## DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit			
Input leakage current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$			
Output leakage current	$I_{LO}$	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{IO} = V_{SS}$ to $V_{CC}$	-1	-	1	$\mu\text{A}$			
Operating power supply	$I_{CC}$	$I_{IO} = 0\text{mA}$ , $\overline{CS1} = V_{IL}$ , $CS2 = \overline{WE} = V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	-	-	3	mA			
Average operating current	$I_{CC1}$	Cycle time = $1\mu\text{s}$ , 100% duty, $I_{IO} = 0\text{mA}$ , $\overline{CS1} \leq 0.2\text{V}$ , $CS2 \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-	3	mA			
			$I_{CC2}$	Cycle time = Min, $I_{IO} = 0\text{mA}$ , 100% duty, $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , $V_{IN} = V_{IL}$ or $V_{IH}$	45ns	-	-	35	mA
					70ns	-	-	25	
Output low voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V			
Output high voltage	$V_{OH}$	$I_{OH} = -1.0\text{mA}$	2.4	-	-	V			
Standby Current (TTL)	$I_{SB}$	$\overline{CS1} = V_{IH}$ , $CS2 = V_{IL}$ , Other inputs = $V_{IH}$ or $V_{IL}$	-	-	0.3	mA			
Standby Current (CMOS)	$I_{SB1}$	$\overline{CS1} \geq V_{CC} - 0.2\text{V}$ , $CS2 \geq V_{CC} - 0.2\text{V}$ ( $\overline{CS}$ controlled) or $0\text{V} \leq CS2 \leq 0.2\text{V}$ ( $CS2$ controlled), Other inputs = $0 \sim V_{CC}$ (Typ. condition : $V_{CC} = 3.3\text{V}$ @ $25^\circ\text{C}$ ) (Max. condition : $V_{CC} = 3.6\text{V}$ @ $85^\circ\text{C}$ )	LF	-	1 <sup>1)</sup>	10	$\mu\text{A}$		

### NOTES

1. Typical values are measured at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$  and not 100% tested.

## AC OPERATING CONDITIONS

**Test Conditions** (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.4 to 2.2V

Input Rise and Fall Time : 5ns

Input and Output reference Voltage : 1.5V

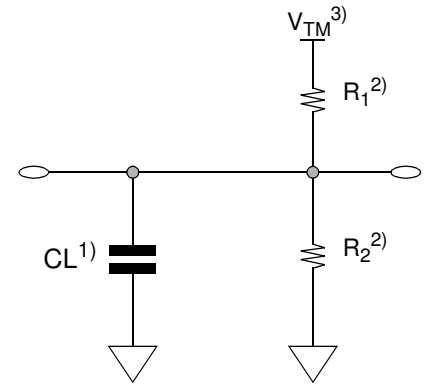
Output Load (See right) :  $CL^{(1)} = 100\text{pF} + 1 \text{ TTL}$

$CL^{(1)} = 30\text{pF} + 1 \text{ TTL}$  (only 45ns part)

1. Including scope and Jig capacitance

2.  $R_1=3070 \text{ ohm}$ ,  $R_2=3150 \text{ ohm}$

3.  $V_{TM}=2.8\text{V}$



**READ CYCLE** ( $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ ,  $Gnd = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

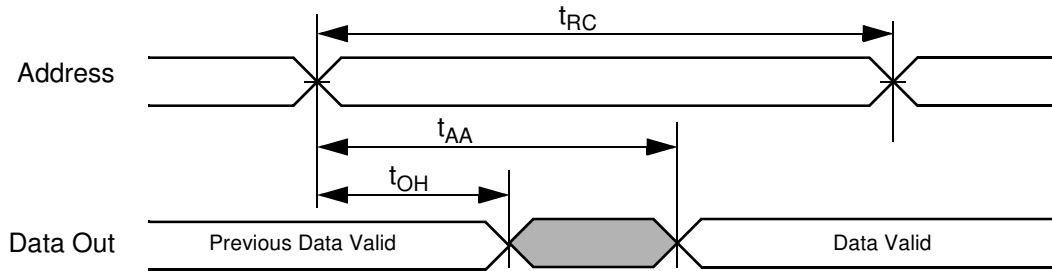
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	45	-	55	-	70	-	ns
Address access time	$t_{AA}$	-	45	-	55	-	70	ns
Chip select to output	$t_{CO1}, t_{CO2}$	-	45	-	55	-	70	ns
Output enable to valid output	$t_{OE}$	-	25	-	25	-	35	ns
Chip select to low-Z output	$t_{LZ1}, t_{LZ2}$	10	-	10	-	10	-	ns
Output enable to low-Z output	$t_{OLZ}$	5	-	5	-	5	-	ns
Chip disable to high-Z output	$t_{HZ1}, t_{HZ2}$	0	20	0	20	0	25	ns
Output disable to high-Z output	$t_{OHZ}$	0	15	0	20	0	25	ns
Output hold from address change	$t_{OH}$	10	-	10	-	10	-	ns

**WRITE CYCLE** ( $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ ,  $Gnd = 0\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

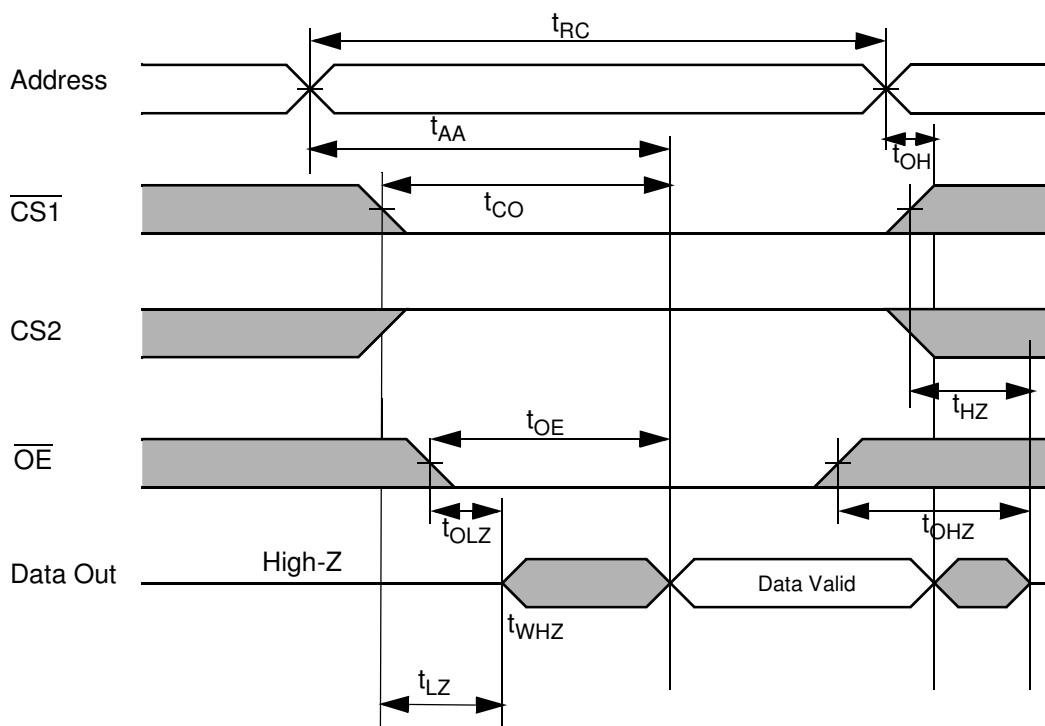
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	45	-	55	-	70	-	ns
Chip select to end of write	$t_{CW1}, t_{CW2}$	45	-	45	-	60	-	ns
Address setup time	$t_{AS}$	0	-	0	-	0	-	ns
Address valid to end of write	$t_{AW}$	45	-	45	-	60	-	ns
Write pulse width	$t_{WP}$	35	-	40	-	50	-	ns
Write recovery time	$t_{WR}$	0	-	0	-	0	-	ns
Write to output high-Z	$t_{WHZ}$	0	15	0	20	0	20	ns
Data to write time overlap	$t_{DW}$	25	-	25	-	30	-	ns
Data hold from write time	$t_{DH}$	0	-	0	-	0	-	ns
End write to output low-Z	$t_{OW}$	5	-	5	-	5	-	ns

## TIMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ )**



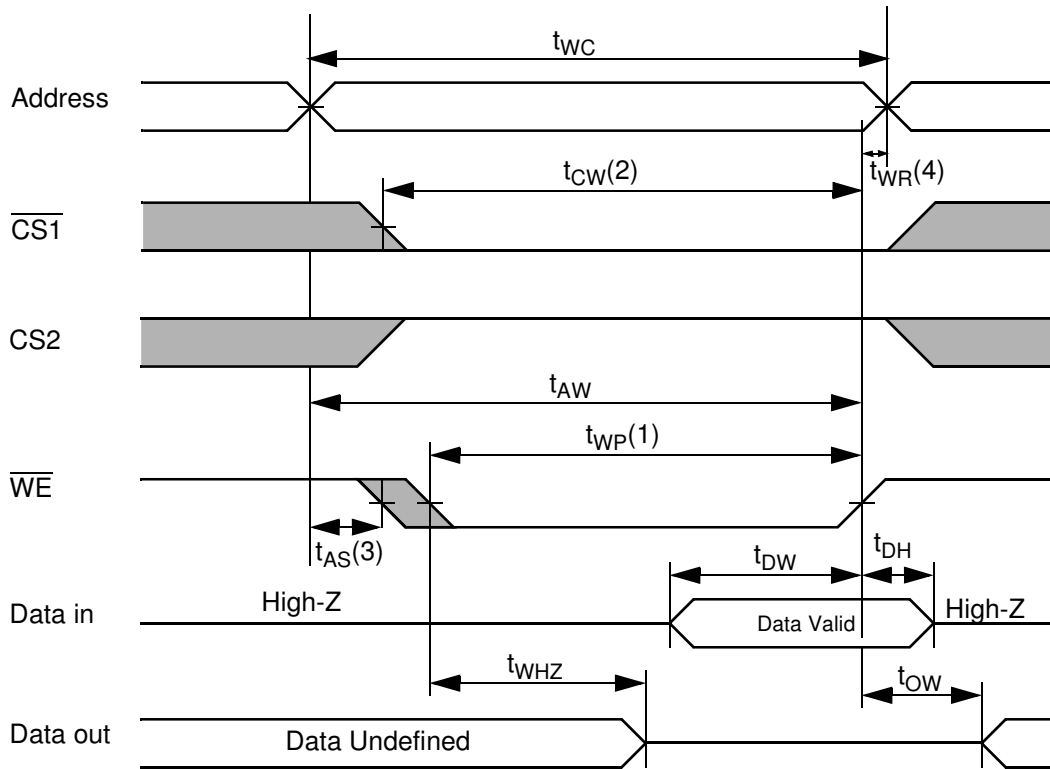
**TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE} = V_{IH}$ )**



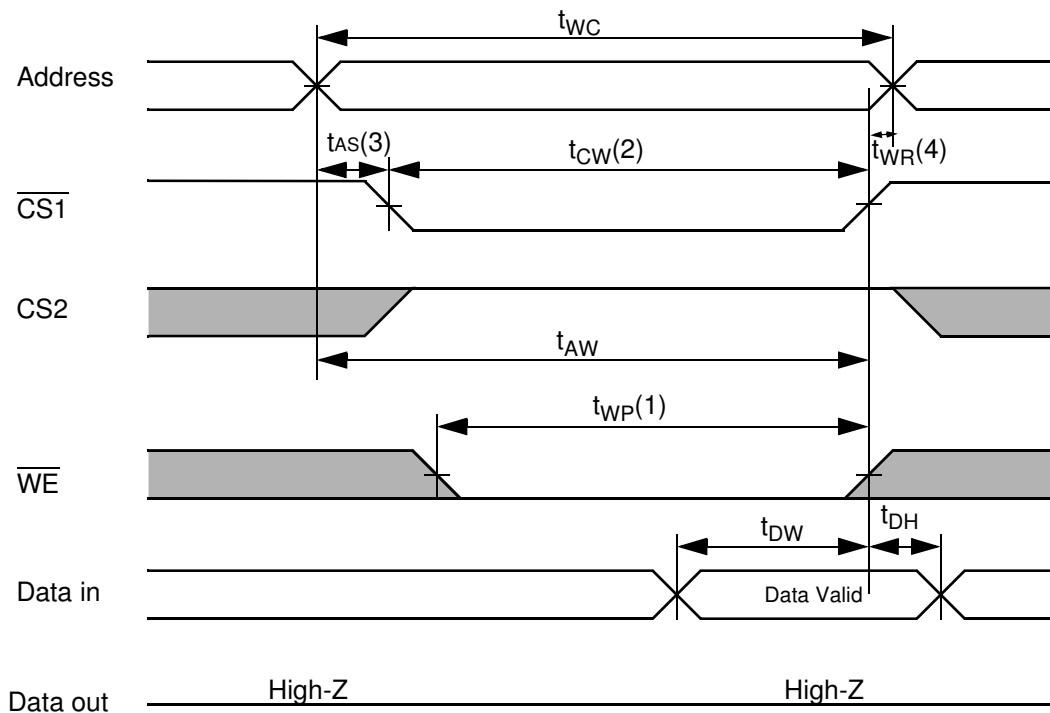
### NOTES (READ CYCLE)

- $t_{HZ}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
- At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  CONTROLLED)**

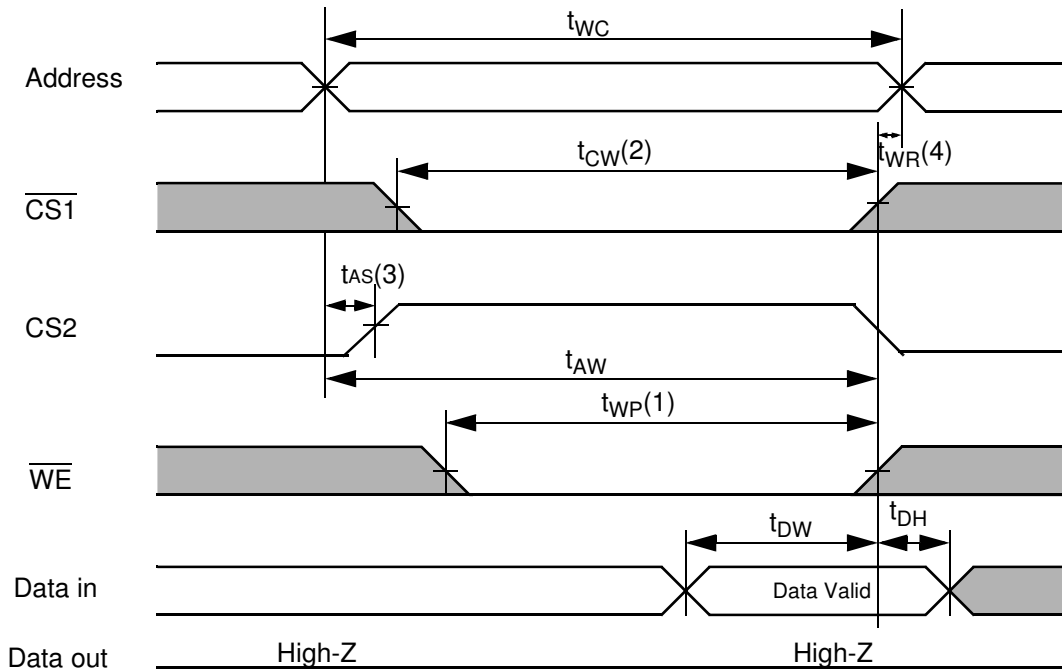


**TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  CONTROLLED)**





**TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 CONTROLLED)**



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap(t<sub>WP</sub>) of low  $\overline{CS1}$ , a high CS2 and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  goes low, CS2 goes high and  $\overline{WE}$  goes low. A write ends at the earliest transition when  $\overline{CS1}$  goes high, CS2 goes high and  $\overline{WE}$  goes high. The t<sub>WP</sub> is measured from the beginning of write to the end of write.
2. t<sub>CW</sub> is measured from the  $\overline{CS1}$  going low to end of write.
3. t<sub>AS</sub> is measured from the address valid to the beginning of write.
4. t<sub>WR</sub> is measured from the end of write to the address change. t<sub>WR</sub> applied in case a write ends as  $\overline{CS1}$  or  $\overline{WE}$  going high.

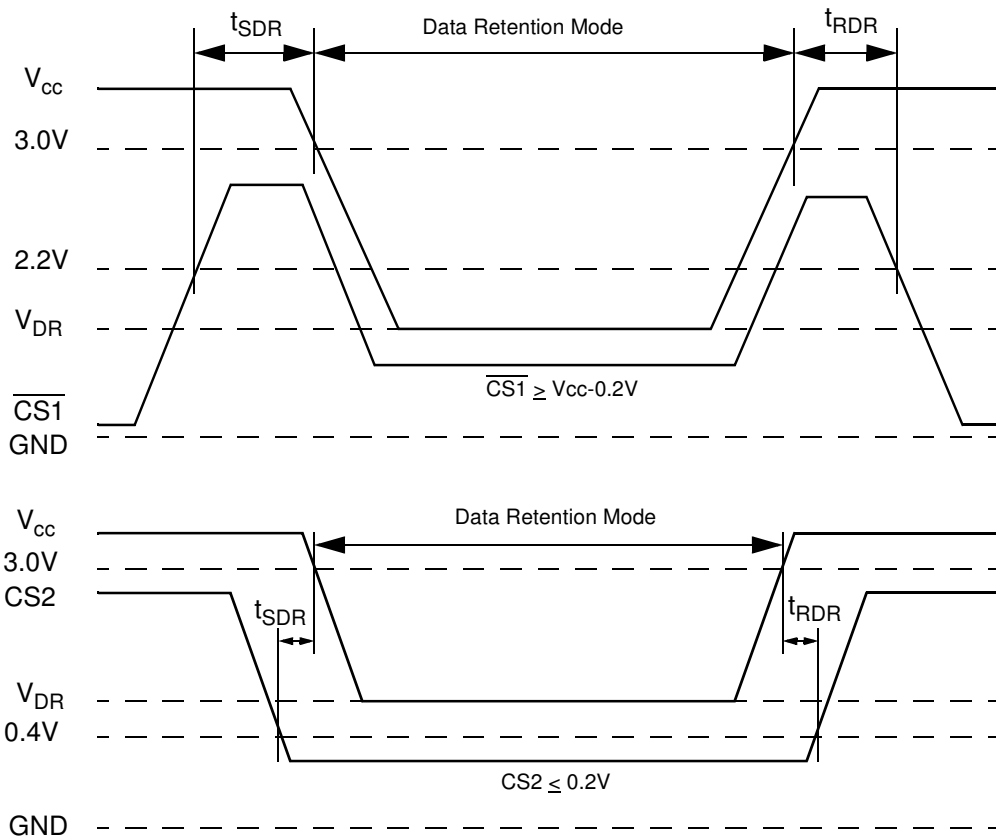
**DATA RETENTION CHARACTERISTICS**

Parameter	Symbol	Test Condition	Min	Typ <sup>2)</sup>	Max	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	1.5	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.5V, I <sub>SB1</sub> Test Condition (Chip Disabled) <sup>1)</sup>	-	0.5	-	μA
Chip Deselect to Data Retention Time	t <sub>SDR</sub>	See data retention wave form	0	-	-	ns
Operation Recovery Time	t <sub>RDR</sub>		t <sub>RC</sub>	-	-	

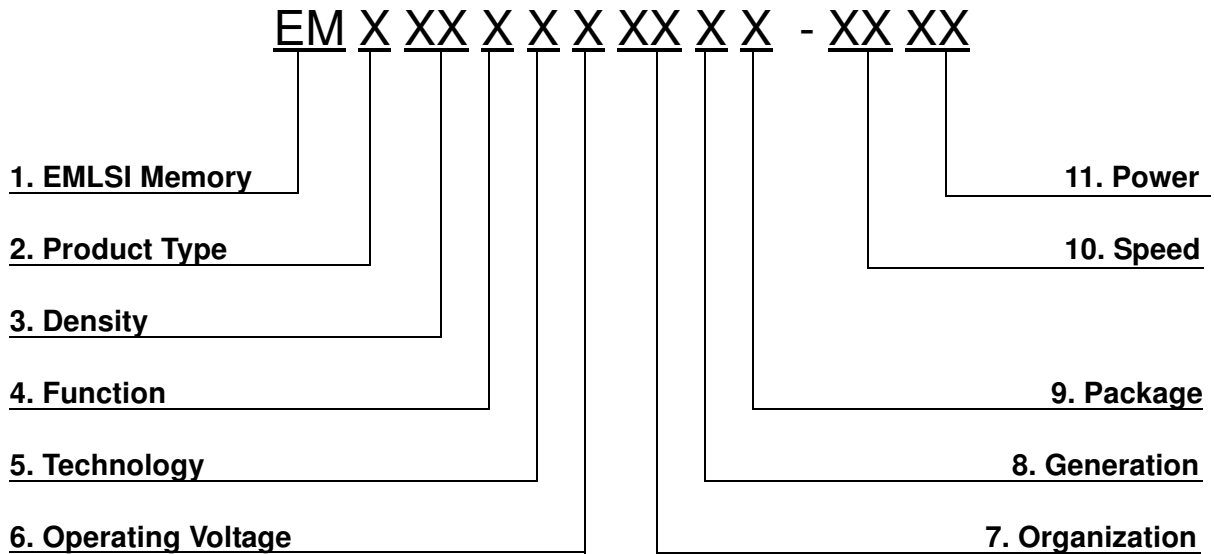
**NOTES**

1. See the I<sub>SB1</sub> measurement condition of data sheet page 5.
2. Typical value is measured at T<sub>A</sub>=25°C and not 100% tested.

**DATA RETENTION WAVE FORM**



**SRAM PART CODING SYSTEM**



**1. Memory Component**  
EM ----- Memory

**2. Product Type**  
6 ----- SRAM

**3. Density**  
1 ----- 1M  
2 ----- 2M  
4 ----- 4M  
8 ----- 8M

**4. Function**  
0 ----- Dual CS  
1 ----- Single CS  
2 ----- Multiplexed  
3 ----- Single CS / LBB, UBB(tBA=tOE)  
4 ----- Single CS / LBB, UBB(tBA=tCO)  
5 ----- Dual CS / LBB, UBB(tBA=tOE)  
6 ----- Dual CS / LBB, UBB(tBA=tCO)

**5. Technology**  
F ----- Full CMOS

**6. Operating Voltage**  
T ----- 5.0V  
V ----- 3.3V  
U ----- 3.0V  
S ----- 2.5V  
R ----- 2.0V  
P ----- 1.8V

**7. Organization**  
8 ----- x8 bit  
16 ----- x16 bit

**8. Generation**  
Blank ----- 1st generation  
A ----- 2nd generation  
B ----- 3rd generation  
C ----- 4th generation  
D ----- 5th generation  
E ----- 6th generation  
F ----- 7th generation  
G ----- 8th generation

**9. Package**  
Blank ----- KGD, 48&36FpBGA  
S ----- 32sTSOP1  
T ----- 32 TSOP1  
U ----- 44 TSOP2

**10. Speed**  
45 ----- 45ns  
55 ----- 55ns  
70 ----- 70ns  
85 ----- 85ns  
10 ----- 100ns  
12 ----- 120ns

**11. Power**  
LL ----- Low Low Power  
LF ----- Low Low Power(Pb-Free & Green)  
L ----- Low Power  
S ----- Standard Power