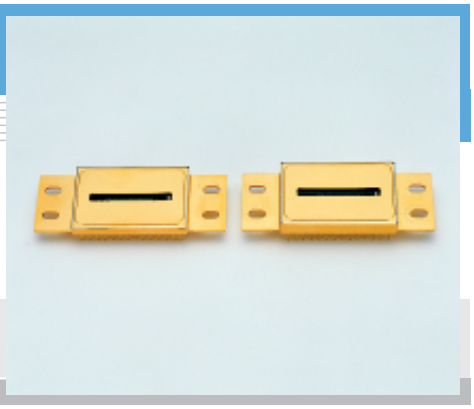


InGaAs linear image sensor
G9201 to G9204 series

Image sensor for DWDM wavelength monitor

G9201 to G9204 series InGaAs linear image sensors are specifically designed as detectors for monitoring WDM in optical communications. These linear image sensors consist of an InGaAs photodiode array with each pixel connected to a charge amplifier array comprised of CMOS transistors, a CDS circuit, an offset compensation circuit, a shift register and a timing generator. These sensors deliver high sensitivity and stable operation in the near infrared spectral range. The package is hermetically sealed for high reliability and the window has an anti-reflective coating for efficient light detection.
Signal processing circuits on the CMOS chip allow selecting a feedback capacitance (Cf) of 10 pF or 0.5 pF by supplying an external voltage. The image sensor operates over a wide dynamic range when Cf=10 pF and delivers high gain when Cf=0.5 pF.

Features

- Wide dynamic range
- Low noise and low dark current
- Selectable gain
- Anti-saturation circuit
- CDS circuit *1
- Offset compensation circuit
- Simple operation (by built-in timing generator) *2
- High resolution: 25 µm pitch (512 ch)
- Low cross-talk
- 256 ch: 1 video line
  512 ch: 2 video lines

Applications

- DWDM wavelength monitor
- Optical spectrum analyzer

Accessories (Optional)

- InGaAs multichannel detector head C8061-01 *3
- Multichannel detector head controller C7557 *3

■ Selection guide

Type No.	Cooling	Number of pixels	Pixel pitch (µm)	Pixel size [µm (H) × µm (V)]	Spectral response range (µm)	Defective pixel
G9201-256S	One-stage TE-cooled	256	50	50 × 250	0.9 to 1.67 (-10 °C)	0
G9202-512S	One-stage TE-cooled	512	25	25 × 250	0.9 to 1.67 (-10 °C)	
G9203-256D *4	Non-cooled	256	50	50 × 500	0.9 to 1.7 (25 °C)	
G9203-256S	One-stage TE-cooled				0.9 to 1.67 (-10 °C)	
G9204-512D *4	Non-cooled	512	25	25 × 500	0.9 to 1.7 (25 °C)	
G9204-512S	One-stage TE-cooled				0.9 to 1.67 (-10 °C)	

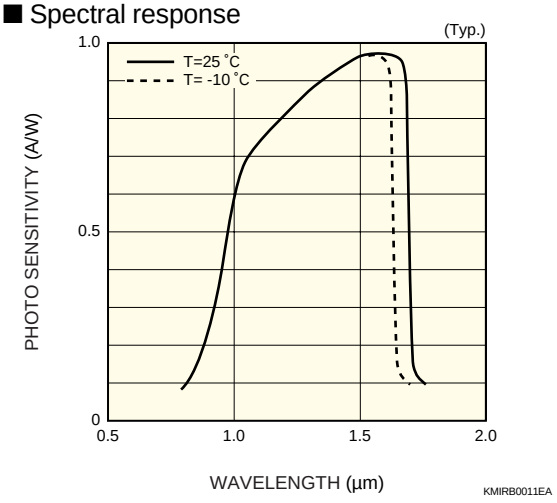
*1: CDS (Correlated Double Sampling) circuit
A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.

*2: Timing generator
Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (Programmable Logic Devices) are used to input the required timing signals. However, G9201 to G9204 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

*3: G9203-256D and G9204-512D are not available for C7557.

*4: For G9203-256D and G9204-512D specifications, see the separate data sheets available from Hamamatsu.

■ Spectral response



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■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Clock pulse voltage	Vϕ	5.5	V
Operating temperature *5	Topr	-40 to +70	°C
Storage temperature *5	Tstg	-40 to +85	°C

*5: Non condensation

■ Electrical characteristics (Ta=25 °C, Vϕ=5 V)

Parameter		Symbol		Min.	Typ.	Max.	Unit
Supply voltage		Vdd		4.9	5.0	5.1	V
		Vref		-	1.26	-	
Supply current		I (Vdd)	256 ch	-	45	50	mA
			512 ch	-	90	100	
		I (Vref)		-	1 Max.	-	mA
Ground		Vss		-	0	-	V
Element bias		INP		3.5	4.5	4.6	V
Element bias current		I (INP)		-	1 Max.	-	mA
Clock frequency		f		0.1	-	4	MHz
Clock pulse voltage	high	Vϕ		Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	low			0	0	0.4	V
Clock pulse rise/fall times		tr ϕ		0	20	100	ns
		tf ϕ					
Clock pulse width		tpw ϕ		200	-	-	ns
Reset pulse voltage	high	V (RES)		Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	low			0	0	0.4	V
Reset pulse rise/fall times		tr (RES)		0	20	100	ns
		tf (RES)					
Reset pulse width		tpw (RES)		6000	-	-	ns
Video output voltage	high	V_H		-	4.5	-	V
	low	V_L		0	1.26	-	
Data rate		fv		-	f/8	-	Hz

■ Electrical and optical characteristics
General ratings (T=25 °C)

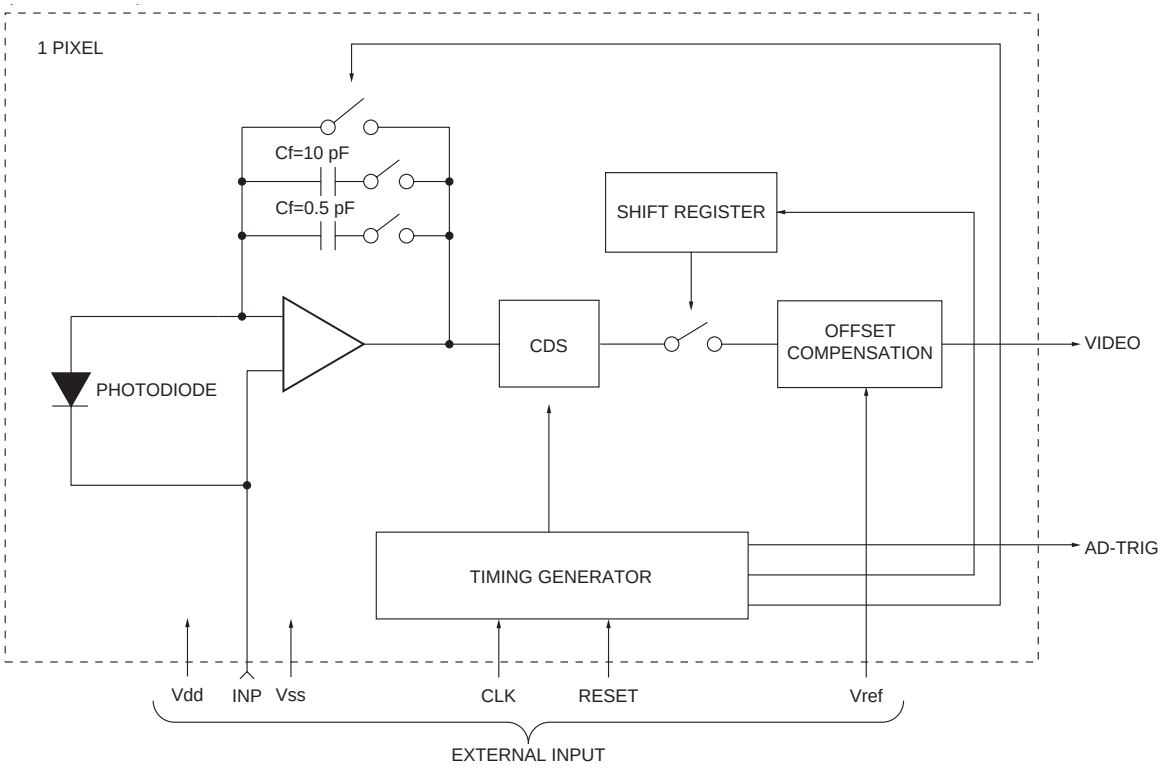
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Peak sensitivity wavelength	λp		-	1.55	-	μm
Saturation charge *6	Qsat	Vp=5 V	-	30	-	pC
RMS noise voltage (readout noise)	N	Standard deviation Number of integration: 50	-	180	300	μVrms
Photo response non-uniformity *7	PRNU	Integration time: 10 msec	-	-	±5	%
Saturation voltage	Vsat		3.0	3.2	-	V

*6: Vϕ=5 V, Cf=10 pF
*7: 50 % of saturation, 10 ms integration time, after dark output subtraction, excluding first and last pixels.

Dark current characteristics (T=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
G9201 series	I_D	-	2	10	pA
G9202 series		-	1	5	
G9203 series		-	4	20	
G9204 series		-	1	5	

■ Equivalent circuit



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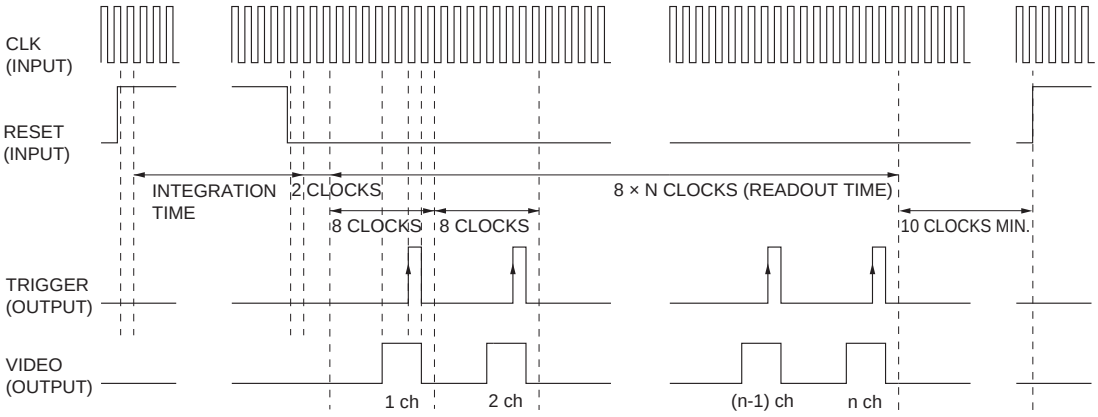
■ Timing chart



■ Basic circuit connection

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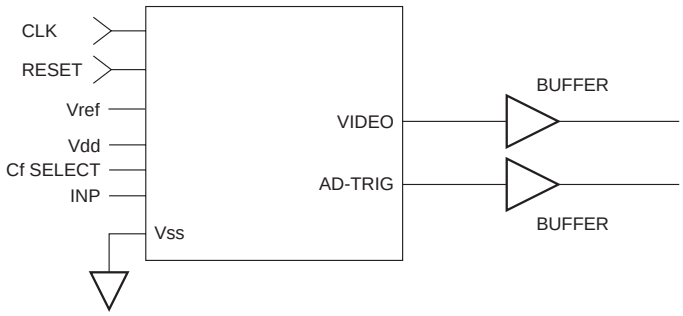

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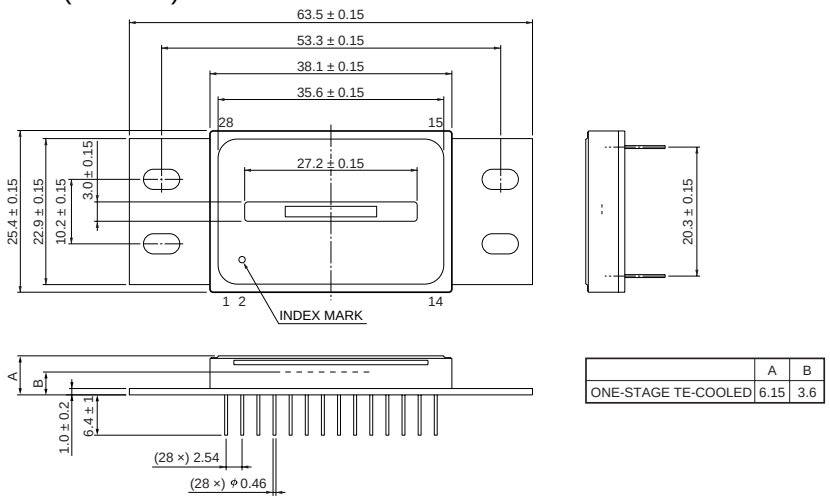
■ Dimensional outline (unit: mm)



	A	B
ONE-STAGE TE-COOLED	6.15	3.6

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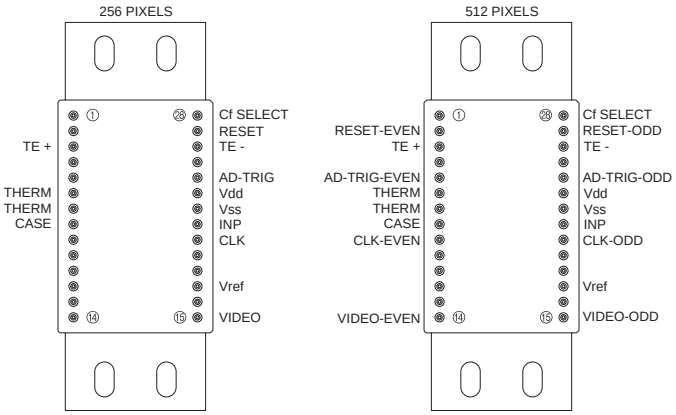
■ Pin connection (top view)



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Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse is integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip.
Vss	-	Ground for the signal processing circuit on the CMOS chip.
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip.
Cf SELECT	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip. Cf=10 pF at 0 V, and Cf=0.5 pF at 5 V.
CASE	-	This terminal is electrically connected to the package.
THERM	-	Thermistor for monitoring temperature inside the package. No connection for room temperature operation type.
TE+, TE-	-	Power supply terminal for the thermoelectric cooler that cools the photodiode array.
AD-TRIG	Output	Digital signal for AD conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit on the CMOS chip

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