Applying the DLX3416* Intelligent Display® Device Appnote 17

This application note is intended to serve as a design and application guide for users of the DLX3416 (referred to as 3416 hereafter) alphanumeric Intelligent Displays. This appnote also covers device electrical description and operation, considerations for general circuit design, and interfacing the 3416 to microprocessors. Refer to the specific data sheet and other Infineon / OSRAM Appnotes for more details.

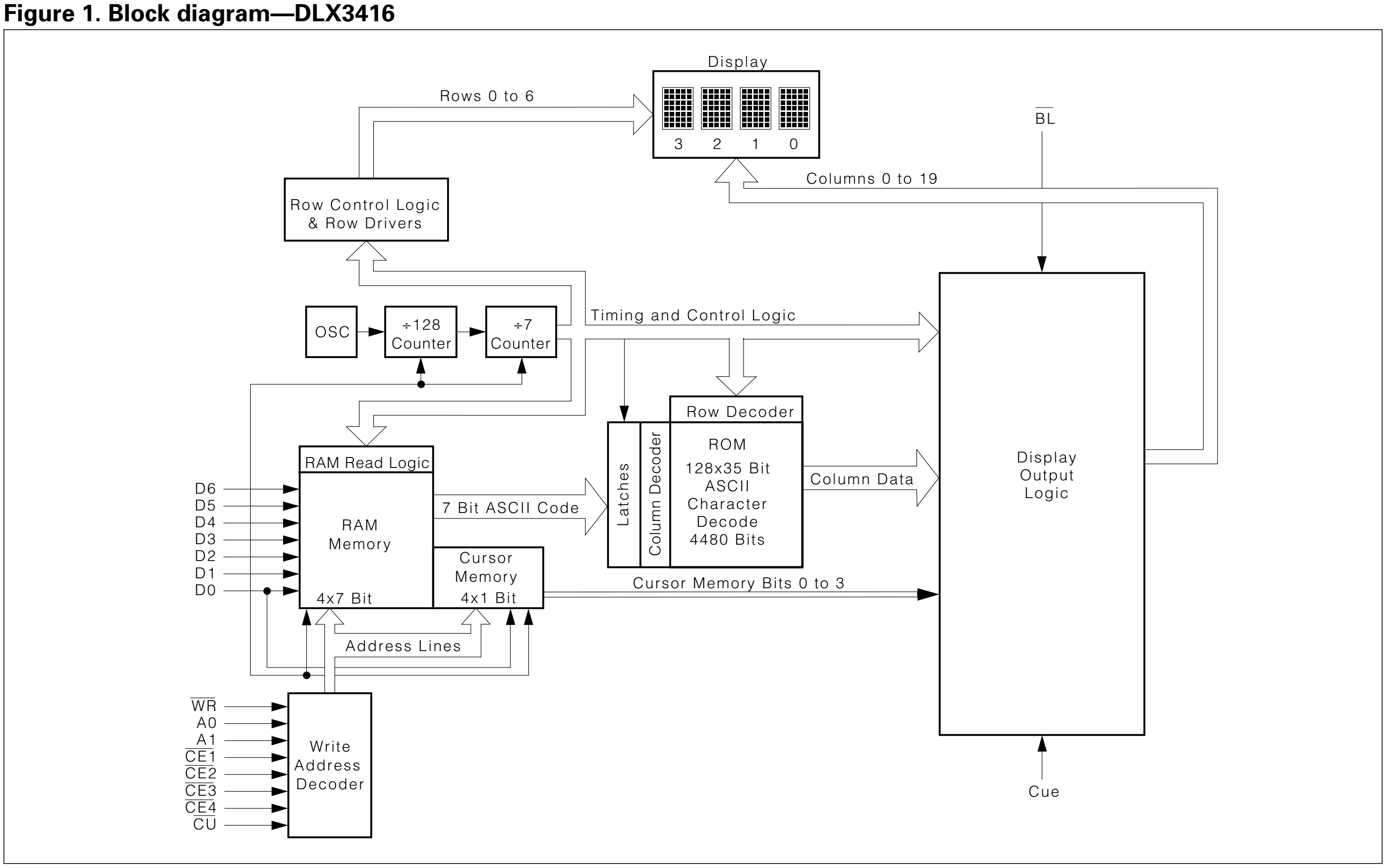
Electrical & Mechanical Description

The internal electronics in these Intelligent Displays eliminates all the traditional difficulties of using multi-digit light emitting displays (segment decoding, drivers, and multiplexing).

An Intelligent Display also provides internal memory for the four digits. This approach allows the user to asynchronously address one of four digits, and load new data without regard to the LED multiplex timing.

Figure 1 is a block diagram of the DLX3416. The unit consists of four (5x7) LED arrays and a single CMOS integrated chip. The IC chip contains the column and row drivers, 128 character ROM, four word x7 bit Random Access Memory, oscillator for multiplexing, multiplex counter/decoder, cursor memory, address decoder, and miscellaneous control logic.

Figure 1. Block diagram—DLX3416



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Packaging

Packaging consists of a transfer molded nylon lens which also serves as an “encapsulation shell” since it covers five of the six “faces.” The assembled and tested substrate (“PTF” multi-layer), is placed within the shell and the entire assembly is then filled with a water clear IC grade epoxy.

This yields a very rugged part, which is quite impervious to moisture, shock and vibration. Although not “hermetic,” the device will easily withstand total immersion in water/detergent solutions.

Figure 2. Top view

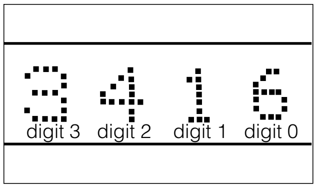


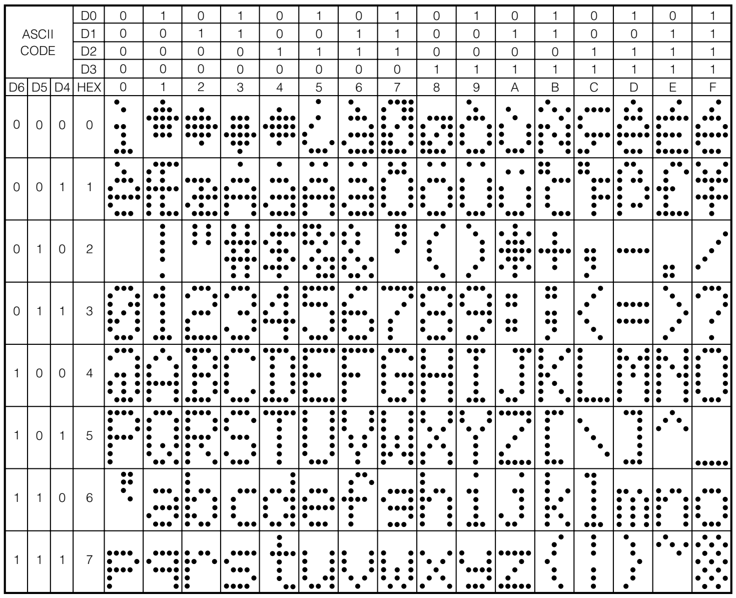
Table 1. Pin outs

Pin	Function	Pin	Function
1	$\overline{CE1}$ Chip Enable	10	GND
2	$\overline{CE2}$ Chip Enable	11	D0 Data Input
3	$\overline{CLR}$ Clear	12	D1 Data Input
4	CUE Cursor Enable	13	D2 Data Input
5	$\overline{CU}$ Cursor Select	14	D3 Data Input
6	$\overline{WR}$ Write	15	D6 Data Input
7	A1 Digit Select	16	D5 Data Input
8	A0 Digit Select	17	D4 Data Input
9	V_{CC}	18	$\overline{BL}$ Display Blank

Table 2. Electrical inputs to the 3416

V_{CC}	Positive supply +5 volts
GND	Ground
D0-D6	Data Lines The seven data input lines are designed to accept the first 64 ASCII characters. See Figure 3 for DL3416 character set (The DL3416 interprets all undefined codes as a blank). See Figure 3 for DLX3416 character set.
A0, A1	Address Lines The address determines the digit position to which the data will be written. Address order is right to left for positive-true logic.
$\overline{WR}$	Write (Active Low) Data and address to be loaded must be present and stable before and after the trailing edge of write. (See DL3416, DLX3416 data sheets for timing information).
$\overline{CE1}$, $\overline{CE2}$	Chip Enable (Active High)
$\overline{CE3}$, $\overline{CE4}$	Chip Enable (Active Low) Determines which device in an array will actually accept data. When either or both chip enable is in the high state, all inputs are inhibited.
$\overline{CLR}$	Clear (Active Low) The data RAM and cursor RAM of the DL 3416 will be cleared when held low for 15 mS. The minimum for the $\overline{CLR}$ is 1 mS for the DLX3416.
CUE	Cursor Enable Activates Cursor function. Cursor will not be displayed regardless of cursor memory contents when cue is Low.
$\overline{CU}$	Cursor Select (Active Low) This input must be held high to store data in data memory and low to store data into the cursor memory.
$\overline{BL}$	Display Blank (Active Low) Blanking the entire display may be accomplished by holding the $\overline{BL}$ input low—not a stored function. When $\overline{BL}$ is released, the stored characters are again displayed. $\overline{BL}$ can be used for flashing or dimming.

Figure 3. Character set—DLX3416



Notes: 1. High = 1 level.
2. Low = 0 level.
3. Upon power up, the device will initialize in a random state.

Clear Memory

Clearing of the entire internal four digit memory may be accomplished by holding the clear line ($\overline{CLR}$) low for one complete internal display multiplex cycle, 15 mS minimum for DL 3416, 1 mS for DLX3416. Less time may leave some data uncleared. $\overline{CLR}$ also clears the cursor memory.

Display Blanking

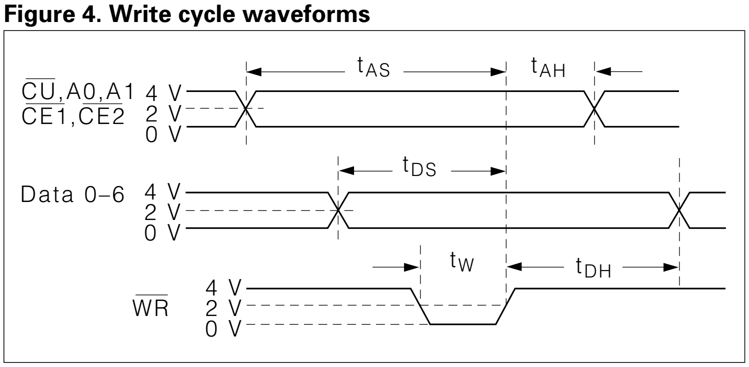
Blanking the display may be accomplished by loading a blank, space or illegal code into each digit of the display or by using the ($\overline{BL}$) display blank input. Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$).

Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, i.e., synchronize before a Write can be done. This can be slow and cumbersome.

Data entry in Intelligent Displays is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

Figure 4. Write cycle waveforms



The waveforms of Figure 4 demonstrate the relationships of the signals required to generate a write cycle. (Check individual data sheet for minimum values). As can be seen from the waveforms, all signals are referenced from the rising or trailing edge of write.

Cursor

The DLX3416 cursor function causes all dots to light at 50% brightness. The cursor can be used to indicate the position in the display of the next character to be entered. The cursor is not a character but overrides the display of a stored character. Upon removal of the cursor, the display will again show the character stored in memory.

The cursor can be written into any digit position by setting the cursor enable (CUE) high, setting the digit address (A1, A0), enabling Chip Enable, ($\overline{CE1}$, $\overline{CE2}$), cursor select ($\overline{CU}$), Write ($\overline{WR}$) and Data (D0). A high on data line D0 will place a cursor into the position set by the address A0 and A1. Conversely, a low on D0 will remove the cursor. The cursor will remain displayed after the cursor ($\overline{CU}$) and write ($\overline{WR}$) signals have been removed. During the cursor-write sequence, data lines D1 through D6 are ignored by the 3416.

If the user does not wish to utilize the cursor function, the cursor enable (CUE) can be tied low to disable the cursor function. A flashing cursor can be realized by simply pulsing the CUE line after cursor data has been stored.

General Design Considerations

Using Positive true logic, address order is from right to left. For left to right address order, use the "ones complement" or simple inversion of the addresses.

For systems with only a 6 bit (abbreviated ASCII) code format, Data Line D6 cannot be left open. Data D6 must be the complement of Data Line D5.

A "display test" or "lamp test" function can be achieved by simply storing a cursor into all digits.

Because of the random state of the cursor RAM after power up, if the cursor function is to be used, it will be necessary to clear cursors initially to assure that all cursor memories contain its zero state. This is easily accomplished with the $\overline{CLR}$ input.

When using the 3416 on a separate display board having more than 6 inches of cable length, it may be necessary to buffer all inputs. This is most easily achieved with Hex non-inverting buffers such as the 74365. The object is to prevent transient current in the protection diodes. The buffers should be located on the display board near the displays.

Local power supply bypass capacitors are also needed in many cases. These should be 6 or 10 volt, tantalum type with 10 µF or greater capacitance. Low internal resistance is important due to current steps which result from the internal multiplexing of the displays.

If small wire cables are used, it is good engineering practice to calculate the wire resistance of the ground plus the +5 volt wires. More than 0.1 volt drop, (at 25 mA per digit worst cast) should be avoided, since this loss is in addition to any inaccuracies or load regulation limitations of the power supply.

The 5 volt power supply for the displays should be the same one supplying V_{CC} to all logic devices which drive the display devices. If a separate supply must be used, then local buffers using hex non-inverting gates should be used on all inputs and these buffers should be powered from the display power supply. This precaution is to avoid logic inputs higher than display V_{CC} during power up or line transients.

Figure 5.

Loading Data

$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A_1	A_0	D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
L	X	X	X	H	X	H	X	X	X	X	X	X	X	X	X	Blank			
H	H	X	L	H	X	H	X	X	X	X	X	X	X	X	X	Previous Characters			
H	X	H	L	H	X	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	X	X	L	H	H	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	L	L	L	H	L	H	L	L	H	L	L	L	L	L	H	NC	NC	NC	A
H	L	L	L	H	L	H	L	H	H	L	L	L	L	H	L	NC	NC	B	A
H	L	L	L	H	L	H	H	L	H	L	L	L	L	H	H	NC	C	B	NC
H	L	L	L	H	L	H	H	H	H	L	L	L	H	L	L	D	C	NC	A
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	D	C	B	E
H	L	L	L	H	L	H	H	L	H	L	L	H	L	H	H	D	K	B	E
H	L	L	L	H	L	H	–	–	–	–	–	–	–	–	–	See Character Set			

Loading Cursor

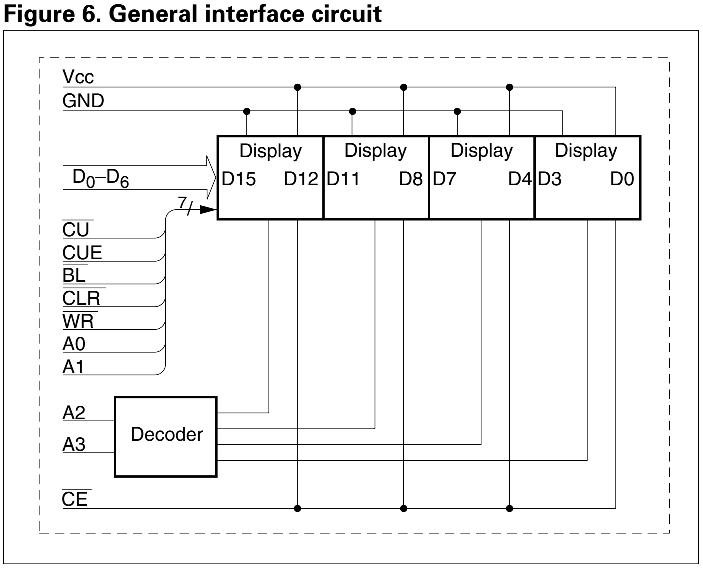
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A_1	A_0	D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
H	L	L	L	H	X	H	X	X	X	X	X	X	X	X	X	Normal Data Entry			
H	L	L	H	H	H	H	X	X	X	X	X	X	X	X	X	Enable Previous Stored Cursors			
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	NC	NC	NC	■
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	NC	NC	■	■
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	NC	■	■	■
H	L	L	H	L	L	H	H	H	X	X	X	X	X	X	H	■	■	■	■
H	L	L	L	H	H	H	X	X	X	X	X	X	X	X	X	D	K	B	E
H	L	L	L	L	L	H	L	L	X	X	X	X	X	X	L	D	K	B	E
H	L	L	H	H	H	H	X	X	X	X	X	X	X	X	X	■	■	■	E

X = Don't care
NC = No change from previously displayed characters
■ = all dots/segments on at half brightness

Interfacing the 3416

A general and straightforward interface circuit is shown in Figure 6. This scheme can easily interface to µP systems or any other systems which can provide the seven data lines, appropriate address, and control lines.

Figure 6. General interface circuit



Parallel I/O

The parallel I/O device of a microprocessor can easily be connected to the circuit in Figure 6. One eight bit output port can provide the seven input data bits and the cursor (CU). Another eight bit output port can contain the address and chip enable information and the other control signals.

INIT:	MVI A,80H OUT CONTROL	;CONTROL DATA MODE 0 ;LOAD CONTROL REGISTER
CUSR:	MVI A,00H OUT PORT A MVI B, 0FH	;CLEAR CURSOR DATA ;LOAD DATA PORT ;SET CHARACTER COUNTER
CUSRI	:MOV A, B CALL DSPWT DCR B JNZ CUSRI MOV A, B CALL DSPWT MVI A, FFH OUT PORT B	; ;WRITE SUBROUTINE ;DECREMENT COUNTER ;DIGIT 0? ; ; ;SET DATA FOR CONTROL ;LOAD CONTROL LINES
DISP:	LXI H, TABLE	;SET TABLE ADDRESS

DISP1	MOV A, M
	
	OUT PORT A
	MOV A, B
	CALL DSPWT
	
	INX H
	
	INR B
	MVI A, 10H
	CMP B
	JNZ DISP1
	HALT
		;MOVE TABLE DATA INTO ACCUMULATOR
		;LOAD DATA PORT
		;
		;LOAD ADDRESS AND CONTROL
		;INCREMENT TABLE ADDRESS
		;INCREMENT COUNTER SET # OF DIGITS
		;
		;16 CHARACTERS?
		;END OF PROGRAM

DSPWT	:ORI F0H OUT PORT C ANI 7FH OUT PORT C ORI F0H OUT PORT C RET	;SET CONTROL BITS OFF ;LOAD CONTROL ;SET WRITE BIT ON ;LOAD WRITE ORI F0H ;LOAD CONTROL
TABLE:	DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB	;0C3H ;0C9H ;0D4H ;0D3H ;0C1H ;0D4H ;0CEH ;0C1H ;0C6H ;0A0H ;0D3H ;0D4H ;0C8H ;0C7H ;0C9H ;0CCH

Figure 7. 16-digit parallel I/O system

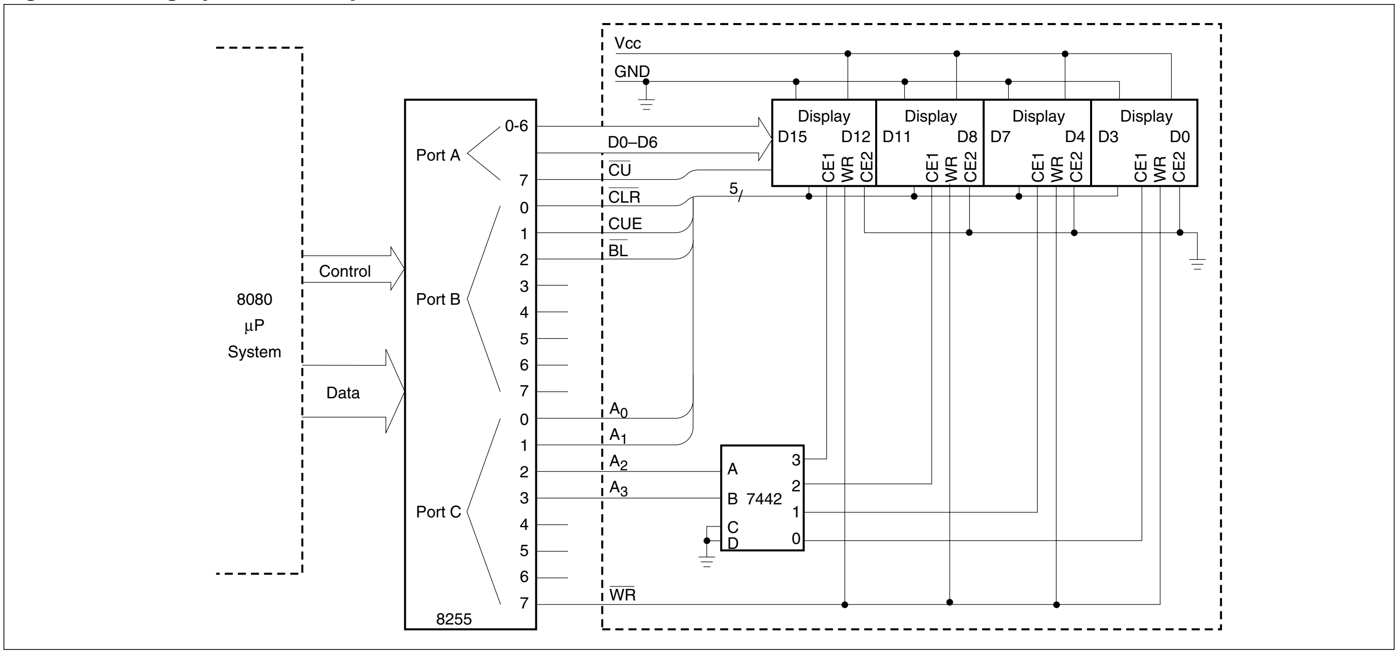


Figure 8. Mapped interface.

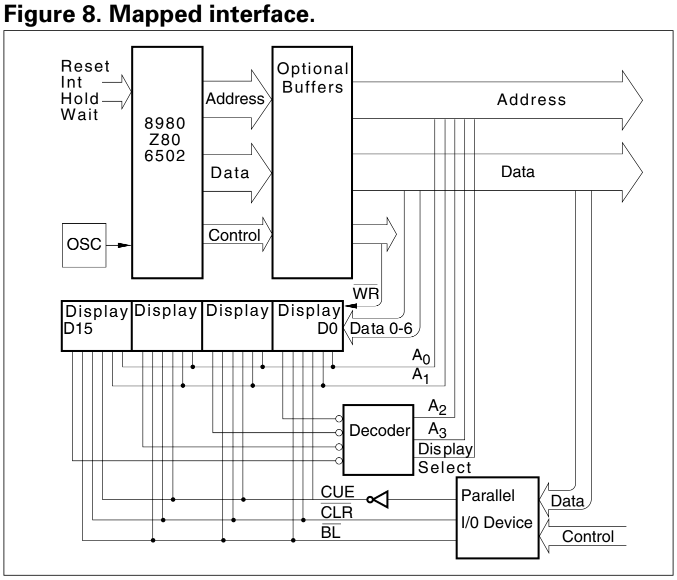


Figure 9. Interface with 6800 microprocessor

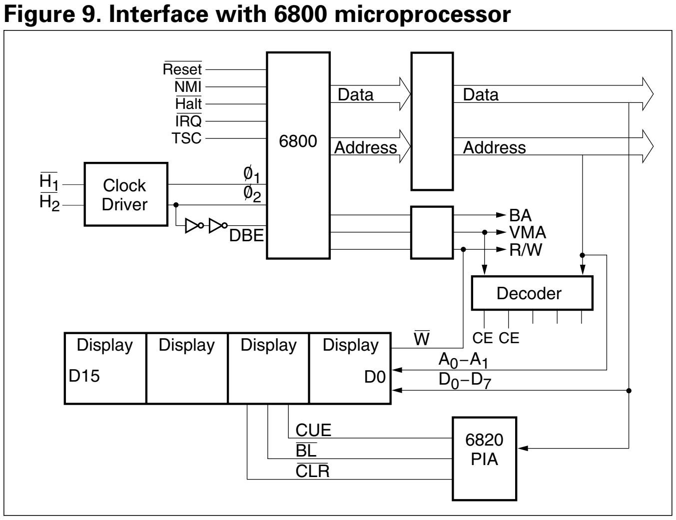


Figure 7 illustrates a 16 character display with an 8080 system using the 8255 programmable peripheral interface I/O device. The following program will display a simple 16 character message using this interface.

I/O or Memory Mapped Addressing

Some designers may wish to avoid the additional cost of a parallel I/O in their system. Structuring the addressing architecture for the 3416 to look like a set of peripheral or output devices (I/O mapped) or RAM's and ROM's (memory mapped) is very easy. Figure 8 shows the simplicity of interfacing to microprocessors, such as 8080, Z80 and 6502 as examples.

The interface with the 6800 microprocessor in Figure 9 illustrates the need for designers to check the timing requirements of the 3416 and the µP. The typical data output hold time is only 30 ns for DBE=∅2 timing; two inverters in the DBE line are added to increase the data output hold time for compatibility with the 50 nS minimum specification of the 3416.

Conclusion

Note that although other manufacturers' products are used in examples, this application note does not imply specific endorsement, or recommendation or warranty of other manufacturer's products by Infineon / OSRAM.

The interface schemes shown demonstrate the simplicity of using the 3416 with microprocessors. The slight differences encountered with various microprocessors to interface with the 3416 are similar to those encountered when using different RAMs. The techniques used in the examples were shown for their generality, and any display of this family are interchangeable in these examples. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.