TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95CW64
TMP95CW65

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP95CW64F / TMP95CW65F

1. Outline and Features

TMP95CW64/W65 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment. TMP95CW64 incorporates masked ROM, while TMP95CW65 has no ROM. Otherwise, all the functions of the products are the same.
TMP95CW64/W65 comes in a 100-pin flat package.
Listed below are the features.

(1) High-speed 16-bit CPU (900/H CPU)

- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: Four-channels (640 ns / 2 bytes at 25 MHz)

(2) Minimum instruction execution time: 160 ns (at 25 MHz)

(3) Built-in RAM: 4 Kbytes
Built-in ROM:

TMP95CW64	128 Kbyte ROM
TMP95CW65	No ROM

(4) External memory expansion

- Expandable up to 16 Mbytes (shared program/data area)
- External data bus width select pin (AM8/$\overline{16}$)
- Can simultaneously support 8/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 8 channels

- With event counter function: 2 channels

(6) 16-bit timer/event counter: 2 channels

(7) General-purpose serial interface: 3 channels

(8) 10-bit A/D converter: 8 channels

(9) 8-bit D/A converter: 2 channels

(10) Watchdog timer

(11) Chip select/wait controller: 4 blocks

(12) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 26 internal interrupts:] Seven selectable priority levels
- 10 external interrupts:]

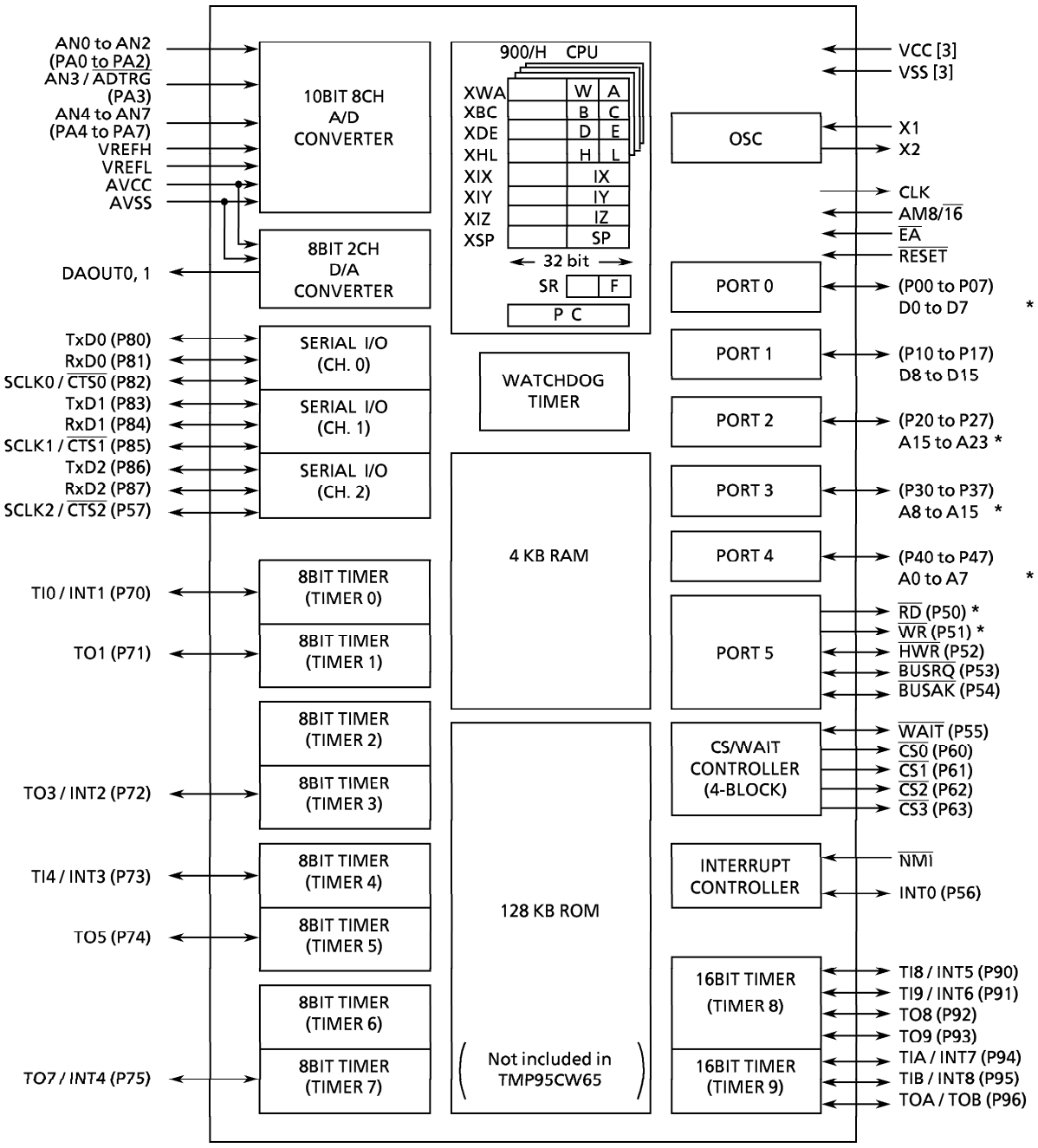
(13) Input/output ports

TMP95CW64	81 pins
TMP95CW65	55 pins

(14) Standby mode
- Four HALT modes: RUN, IDLE2, IDLE1, STOP

(15) Operating voltage
- V_{CC} = 2.7 – 3.3 V
- V_{CC} = 4.5 – 5.5 V

(16) Package
- 100-pin QFP: P-LQFP100-1414-0.50F



Note: Pin states after reset

Product	AM8/16	Pin function after reset
TMP95CW64	Fixed to high level	Multi-use pins can select function in parentheses ( ).
TMP95CW65	High level	Multi-use pins other than those marked by an asterisk can select functions in parentheses ( ).
	Low level	Multi-use pins other than those marked by asterisk can select function in parentheses ( ). However, port 1 can select functions outside parentheses ( ).

Figure 1 TMP95CW64/TMP95CW65 Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP95CW64F/W65F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1 is a pin assignment diagram for TMP95CW64F/W65F.

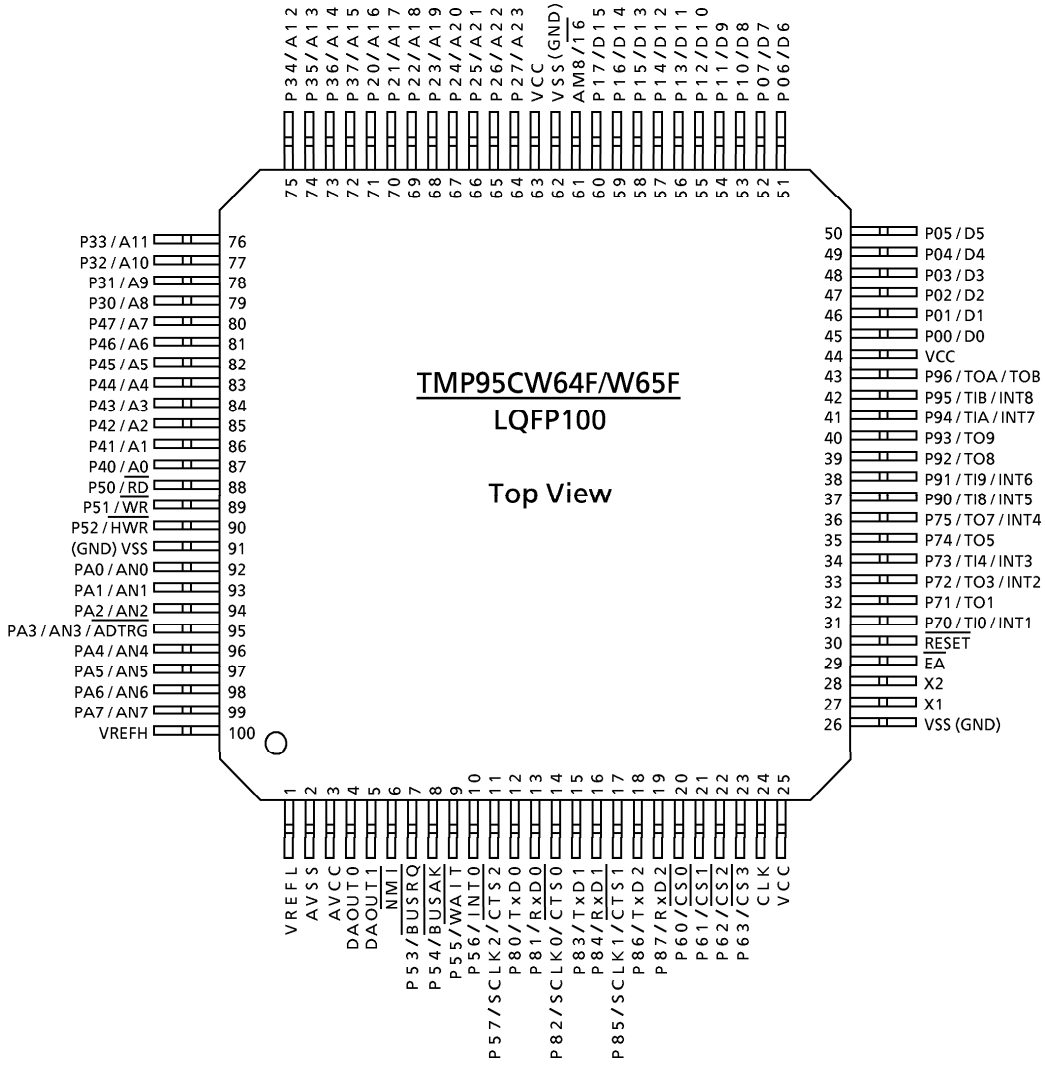


Figure 2.1 Pin Assignment Diagram (100-Pin LQFP)

2.2 Pin Names and Functions

Table 2.2 shows the names and functions of the input/output pins.

Table 2.2 Pin Names and Functions (1/4)

Pin Name	Number of Pins	Input/Output	Function
P00 to P07	8	Input/output	Port 0: I/O port. Input or output specifiable in units of bits
/ D0 to D7		Input/output	Data: Data bus 0 to 7
P10 to P17	8	Input/output	Port 1: I/O port. Input or output specifiable in units of bits
/ D8 to D15		Input/output	Data: Data bus 8 to 15
P20 to P27	8	Input/output	Port 2: I/O port. Input or output specifiable in units of bits
/ A16 to A23		Output	Address: Address bus 16 to 23
P30 to P37	8	Input/output	Port 3: I/O port. Input or output specifiable in units of bits
/ A8 to A15		Output	Address: Address bus 8 to 15
P40 to P47	8	Input/output	Port 4: I/O port. Input or output specifiable in units of bits
/ A0 to A7		Output	Address: Address bus 0 to 7
P50	1	Output	Port 50: Output-only port
/ $\overline{RD}$		Output	Read: Outputs strobe signal to read external memory (setting P5 <P50> = 0 and P5FC <P50F> = 1 outputs strobe signal at all read timings)
P51	1	Output	Port 51: Output-only port.
/ $\overline{WR}$		Output	Write: Outputs strobe signal to write data on pins D0 to D7
P52	1	Input/output	Port 52: I/O port (with built-in pull-up resistor)
/ $\overline{HWR}$		Output	Upper write: Outputs strobe signal to write data on pins D8 to D15
P53	1	Input/output	Port 53: I/O port (with built-in pull-up resistor)
/ $\overline{BUSRQ}$		Input	Bus request: Input pin to request external bus release
P54	1	Input/output	Port 54: I/O port (with built-in pull-up resistor)
/ $\overline{BUSAK}$		Output	Bus acknowledge: Output pin to acknowledge that CPU received $\overline{BUSRQ}$ and released external bus.
P55	1	Input/output	Port 55: I/O port (with built-in pull up resistor)
/ $\overline{WAIT}$		Input	Wait: Bus wait request pin for CPU (Effective when 1 + N WAIT mode, or 0 + N WAIT mode. Set using chip select/wait control register.)
P56	1	Input/output	Port 56: I/O port (with built-in pull-up resistor)
/ INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. 

Table 2.2 Pin Names and Functions (2/4)

Pin Name	Number of Pins	Input/Output	Function
P57	1	Input/output	Port 57: I/O port (with built-in pull-up resistor)
/ SCLK2		Input/output	Serial clock input/output 2
/ $\overline{\text{CTS2}}$		Input	Serial data ready to send 2 (Clear-to-send)
P60	1	Output	Port 60: Output-only port
/ $\overline{\text{CS0}}$		Output	Chip select 0: Outputs 0 if address is within specified address range
P61	1	Output	Port 61: Output-only port
/ $\overline{\text{CS1}}$		Output	Chip select 1: Outputs 0 if address is within specified address range
P62	1	Output	Port 62: Output-only port
/ $\overline{\text{CS2}}$		Output	Chip select 2: Outputs 0 if address is within specified address range
P63	1	Output	Port 63: Output-only port
/ $\overline{\text{CS3}}$		Output	Chip select 3: Outputs 0 if address is within specified address range
P70	1	Input/output	Port 70: I/O port
/ TI0		Input	Timer input 0: Input pin for timer 0
/ INT1		Input	Interrupt request pin 1: Rising-edge interrupt request pin
P71	1	Input/output	Port 71: I/O port.
/ TO1		Output	Timer output 1: Output pin for timer 0 or 1
P72	1	Input/output	Port 72: I/O port
/ TO3		Output	Timer output 3: Output pin for timer 2 or 3
/ INT2		Input	Interrupt request pin 2: Rising-edge interrupt request pin
P73	1	Input/output	Port 73: I/O port
/ TI4		Input	Timer input 4: Input pin for timer 4
/ INT3		Input	Interrupt request pin 3: Rising-edge interrupt request pin
P74	1	Input/output	Port 74: I/O port
/ TO5		Output	Timer output 5: Output pin for timer 4 or 5
P75	1	Input/output	Port 75: I/O port
/ TO7		Output	Timer output 7: Output pin for timer 6 or 7
/ INT4		Input	Interrupt request pin 4: Rising-edge interrupt request pin
P80	1	Input/output	Port 80: I/O port (with built-in pull-up resistor)
/ TxD0		Output	Serial transmission data 0
P81	1	Input/output	Port 81: I/O port (with built-in pull-up resistor)
/ RxD0		Input	Serial receive data 0
P82	1	Input/output	Port 82: I/O port (with built-in pull-up resistor)
/ SCLK0		Input/output	Serial clock input/output 0
/ $\overline{\text{CTS0}}$		Input	Serial data ready to send 0 (Clear-to-send)

Table 2.2 Pin Names and Functions (3/4)

Pin Name	Number of Pins	Input/Output	Function
P83	1	Input/output	Port 83: I/O port (with built-in pull-up resistor)
/ TxD1		Output	Serial transmission data 1
P84	1	Input/output	Port 84: I/O port (with built-in pull-up resistor)
/ RxD1		Input	Serial receive data 1
P85	1	Input/output	Port 85: I/O port (with built-in pull-up resistor)
/ SCLK1		Input/output	Serial clock input/output 1
/ $\overline{\text{CTS1}}$		Input	Serial data ready to send 1 (Clear-to-send)
P86	1	Input/output	Port 86: I/O port (with built-in pull-up resistor)
/ TxD2		Output	Serial transmission data 2
P87	1	Input/output	Port 87: I/O port (with built-in pull-up resistor)
/ RxD2		Input	Serial receive data 2
P90	1	Input/output	Port 90: I/O port
/ TI8		Input	Timer input 8: Input pin for timer 8
/ INT5		Input	Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge
P91	1	Input/output	Port 91: I/O port
/ TI9		Input	Timer input 9: Input pin for timer 8
/ INT6		Input	Interrupt request pin 6: Rising edge interrupt request pin
P92	1	Input/output	Port 92: I/O port
/ TO8		Output	Timer output 8: Output pin for timer 8
P93	1	Input/output	Port 93: I/O port
/ TO9		Output	Timer output 9: Output pin for timer 8
P94	1	Input/output	Port 94: I/O port
/ TIA		Input	Timer input A: Input pin for timer 9
/ INT7		Input	Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge
P95	1	Input/output	Port 95: I/O port
/ TIB		Input	Timer input B: Input pin for timer 9
/ INT8		Input	Interrupt request pin 8: Rising edge interrupt request pin
P96	1	Input/output	Port 96: I/O port
/ TOA		Output	Timer input A: Output pin for timer 9
/ TOB		Output	Timer input B: Output pin for timer 9
PA0 to PA2	3	Input	Port A0 to A2: Input-only port
/ AN0 to AN2		Input	Analog input 0 to 2: A/D converter input pins
PA3	1	Input	Port A3: Input-only port
/ AN3		Input	Analog input 3: A/D converter input pin
/ $\overline{\text{ADTRG}}$		Input	External start trigger

Table 2.2 Pin Names and Functions (4/4)

Pin Name	Number of Pins	Input/Output	Function
PA4 to PA7	4	Input	Port A4 to A7: Input-only port
/ AN4 to AN7		Input	Analog input 4 to 7: A/D converter input pins
DAOUT0	1	Output	D/A output 0: D/A converter 0 output pin
DAOUT1	1	Output	D/A output 1: D/A converter 1 output pin
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both falling and rising edge
CLK	1	Output	Clock output: Outputs external clock divided by 4. Pulled up during reset.
$\overline{EA}$	1	Input	External access: With TMP95CW64, connect to VCC. With TMP95CW65, connect to GND.
AM8 / $\overline{16}$	1	Input	Address mode: External data bus width select pin With TMP95CW64: Connect this pin to VCC. Data bus width at external access can be set by chip select/wait control register. With TMP95CW65: Connect to GND when external 16-bit bus is fixed or external 8/16-bit buses are mixed. When external 8-bit bus is fixed, connect to VCC.
$\overline{RESET}$	1	Input	Reset: Initializes TMP95CW64/W65 (with built-in pull-up resistor)
VREFH	1	Input	Reference voltage input pin for A/D converter (high)
VREFL	1	Input	Reference voltage input pin for A/D converter (low)
AVCC	1		Power supply pin for A/D converter and reference voltage input pin for D/A converter: Connect to power supply
AVSS	1		GND pin for A/D converter and reference voltage input pin for D/A converter: Connect to GND
X1 / X2	2	Input/output	Oscillator connecting pin
VCC	3		Collector supply pin: Connect all VCC pins to power supply
VSS	3		GND pin: Connect all VSS pins to GND (0 V)

Note: Disconnect the pull-up resistors from pins other than $\overline{RESET}$ pin by software.

3. Operation

The following describes block by block the functions and basic operation of TMP95CW64/W65.
Notes and restrictions for each block are outlined in "7, Use Precautions and Restrictions" at the end of this manual.

3.1 CPU

TMP95CW64/W65 incorporates a high-performance 16-bit CPU (900/H-CPU). For CPU operation, see the "TLCS-900/H CPU".
The following describes the unique functions of the CPU used in TMP95CW64/W65; these functions are not covered in the TLCS-900/H CPU section.

3.1.1 Reset

When resetting the TMP95CW64/W65 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level for at least 10 system clocks (ten states: 0.8 μs at 25 MHz).
When the reset is accepted, the CPU:

- Sets as follows the program counter (PC) in accordance with the reset vector stored at address FFFF00H to FFFF02H:
  PC (7: 0) ← value at FFFF00H address
  PC (15: 8)← value at FFFF01H address
  PC (23: 16) ← value at FFFF02H address
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF2:0> of the status register (SR) to 111 (sets the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register to 1 (MAX mode).
  (Note: As this product does not support a MIN mode, don't write 0 to <MAX>.)
- Clears bits <RFP2:0> of the status register to 000 (sets the register bank to 0).

When reset is released, the CPU starts executing instructions in accordance with the program counter settings. CPU internal registers not mentioned above do not change when the reset is released.
When the reset is accepted, the CPU sets internal I/O, ports, and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.
- Pulls up the CLK pin to high level.

  (Note: During reset, do not reduce the external voltage level as this can cause malfunction.)

Figure 3.1 shows an example of the basic timing of the reset operation.

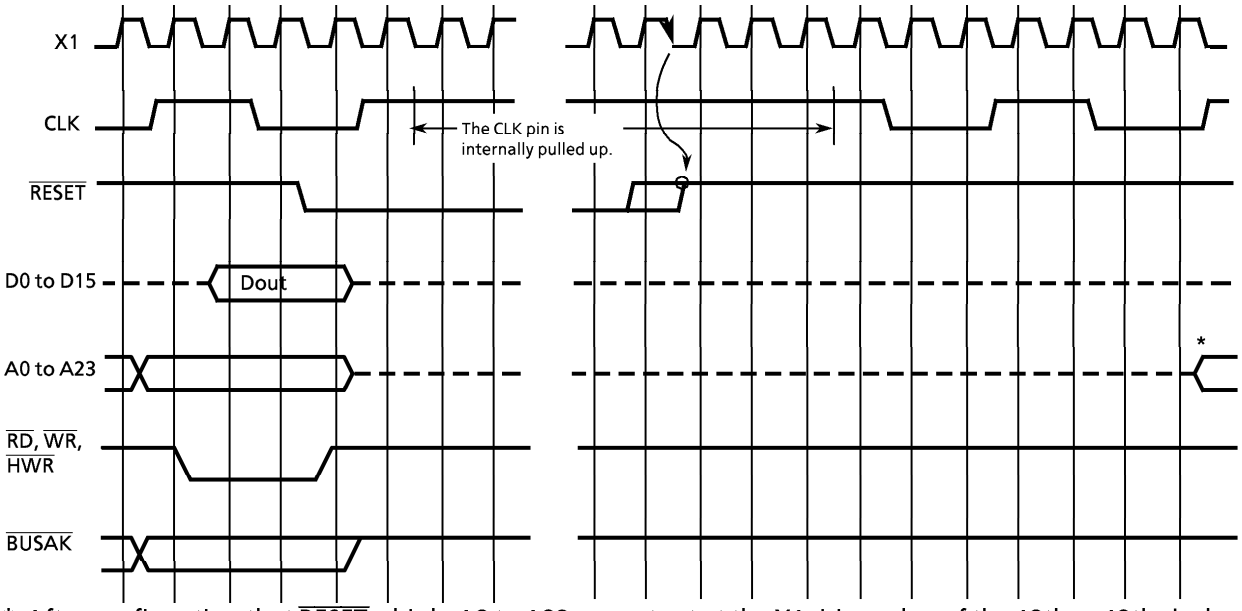


Figure 3.1 TMP95CW64/W65 Reset Timing Example

3.1.2 External Data Bus Width Selection (AM8/$\overline{16}$ Pin)

(1) With TMP95CW64 ($\overline{EA}$ high level)

Connect the input pin to VCC. After a reset, this pin accesses ROM by the internal 16-bit bus.
The data bus width for an external access depends on the setting in the <B0BUS>, <B1BUS>, <B2BUS>, or <BEXBUS> bit of the chip select/wait control registers. To access the 16-bit bus, set port 1 to D8 to D15.

(2) With TMP95CW65 ($\overline{EA}$ low level)

Selects the width of the external data bus by sampling the AM8/$\overline{16}$ input pin at the rising edge of the reset signal.

- When AM8/$\overline{16}$ = low level
  P00 to P17 function as a 16-bit data bus (D0 to D15) (8- and 16-bit data bus width mixed, or 16-bit data bus width fixed).
  The data bus width for an external access depends on the setting in the <B0BUS>, <B1BUS>, <B2BUS>, or <BEXBUS> bit of the chip select/wait control registers.
- When AM8/$\overline{16}$ = high level
  P00 to P07 function as an 8-bit data bus (D0 to D7) (external 8-bit data bus fixed).
  The <B0BUS>, <B1BUS>, <B2BUS>, or <BEXBUS> setting is ignored.

3.2 Memory Map

TMP95CW64/W65 uses 160 bytes of address space as an internal I/O area.
This is allocated to address area 000000H to 00009FH. The CPU can access this internal I/O by direct addressing mode using short command code.

Figure 3.2 shows the memory map and the access widths for the CPU addressing modes.

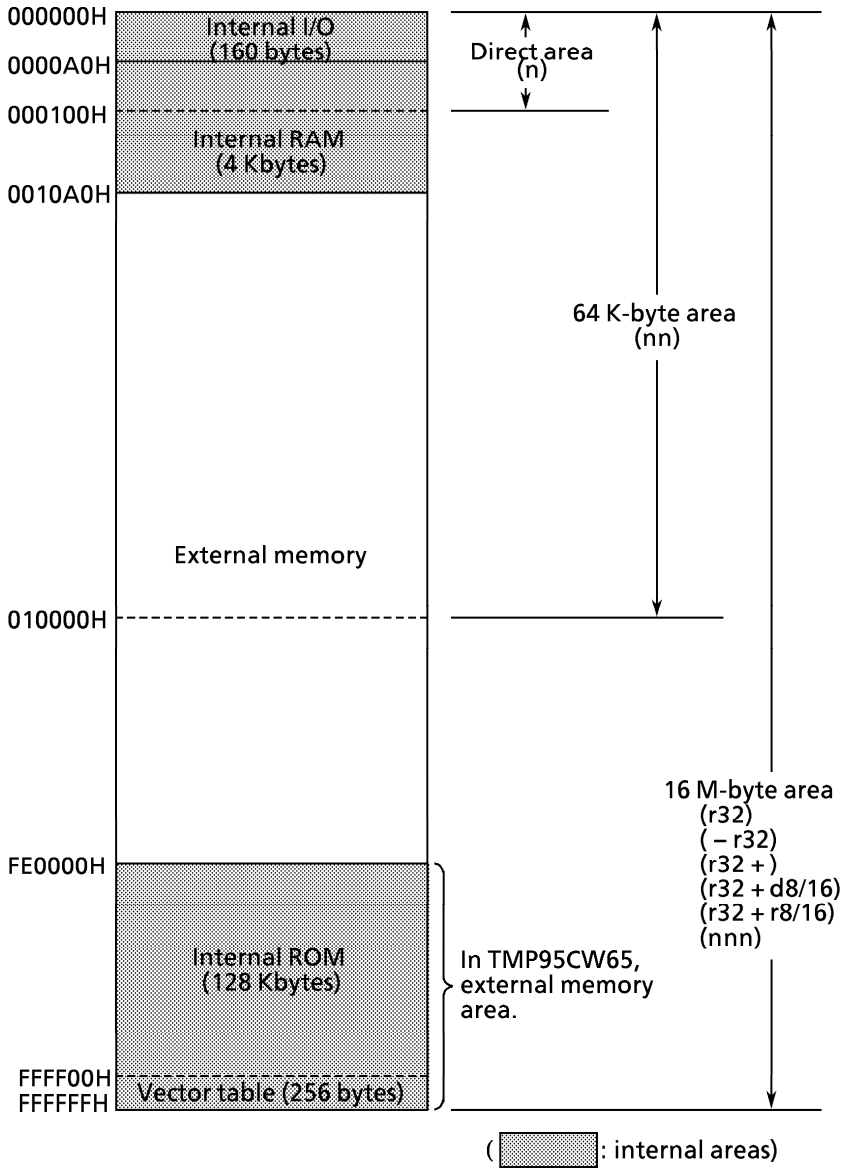


Figure 3.2 TMP95CW64/W65 Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 6.5	V
Input Voltage	V_{IN}	− 0.5 to Vcc + 0.5	V
Output current (total)	ΣI_{OL}	+ 120	mA
Output current (total)	ΣI_{OH}	− 120	mA
Power Dissipation (Ta = + 70°C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	+ 260	°C
Storage Temperature	T_{STG}	− 65 to + 150	°C
Operating Temperature	T_{OPR}	− 20 to + 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Electrical Characteristics

(1) Vcc = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

(Typical values are for Ta = + 25°C, VCC = + 5 V.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IL} V_{IL1} V_{IL2} V_{IL3} V_{IL4}		−0.3 −0.3 −0.3 −0.3 −0.3	0.8 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V
Input High Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IH} V_{IH1} V_{IH2} V_{IH3} V_{IH4}		2.2 0.7 Vcc 0.75 Vcc Vcc − 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output High Voltage	V_{OH} V_{OH1} V_{OH2}	I_{OH} = − 400 μA I_{OH} = − 100 μA I_{OH} = − 20 μA	2.4 0.75 Vcc 0.9 Vcc		V V V
Darlington Drive Current (8 Output Pins max.)	I_{DAR}	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ	−1.0	− 3.5	mA
Input Leakage Current Output Leakage Current	I_{LI} I_{LO}	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc − 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE2 IDLE1 STOP (Ta = − 20 to + 70°C) STOP (Ta = 0 to + 50°C)	I_{CC}	fc = 25 MHz 0.2 ≦ Vin ≦ Vcc − 0.2 0.2 ≦ Vin ≦ Vcc − 0.2	40 (Typ) 30 (Typ) 3.5 (Typ) 0.5 (Typ)	50 40 10 50 10	mA mA mA μA μA
Power Down Voltage (@STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0	6.0	V
Pull Up Registance	R_{RP}		45	160	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 to 4	V_{TH}		0.4	1.0 (Typ)	V

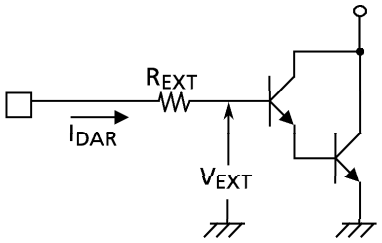
Note: I_{DAR} guarantees up to eight pins from any output port.

(2) Vcc = + 3 V ± 10%, Ta = − 20 to + 70°C (fc = 4 to 10 MHz)

(Typical values are for Ta = + 25°C, VCC = + 3 V.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IL} V_{IL1} V_{IL2} V_{IL3} V_{IL4}		−0.3 −0.3 −0.3 −0.3 −0.3	0.6 0.3 Vcc 0.25 Vcc 0.3 0.2 Vcc	V V V V V
Input High Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IH} V_{IH1} V_{IH2} V_{IH3} V_{IH4}		2.0 0.7 Vcc 0.75 Vcc Vcc − 0.3 0.8 Vcc	Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3 Vcc + 0.3	V V V V V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output High Voltage	V_{OH}	I_{OH} = − 400 μA	2.4		V
Input Leakage Current Output Leakage Current	I_{LI} I_{LO}	0.0 ≦ Vin ≦ Vcc 0.2 ≦ Vin ≦ Vcc − 0.2	0.02 (Typ) 0.05 (Typ)	± 5 ± 10	μA μA
Operating Current (RUN) IDLE2 IDLE1 STOP (Ta = − 20 to + 70°C) STOP (Ta = 0 to + 50°C)	I cc	fc = 10 MHz 0.2 ≦ Vin ≦ Vcc − 0.2 0.2 ≦ Vin ≦ Vcc − 0.2	12 (Typ) 4.5 (Typ) 0.8 (Typ) 0.5 (Typ)	25 17 5 50 10	mA mA mA μA μA
Power Down Voltage (@ STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0	6.0	V
Pull Up Registance	R_{RP}		70	400	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 to 4	V_{TH}		0.4	1.0 (Typ)	V

Refer: I_{DAR} definition diagram.



4.3 AC Electrical Characteristics

(1) Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C

(fc = 8 MHz to 25 MHz)

No.	Parameter	Symbol	Formula		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	40	125	50		40		ns
2	Clock pulse width	t_{CLK}	2.0x – 40		60		40		ns
3	A0 to 23 valid → Clock hold	t_{AK}	0.5x – 20		5		0		ns
4	Clock valid → A0 to 23 hold	t_{KA}	1.5x – 60		15		0		ns
5	A0 to 23 valid → $\overline{RD}$/$\overline{WR}$ fall	t_{AC}	1.0x – 20		30		20		ns
6	$\overline{RD}$/$\overline{WR}$ rise → A0 to 23 hold	t_{CA}	0.5x – 20		5		0		ns
7	A0 to 23 valid → D0 to 15 input	t_{AD}		3.5x – 40		135		100	ns
8	$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.5x – 45		80		55	ns
9	$\overline{RD}$ low pulse width	t_{RR}	2.5x – 40		85		60		ns
10	$\overline{RD}$ rise → D0 to 15 hold	t_{HR}	0		0		0		ns
11	$\overline{WR}$ low pulse width	t_{WW}	2.5x – 40		85		60		ns
12	D0 to 15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 40		60		40		ns
13	$\overline{WR}$ rise →D0 to 15 hold	t_{WD}	0.5x – 10		15		10		ns
14	A0 to 23 valid → $\overline{WAIT}$ input ($^{1\ WAIT}_{+\ n\ mode}$)	t_{AW}		3.5x – 90		85		50	ns
	A0 to 23 valid → $\overline{WAIT}$ input ($^{0+n\ WAIT}_{mode}$)	t_{AW}		1.5x – 40		35		20	ns
15	$\overline{RD}$/$\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{1\ WAIT}_{+\ n\ mode}$)	t_{CW}	2.5x + 0		125		100		ns
	$\overline{RD}$/$\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{0+n\ WAIT}_{mode}$)	t_{CW}	0.5x + 0		25		20		ns
16	$\overline{WR}$ rise→ PORT valid	t_{CP}		200		200		200	ns
17	$\overline{CS}$ Low pulse width (PSRAM mode)	t_{CE}	3.0x – 40		110		80		ns
18	$\overline{CS}$ fall→ D0 to 15 input (PSRAM mode)	t_{CEA}		3.0x – 60		90		60	ns
19	Address setup time (PSRAM mode)	t_{PASC}	0.5x – 15		10		5		ns
20	$\overline{CS}$ precharge time (PSRAM mode)	t_{PP}	1.0x – 10		40		30		ns

AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V , CL = 50 pF
- Input level: High 2.4 V / Low 0.45 V (D0 to D15)
  High 0.8 Vcc / Low 0.2 Vcc (except for D0 to D15)

(2) Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C

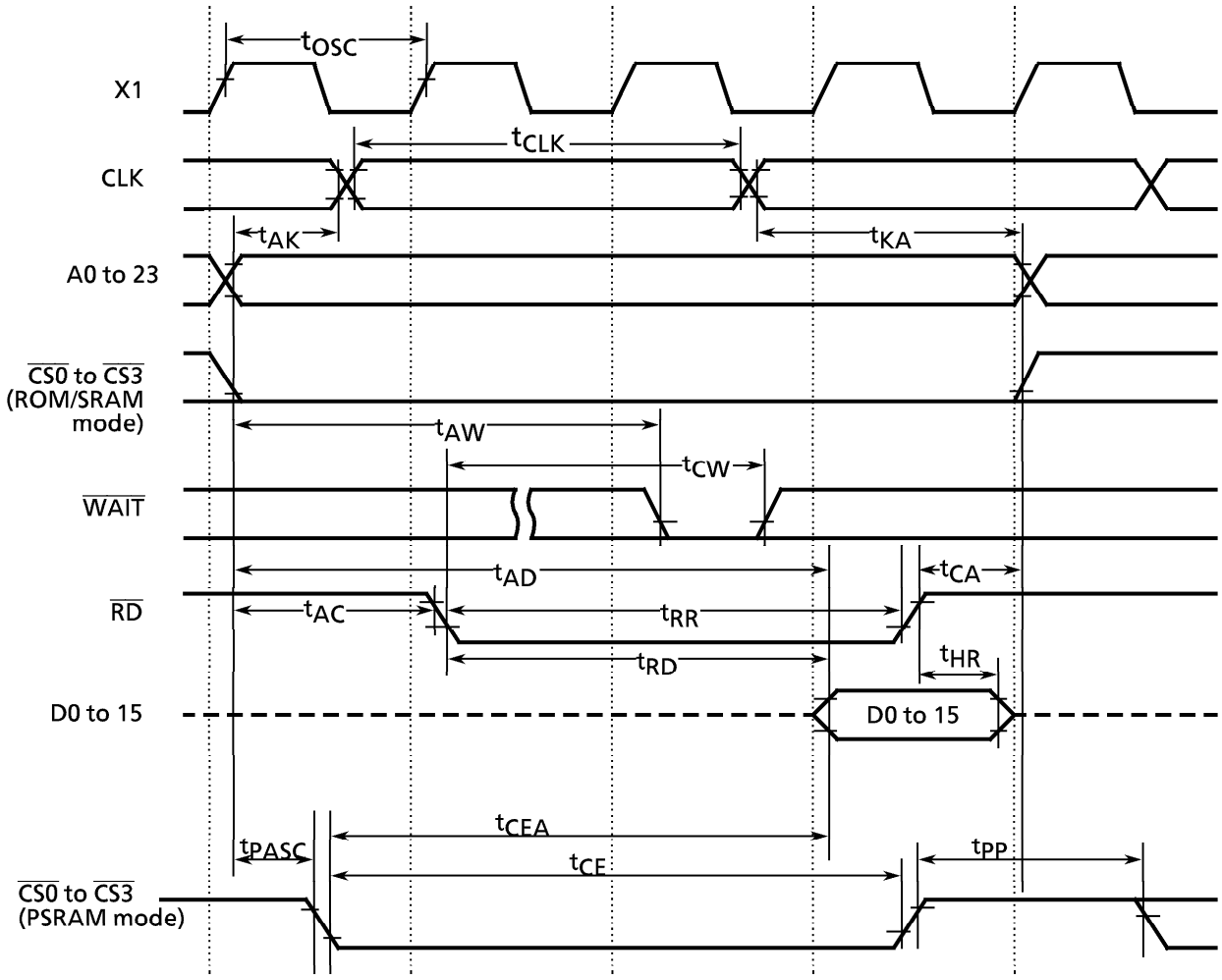
(fc = 4 MHz to 10 MHz)

No.	Parameter	Symbol	Formula		10 MHz		Unit
			Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	100	250	100		ns
2	Clock pulse width	t_{CLK}	2.0x – 70		130		ns
3	A0 to 23 valid → $\overline{RD}$/$\overline{WR}$ fall	t_{AC}	1.0x – 60		40		ns
4	$\overline{RD}$/$\overline{WR}$ rise→ A0 to 23 hold	t_{CA}	0.5x – 40		10		ns
5	A0 to 23 valid → D0 to 15 input	t_{AD}		3.5x – 125		225	ns
6	$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.5x – 115		135	ns
7	$\overline{RD}$ Low pulse width	t_{RR}	2.5x – 40		210		ns
8	$\overline{RD}$rise→ D0 to 15 hold	t_{HR}	0		0		ns
9	$\overline{WR}$ Low pulse width	t_{WW}	2.5x – 40		210		ns
10	D0 to 15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 120		80		ns
11	$\overline{WR}$ rise →D0 to 15 hold	t_{WD}	0.5x – 40		10		ns
12	A0 to 23 valid → $\overline{WAIT}$ input ($^{1\ WAIT}_{+\ n\ mode}$)	t_{AW}		3.5x – 130		220	ns
	A0 to 23 valid → $\overline{WAIT}$ input ($^{0+n\ WAIT}_{mode}$)	t_{AW}		1.5x – 80		70	ns
13	$\overline{RD}$/$\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{1\ WAIT}_{+\ n\ mode}$)	t_{CW}	2.5x + 0		250		ns
	$\overline{RD}$/$\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{0+n\ WAIT}_{mode}$)	t_{CW}	0.5x + 0		50		ns
14	$\overline{WR}$ rise→ PORT valid	t_{CP}		200		200	ns
15	$\overline{CS}$ Low pulse width (PSRAM mode)	t_{CE}	3.0x – 70		230		ns
16	$\overline{CS}$ fall → D0 to 15 input (PSRAM mode)	t_{CEA}		3.0x – 160		140	ns
17	Address setup time (PSRAM mode)	t_{PASC}	0.5x – 30		20		ns
18	$\overline{CS}$ precharge time (PSRAM mode)	t_{PP}	1.0x – 40		60		ns

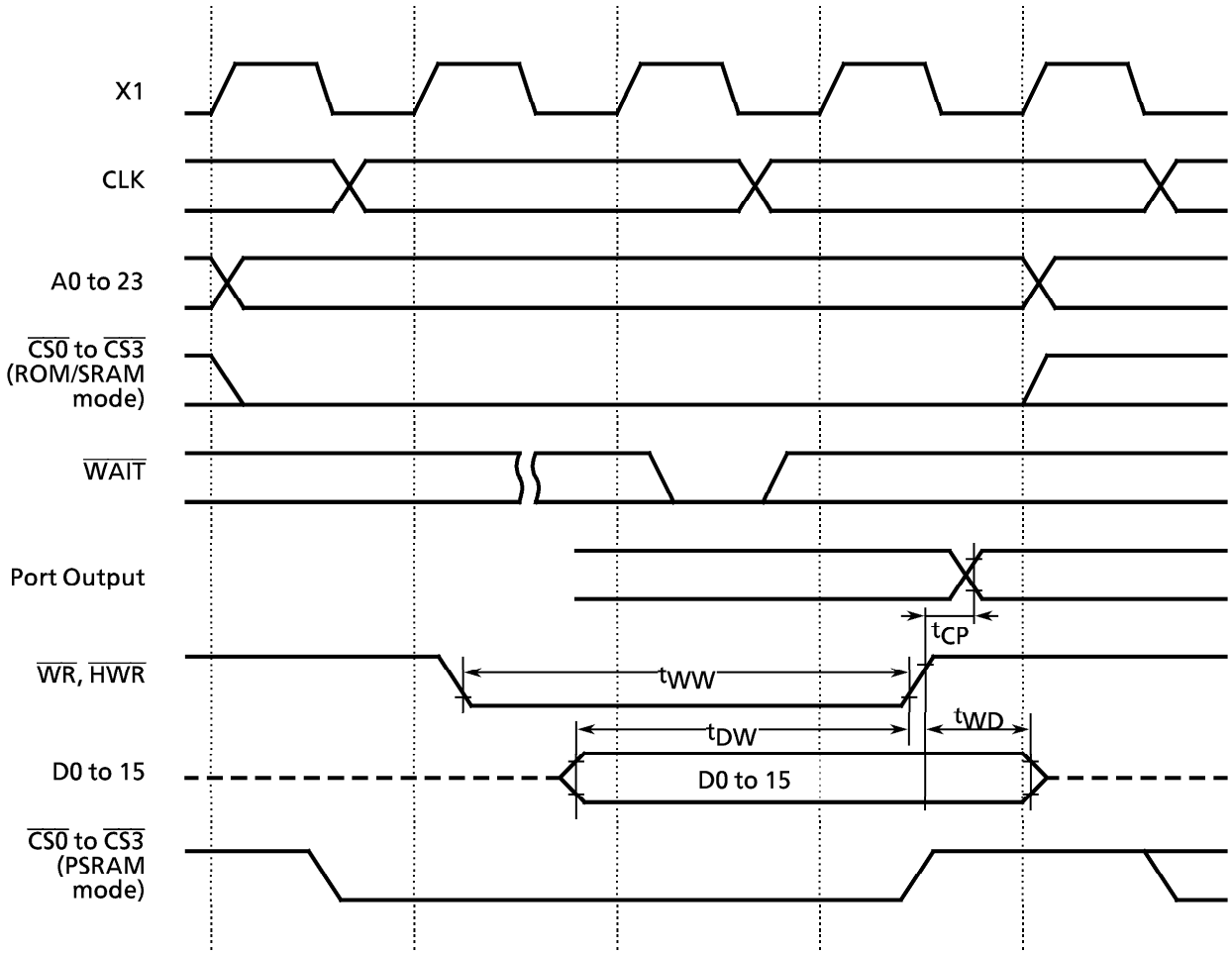
AC measuring conditions

- Output level: High 0.7x Vcc / Low 0.3x Vcc, CL = 50 pF
- Input level: High 0.9x Vcc / Low 0.1x Vcc

(3) Read Cycle


tOSC
X1
tCLK
CLK
tAK
tKA
A0 to 23
CS0 to CS3
(ROM/SRAM
mode)
tAW
tCW
WAIT
tAD
tCA
RD
tAC
tRR
tRD
tHR
D0 to 15
D0 to 15
tCEA
tPASC
tCE
tPP
CS0 to CS3
(PSRAM mode)

(4) Write Cycle



4.4 Serial Channel Timing

(1) I/O interface mode

① SCLK input mode

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

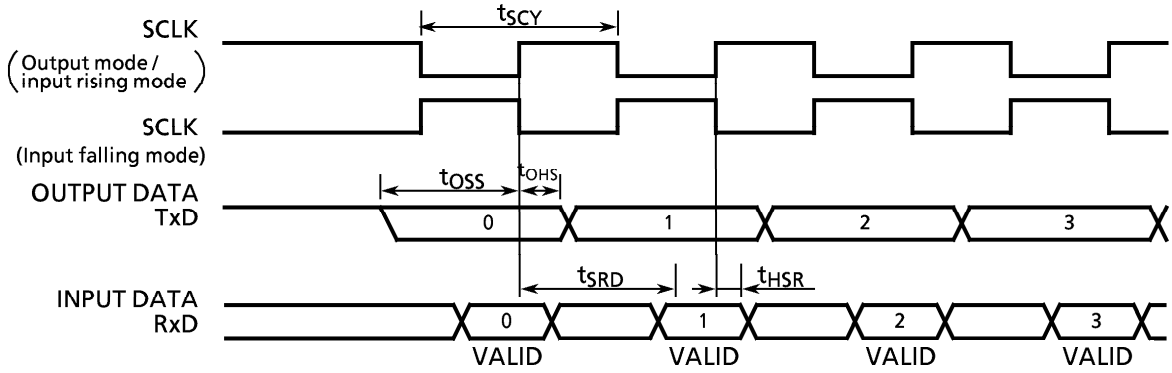
Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16x		1.6		0.64		μs
Output Data → SCLK rise/fall*	t_{OSS}	t_{SCY}/2 – 5x – 50		250		70		ns
SCLK rise/fall* → Output Data hold	t_{OHS}	5x – 100		400		100		ns
SCLK rise/fall* → input data hold	t_{HSR}	0		0		0		ns
SCLK rise/fall* → valid data input	t_{SRD}		t_{SCY} – 5x – 100		1000		340	ns

*) SCLK rise/fall: In SCLK rising edge mode, SCLK rising edge timing; in SCLK falling edge mode, SCLK falling edge timing

② SCLK output mode

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16x	8192x	1.6	819.2	0.64	327.6	μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} – 2x – 150		1250		410		ns
SCLK rising edge → Output Data hold	t_{OHS}	2x – 80		120		0		ns
SCLK rising edge → Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge → valid data input	t_{SRD}		t_{SCY} – 2x – 150		1250		410	ns



(2) UART Mode (SCLK0 to 2 External Input)

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4x + 20		420		180		ns
Low-level SCLK pulse width	t_{SCYL}	2x + 5		205		85		ns
High-level SCLK pulse width	t_{SCYH}	2x + 5		205		85		ns

4.5 A/D Conversion Characteristics

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
A/D analog reference supply voltage (+)		V_{REFH}		Vcc – 0.2		Vcc	V
A/D analog reference supply voltage (–)		V_{REFL}		Vss		Vss + 0.2	
Analog reference voltage		AV_{CC}		Vcc – 0.2		Vcc	
Analog reference voltage		AV_{SS}		Vss		Vss + 0.2	
Analog input voltage		V_{AIN}		V_{REFL}		V_{REFH}	
Analog reference voltage supply current	<VREFON> = 1	I_{REF}	Vcc = 5 V ± 10%			3.7	mA
			Vcc = 3 V ± 10%			2.2	
	<VREFON> = 0		Vcc = 2.7 to 5.5 V		0.02	5.0	μA
Total tolerance (excludes quantization error)		E_T	Vcc = 5 V ± 10%		± 1	± 3	LSB
			Vcc = 3 V ± 10%		± 1	± 3	

Note 1: 1LSB = (VREFH – VREFL) / 2^{10} [V]
Note 2: Power supply current ICC from the VCC pin includes the power supply current from the AVCC pin.

4.6 D/A Conversion Characteristics

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Analog reference voltage	AV_{CC}		Vcc – 0.2		Vcc	V
Analog reference voltage	AV_{SS}		V_{SS}		Vss + 0.2	
Total tolerance		R = 1 MΩ (Note)			7.0	LSB
		R = 5 MΩ (Note)			4.0	LSB
		R = 10 MΩ (Note)			3.5	LSB
Differential linear error				2.0		LSB

Note: R is the external load resistance on the D/A converter output pin (DAOUT0, DAOUT1).

4.7 Event Counter (External Input Clocks: TI0, TI4, TI8, TI9, TIA, TIB)

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
External input clock cycle	t_{VCK}	8x + 100		900		420		ns
External low-level input clock pulse width	t_{VCKL}	4x + 40		440		200		ns
External high-level input clock pulse width	t_{VCKH}	4x + 40		440		200		ns

4.8 Interrupt Operation

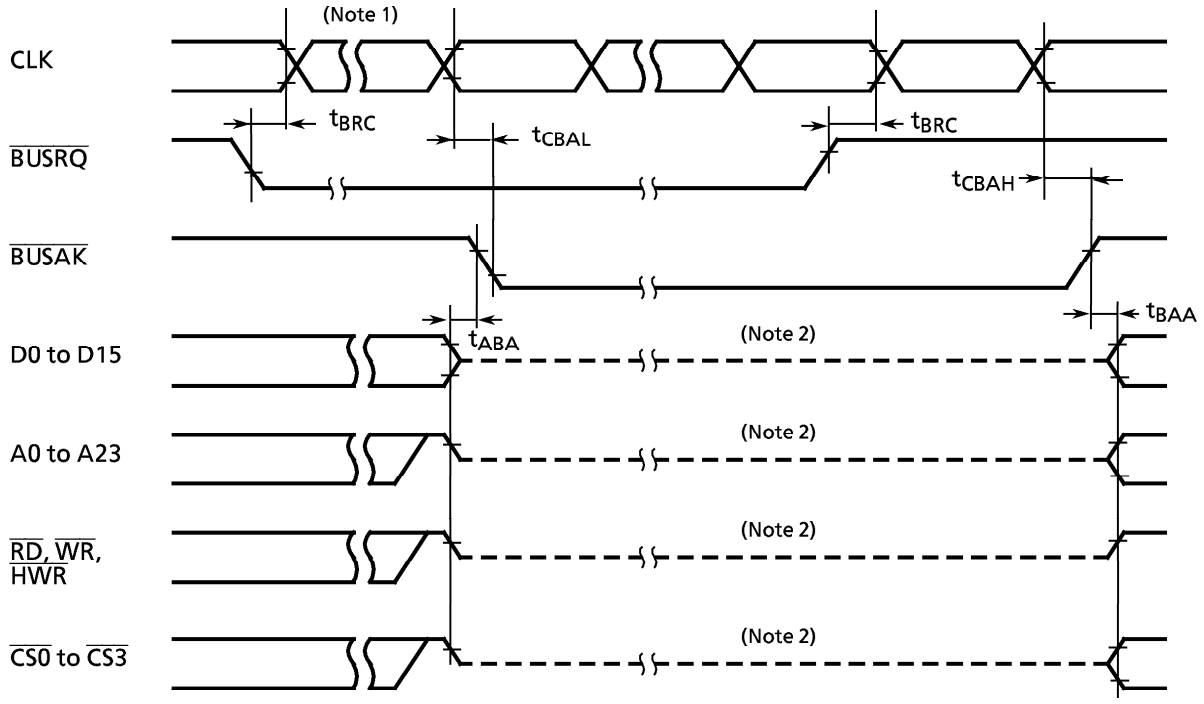
Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 to 4 low-level pulse width	t_{INTAL}	4x		400		160		ns
$\overline{NMI}$, INT0 to 4 high-level pulse width	t_{INTAH}	4x		400		160		ns
INT5 to INT8 low-level pulse width	t_{INTBL}	8x + 100		900		420		ns
INT5 to INT8 high-level pulse width	t_{INTBH}	8x + 100		900		420		ns

4.9 Bus Request/Bus Acknowledge Timing

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)
Vcc = + 3 V ± 10%, Ta = – 20 to + 70°C (fc = 4 to 10 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ setup time for CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ fall	t_{CBAL}		2.0x + 120		320		200	ns
CLK→ $\overline{BUSAK}$ rise	t_{CBAH}		0.5x + 40		90		60	ns
Time from output buffer off until $\overline{BUSAK}$ falling edge	t_{ABA}	0	80	0	80	0	80	ns
Time from $\overline{BUSAK}$ rising edge until output buffer on	t_{BAA}	0	80	0	80	0	80	ns



Note 1: When $\overline{BUSRQ}$ goes to low level to request bus release, if the current bus cycle is yet complete due to a wait, the bus is not released until the wait completes.

Note 2: The dotted line indicates only that the output buffer is off, not that the signal is at middle level. Immediately after bus release, the signal level prior to the bus release is held dynamically by the external load capacitance. Therefore, designs should allow for the fact that when using an external resistor or similar to fix the signal level while the bus is released, after bus release a delay occurs before the signal goes to its fixed level (due to the CR time constant). The internal programmable pull-up resistor continues to function in accordance with the internal signal level.