

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74AC112P, TC74AC112F, TC74AC112FN

## Dual J-K Flip Flop with Preset and Clear

The TC74AC112 is an advanced high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

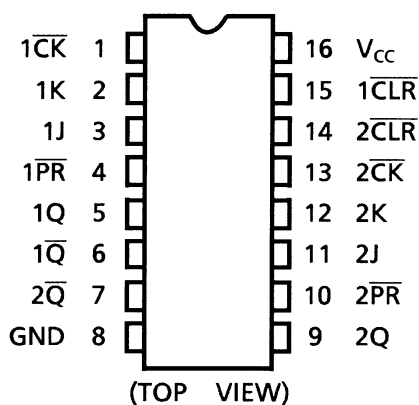
In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

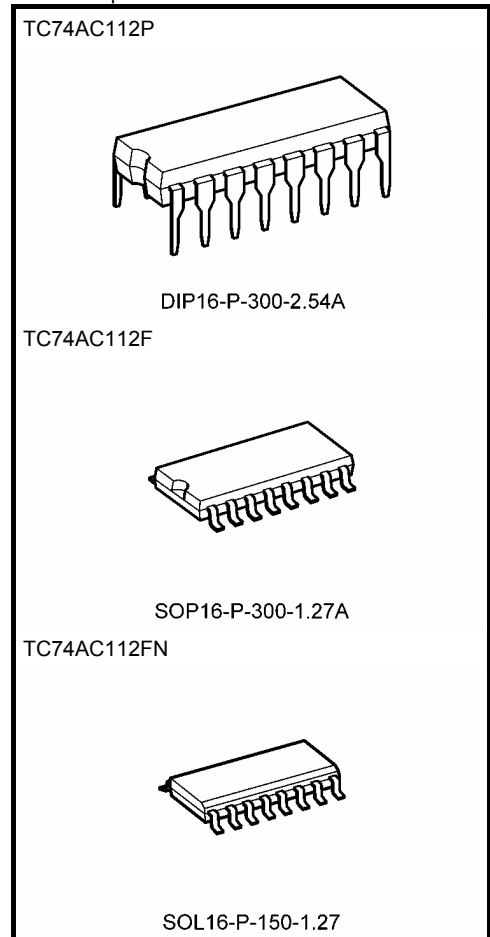
### Features

- High speed:  $f_{max} = 170 \text{ MHz (typ.) at } V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 5.5 \text{ V}$
- Pin and function compatible with 74F112

### Pin Assignment

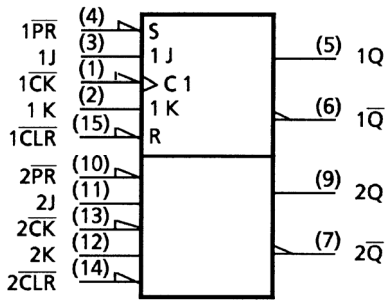


Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

## IEC Logic Symbol

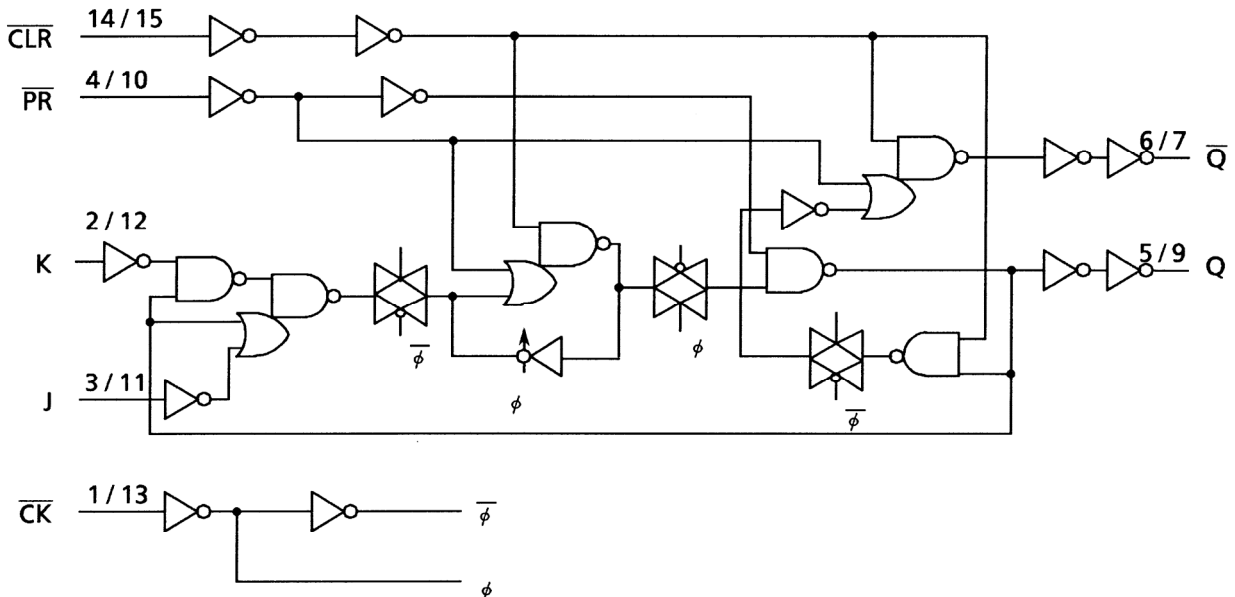


## Truth Table

Inputs					Outputs		Function
CLR	PR	J	K	CK	Q	Q̄	
L	H	X	X	X	L	H	Clear
H	L	X	X	X	H	L	Preset
L	L	X	X	X	H	H	
H	H	L	L	↓	Q <sub>n</sub>	Q̄ <sub>n</sub>	No Change
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	Q̄ <sub>n</sub>	Q <sub>n</sub>	Toggle
H	H	X	X	↑	Q <sub>n</sub>	Q̄ <sub>n</sub>	No Change

X: Don't care

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied up to 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dV	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—				
I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—				
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 12 mA	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44				
I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65				
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Unit
			VCC (V)	Limit	
Minimum pulse width ( $\overline{\text{CK}}$ )	$t_W (L)$	—	3.3 ± 0.3	7.5	ns
	$t_W (H)$		5.0 ± 0.5	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_W (L)$	—	3.3 ± 0.3	7.0	ns
			5.0 ± 0.5	5.0	
Minimum set-up time	$t_s$	—	3.3 ± 0.3	11.0	ns
			5.0 ± 0.5	6.0	
Minimum hold time	$t_h$	—	3.3 ± 0.3	0.0	ns
			5.0 ± 0.5	0.0	
Minimum removal time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_{\text{rem}}$	—	3.3 ± 0.3	3.0	ns
			5.0 ± 0.5	2.0	

### AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			VCC (V)	Min	Typ.	Max	Min		Max
Propagation delay time ( $\overline{\text{CK}} - Q$ , $\overline{Q}$ )	$t_{pLH}$	—	3.3 ± 0.3	—	9.1	15.5	1.0	17.8	ns
	$t_{pHL}$		5.0 ± 0.5	—	6.5	9.4	1.0	10.8	
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}} - Q$ , $\overline{Q}$ )	$t_{pLH}$	—	3.3 ± 0.3	—	8.6	14.6	1.0	16.8	ns
	$t_{pHL}$		5.0 ± 0.5	—	5.8	8.3	1.0	9.6	
Maximum clock frequency	$f_{\text{max}}$	—	3.3 ± 0.3	45	90	—	45	—	MHz
			5.0 ± 0.5	80	150	—	80	—	
Input capacitance	$C_{\text{IN}}$	—	—	5	10	—	10	pF	
Power dissipation capacitance	$C_{\text{PD}}$ (Note)	—	—	85	—	—	—	pF	

Note:  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

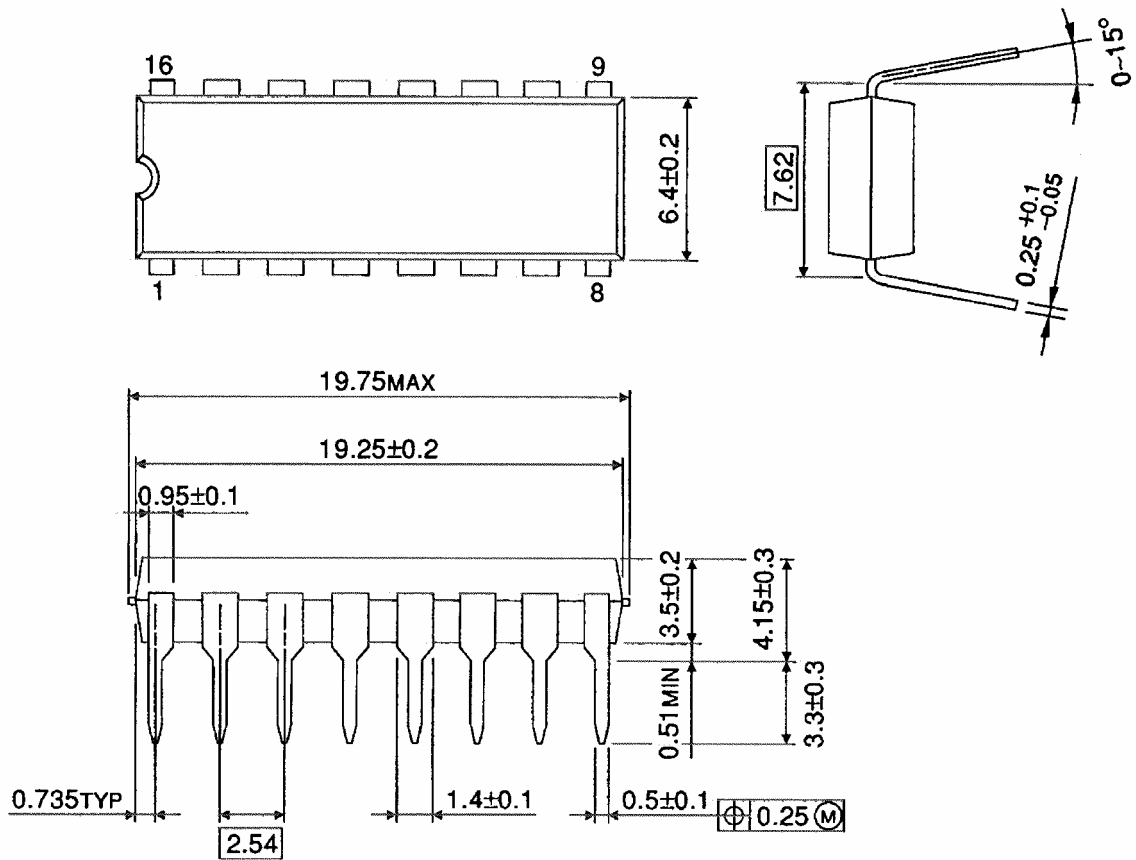
Average operating current can be obtained by the equation:

$$I_{\text{CC}} (\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/2 \text{ (per F/F)}$$

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm



Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)



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20070701-EN GENERAL

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