Low-Dropout Linear Regulator Controller with PGOOD Indication

General Description

The RT9024 is a low-dropout voltage regulator controller with a specific PGOOD indicating scheme. The part could drive an external N-MOSFET for various applications. The part is operated with V_{CC} power ranging from 3.8V to 13.5V. With such a topology, it's with advantages of flexible and cost-effective. The part comes to a small footprint package of SOT-23-6.

Ordering Information

RT9024 □□
- Package Type
  E : SOT-23-6
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100%matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Features

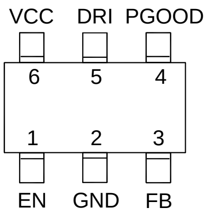
- **3.8V to 13.5V Operation Voltage**
- **0.8V ± 2% High Accuracy Voltage Reference**
- **Quick Transient Response**
- **Power Good Indicator with Delay**
- **Enable Control**
- **Small Footprint Package SOT-23-6**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- DSC
- DSLR

Pin Configurations

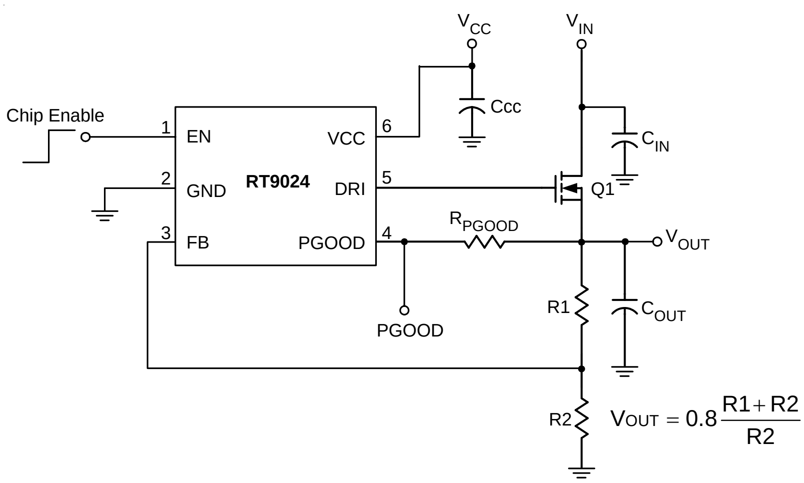
(TOP VIEW)



SOT-23-6

Note : There is no pin1 indicator on top mark for SOT-23-6 type, and pin 1 will be lower left pin when reading top mark from left to right.

Typical Application Circuit



Test Circuit

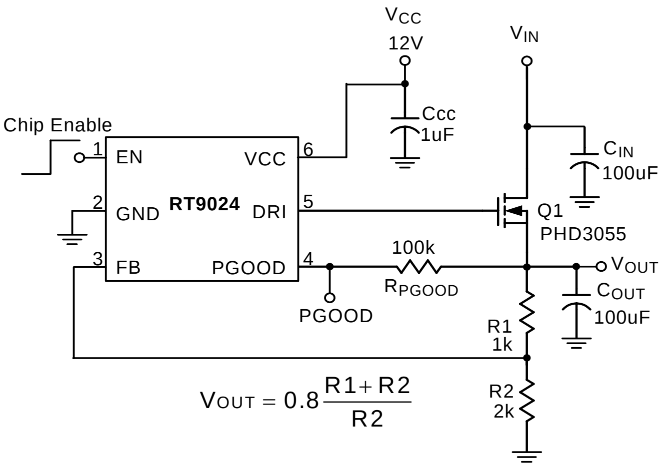


Figure 1. Typical Test Circuit

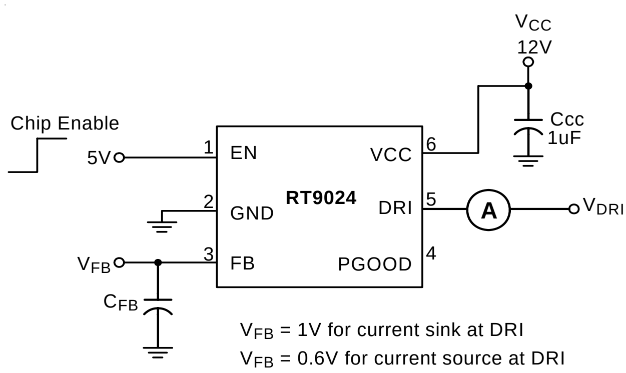
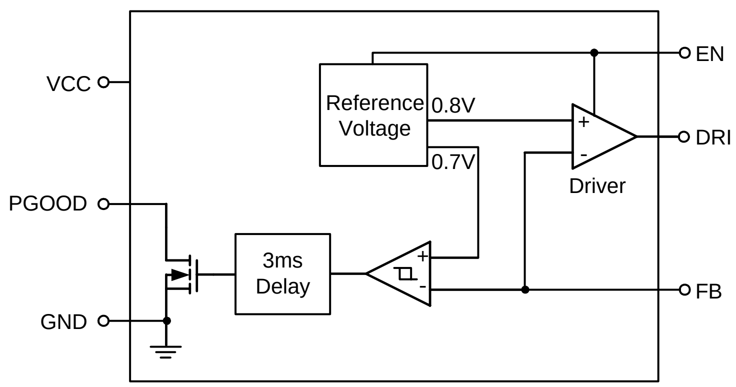


Figure 2. DRI Source/Sink Current Test Circuit

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Chip Enable (Active High).
2	GND	Ground.
3	FB	Output Voltage Feedback.
4	PGOOD	Power Good Open Drain Output.
5	DRI	Driver Output.
6	VCC	Power Supply Input.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC} ---------- 15V
- Enable Voltage ---------- 7V
- Power Good Output Voltage ---------- 7V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.4W
- Package Thermal Resistance (Note 4)
  SOT-23-6, θ_{JA} ---------- 250°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, V_{CC} ---------- 3.8V to 13.5V
- Enable Voltage ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V/12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Operation Voltage Range		V_{CC} Input Range	3.8	--	13.5	V
POR Threshold		V_{CC} Rising	3.15	3.4	3.65	V
POR Hysteresis		V_{CC} Falling	0.1	0.2	0.3	V
V_{CC} Supply Current		V_{CC} = 12V	--	0.3	0.8	mA
Driver Source Current		V_{CC} = 12V, V_{DRI} = 6V	5	--	--	mA
Driver Sink Current		V_{CC} = 12V, V_{DRI} = 6V	5	--	--	mA
Reference Voltage (V_{FB})		V_{CC} = 12V, V_{DRI} = 5V	0.784	0.8	0.816	V
Reference Line Regulation (V_{FB})		V_{CC} = 4.5V to 15V	--	3	6	mV
Amplifier Voltage Gain		V_{CC} = 12V, No Load	--	70	--	dB
PSRR at 100Hz, No Load		V_{CC} = 12V, No Load	50	--	--	dB
Power Good						
Rising Threshold		V_{CC} = 12V	85	90	95	%
Hysteresis		V_{CC} = 12V	--	15	--	%
Sink Capability		V_{CC} = 12V @ 1mA	--	0.2	0.4	V
Delay Time		V_{CC} = 12V	1	3	10	ms
Falling Delay		V_{CC} = 12V	--	15	20	us

To be Continued

Parameter		Test Conditions	Min	Typ	Max	Units
Chip Enable						
EN Rising Threshold		V_{CC} = 12V	--	0.7	1	V
EN Hysteresis		V_{CC} = 12V	--	30	--	mV
Standby Current		V_{CC} = 12V, V_{EN} = 0V	--	--	5	uA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

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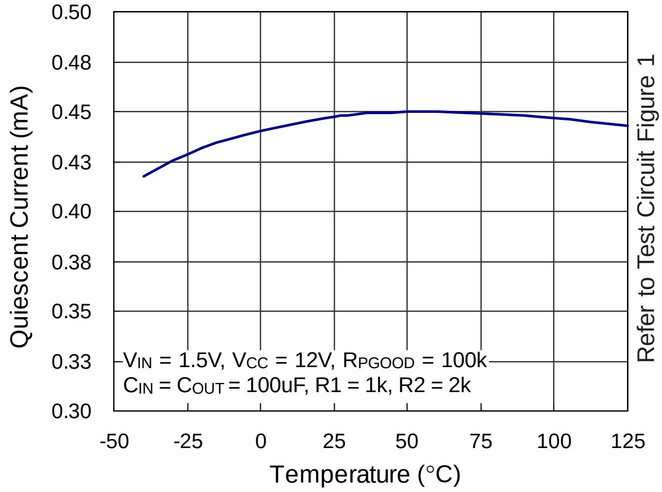
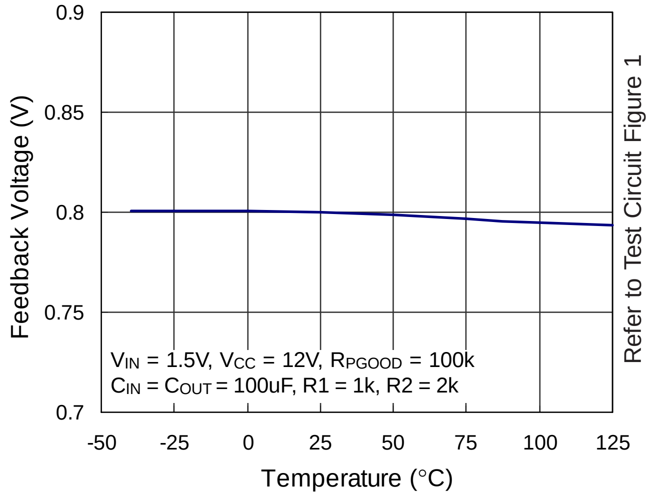
Typical Operating Characteristics

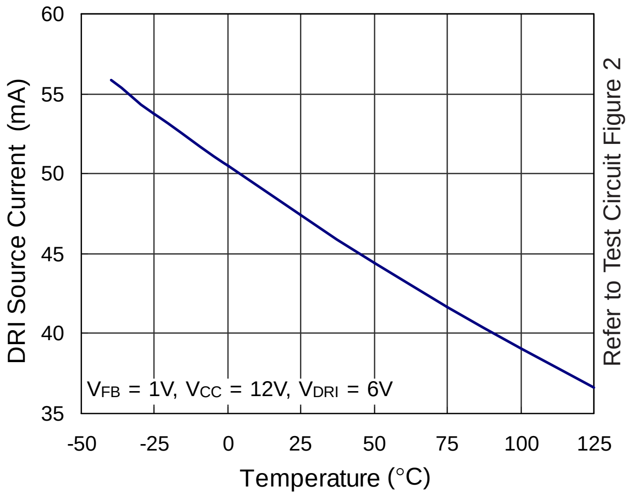
Quiescent Current vs. Temperature



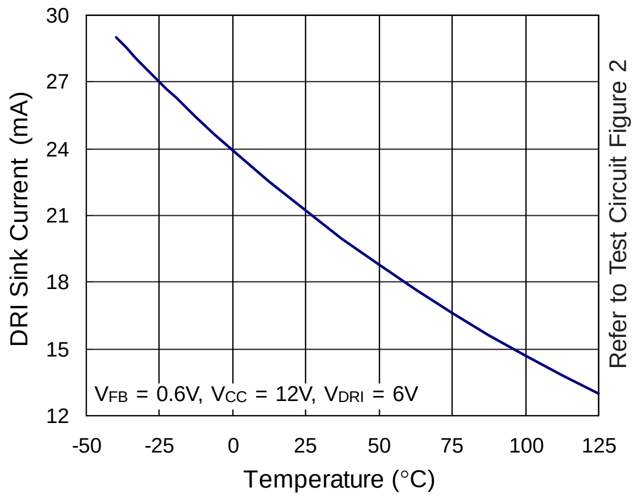
Feedback Voltage vs. Temperature



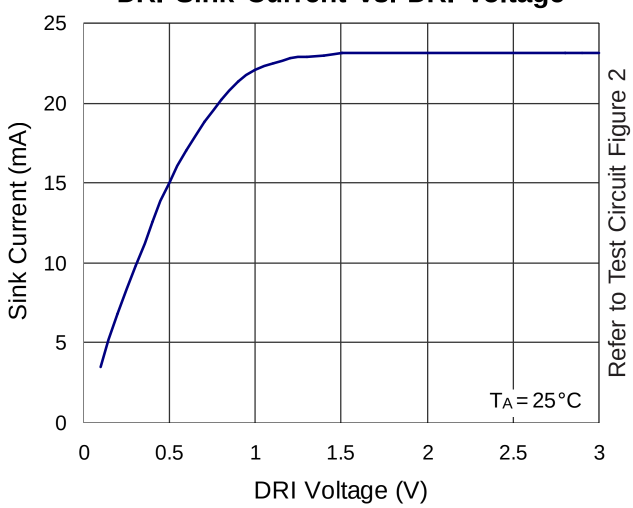
DRI Source Current vs. Temperature



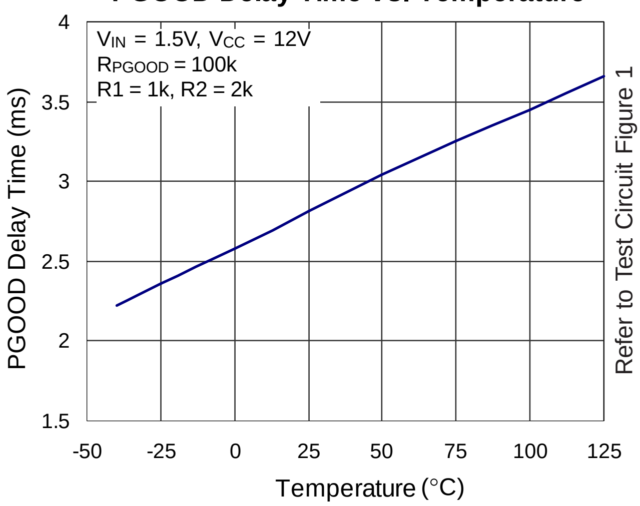
DRI Sink Current vs. Temperature



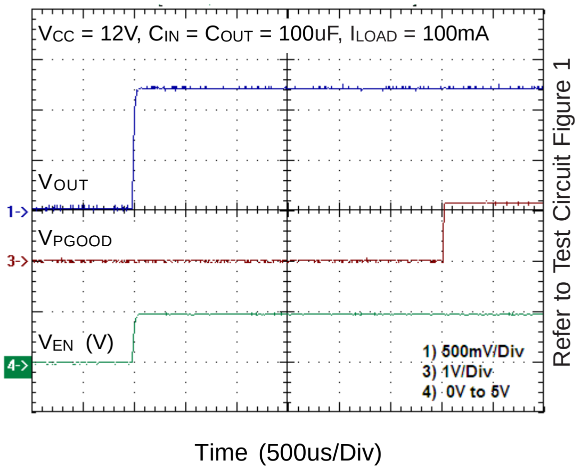
DRI Sink Current vs. DRI Voltage



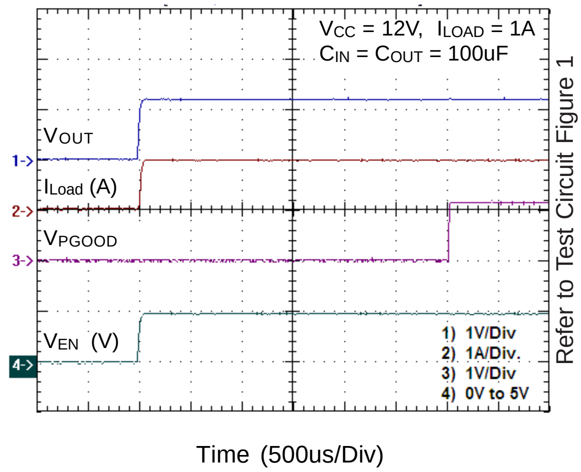
PGOOD Delay Time vs. Temperature



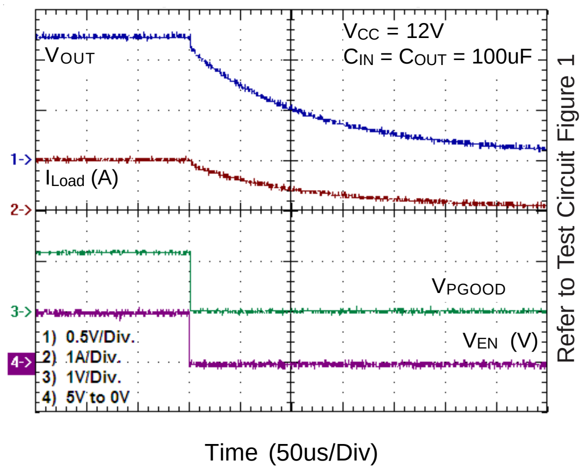
PGOOD Delay Time



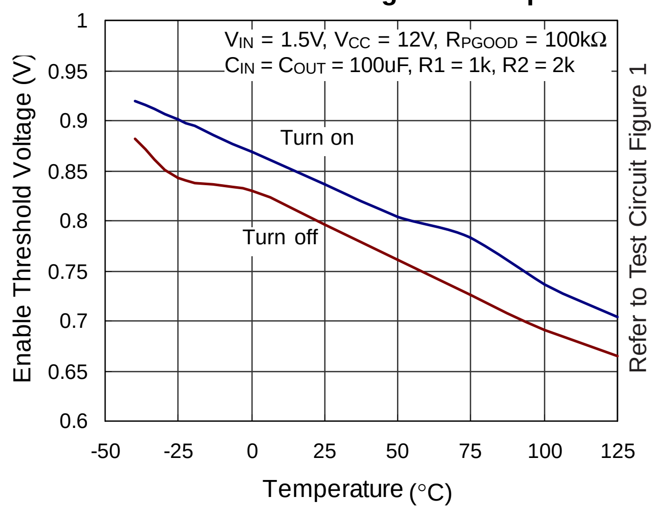
PGOOD Delay Time



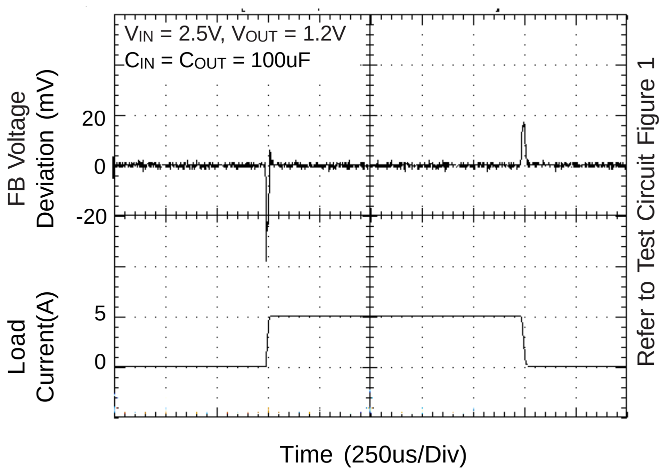
PGOOD Off



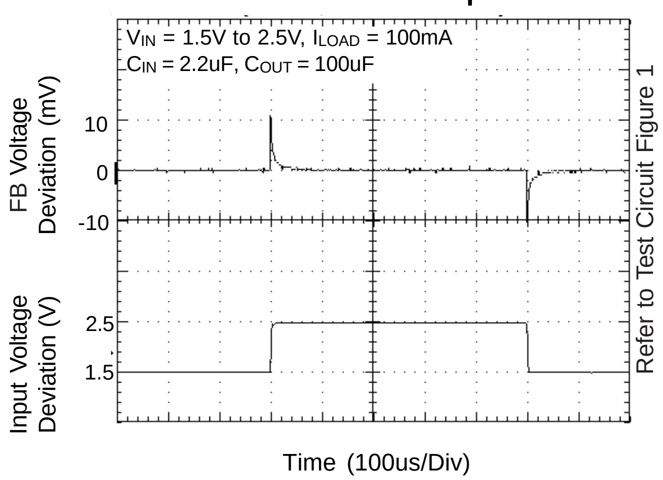
Enable Threshold Voltage vs. Temperature



Load Transient Response



Line Transient Response



Application Information

Capacitors Selection

Careful selection of the external capacitors for RT9024 is highly recommended in order to remain high stability and performance.

Regarding the supply voltage capacitor, connecting a capacitor which is ≥ 1µF between V_{CC} and ground is a must. The capacitor improves the supply voltage stability for proper operation.

Regarding the input capacitor, connecting a capacitor which ≥ 100µF between V_{IN} and ground is recommended to increase stability. With large value of capacitance could result in better performance for both PSRR and line transient response.

When driving external pass element, connecting a capacitor ≥ 100µF between V_{OUT} and ground is recommended for stability. With larger capacitance can reduce noise and improve load transient response and PSRR.

Output Voltage Setting

The RT9024 develops a 0.8V reference voltage; especially suitable for low voltage application. As shown in application circuit, the output voltage could easy set the output voltage by R1 & R2 divider resistor.

Power Good Function

The RT9024 has the power good function with delay. The power good output is an open drain output. Connect a 100kΩ pull up resistor to V_{OUT} to obtain an output voltage. When the output voltage arrives 90% of normal value. PGOOD will become active and be pulled high by external circuits with typically 3ms delay.

Chip Enable Operation

Pull the EN pin low to drive the device into shutdown mode. During shutdown mode, the standby current drops to $5\mu A_{(MAX)}$. The external capacitor and load current determine the output voltage decay rate. Drive the EN pin high to turn on the device again.

MOSFET Selection

The RT9024 are designed to driver external N-MOSFET pass element. MOSFET selection criteria include threshold voltage V_{GS} (V_{TH}), maximum continuous drain current ID, on-resistance $R_{DS(ON)}$,maximum drain-to-source voltage V_{DS} and package thermal resistance $\theta_{(JA)}$.

The most critical specification is the MOSFET $R_{DS(ON)}$. Calculate the required $R_{DS(ON)}$ from the following formula:

$$\text{N}-\text{MOSFET } R_{DS(ON)} = \frac{V_{IN} - V_{OUT}}{I_{LOAD}}$$

For example, the MOSFET operate up to 2A when the input voltage is 1.5V and set the output voltage is 1.2V, R_{ON} = (1.5V-1.2V) / 2A = 150mΩ, the MOSFET's R_{ON} must be lower than 150mΩ. Philip PHD3055E MOSFET with an $R_{DS(ON)}$ of 120mΩ(typ.) is a suitable solution.

The power dissipation is calculate as :

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

The thermal resistance from junction to ambient $\theta_{(JA)}$ is :

$$\theta_{(JA)} = \frac{(T_J - T_A)}{P_D}$$

In this example, P_D = (1.5V – 1.2V) x 2A = 0.6W. The PHD3055E's $\theta_{(JA)}$ is 75°C/W for its D-PAK package, which translates to a 45°C temperature rise above ambient. The package provides exposed backsides that directly transfer heat to the PCB board.

PNP Transistor Selection

The RT9024 could driver the PNP transistor to sink output current. PNP transistor selection criteria include DC current gain h_{FE}, threshold voltage V_{EB}, collector-emitter voltage V_{EN}, maximum continues collector current I_C, package thermal resistance $\theta_{(JA)}$.

For example, the PNP transistor operates sink current up to 0.5A when the input voltage is 1.5V and set the output voltage is 1.2V. As show in Figure 3. A KSB772 PNP transistor, the V_{EN} = 1.2V, V_{BE} = -1V, I_C = 0.5A, I_B = 0.5/160 ≥ 3.125mA, when the DRI pin voltage is 0.2V could sink $6.8mA_{(MAX)}$ is a close match.

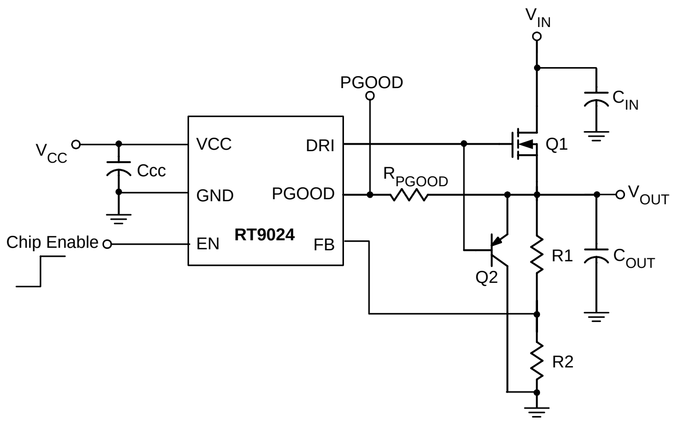


Figure 3

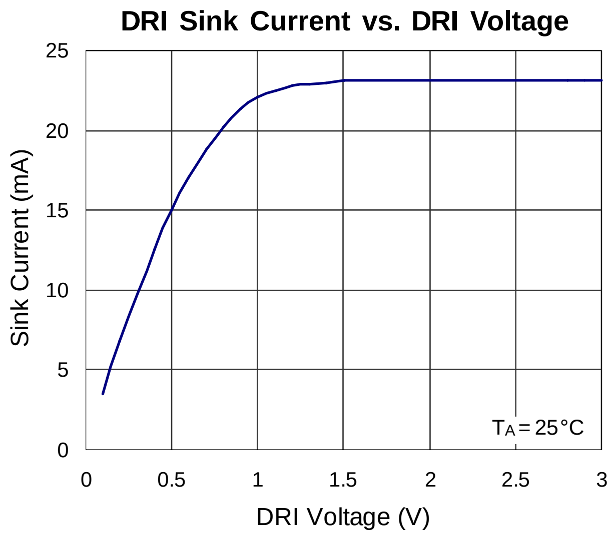


Figure 4

Layout Considerations

There are three critical layout considerations. One is the divider resistors should be located to RT9024 as possible to avoid inducing any noise. The second is capacitors place. The C_{IN} and C_{OUT} have to put at near the N-MOSFET for improve performance. The third is the copper area for pass element. We have to consider when the pass element operating under high power situation that could rise the junction temperature. In addition to the package thermal resistance limit, we could add the copper area to improve the power dissipation. As show in Figure 5 and Figure 6.

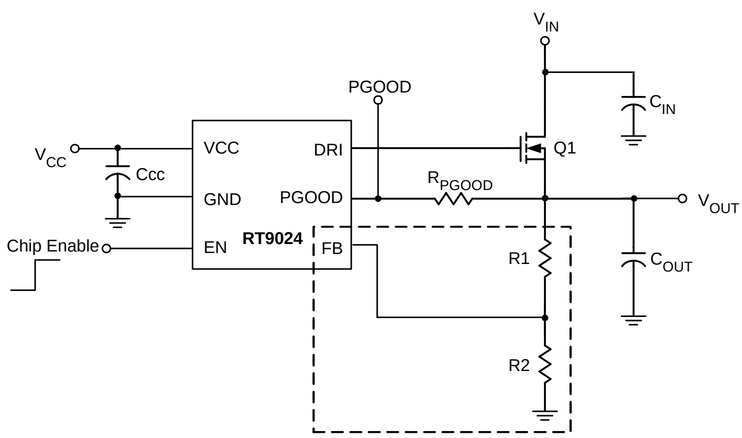


Figure 5

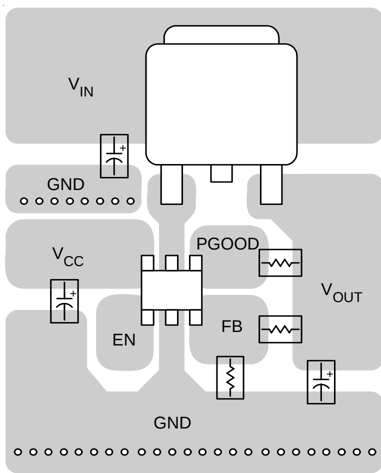
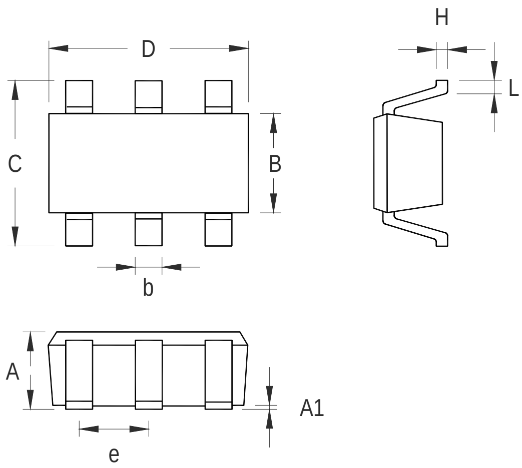


Figure 6

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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