



**AO4922**

**Asymmetric Dual N-Channel Enhancement Mode Field Effect Transistor**

**SRFET™**

**General Description**

The AO4922 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A monolithically integrated Schottky diode in parallel with the synchronous MOSFET to boost efficiency further. *Standard Product AO4922 is Pb-free (meets ROHS & Sony 259 specifications). AO4922L is a Green Product ordering option. AO4922L and AO4922 are electrically identical.*

**Features**

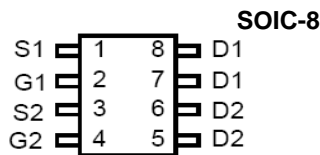
**FET1**

$V_{DS} (V) = 30V$   
 $I_D = 9A$   
 $R_{DS(ON)} < 15.8m\Omega$   
 $R_{DS(ON)} < 18.5m\Omega$

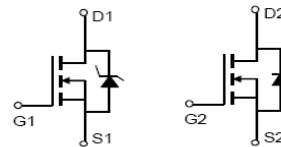
**FET2**

$V_{DS}(V) = 30V$   
 $I_D=7.3A (V_{GS} = 10V)$   
 $<24m\Omega (V_{GS} = 10V)$   
 $<29m\Omega (V_{GS} = 4.5V)$

**UIS TESTED!**  
**Rg, Ciss, Coss, Crss Tested**



**SRFET™**  
Soft Recovery MOSFET:  
Integrated Schottky Diode



**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max FET1	Max FET2	Units
Drain-Source Voltage	$V_{DS}$	30	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	V
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	9.0	7.3	A
$T_A=70^\circ C$		7.2	5.9	
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	40	40	
Avalanche Current <sup>B</sup>	$I_{AR}$	22	12	A
Repetitive avalanche energy $L=0.3mH$ <sup>B</sup>	$E_{AR}$	73	22	mJ
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.0	2.0	W
		$T_A=70^\circ C$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ C$

**Thermal Characteristics FET1**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Steady-State		74	90	
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	32	40	$^\circ C/W$

**Thermal Characteristics FET2**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Steady-State		74	90	
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	32	40	$^\circ C/W$

FET1 Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$ , $V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$		0.01 6	0.1 20	mA
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 12\text{V}$			0.1	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.5	1.8	2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$ , $V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=9\text{A}$ $T_J=125^\circ\text{C}$		13 20.2	15.8 25.2	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=7\text{A}$		15	18.5	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=9\text{A}$		78		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.38	0.5	V
$I_S$	Maximum Body-Diode + Schottky Continuous Current				4	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$		1980	2574	pF
$C_{oss}$	Output Capacitance			317		pF
$C_{rss}$	Reverse Transfer Capacitance			111		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		1.3	2.0	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $I_D=9\text{A}$		33.0	43	
$Q_g(4.5\text{V})$	Total Gate Charge			15.0		nC
$Q_{gs}$	Gate Source Charge			5.3		nC
$Q_{gd}$	Gate Drain Charge			6.0		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $R_L=1.7\Omega$ , $R_{GEN}=3\Omega$		5.5		ns
$t_r$	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off Delay Time			27.0		ns
$t_f$	Turn-Off Fall Time			4.3		ns
$t_{rr}$	Body Diode Reverse Recovery Time		$I_F=9\text{A}$ , $dI/dt=300\text{A}/\mu\text{s}$		11	13
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=9\text{A}$ , $dI/dt=300\text{A}/\mu\text{s}$		7		nC

A: The value of  $R_{\theta JA}$  is measured with the device in a still air environment with  $T_A=25^\circ\text{C}$ . The power dissipation  $P_{DSM}$  and current rating  $I_{DSM}$  are based on  $T_{J(MAX)}=150^\circ\text{C}$ , using  $t \leq 10\text{s}$  junction-to-ambient thermal resistance.

B: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ .

C: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using  $<300 \mu\text{s}$  pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

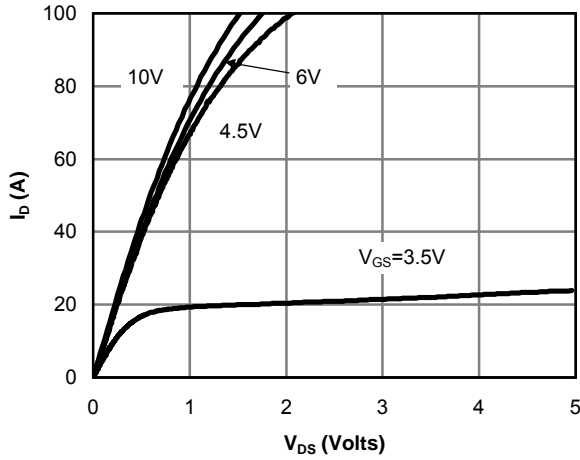


Figure 1: On-Region Characteristics

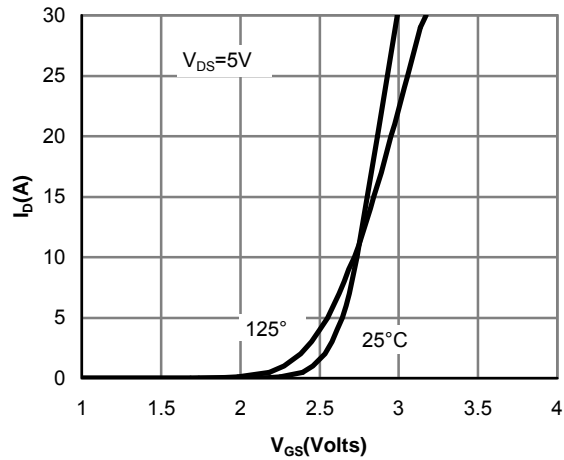


Figure 2: Transfer Characteristics

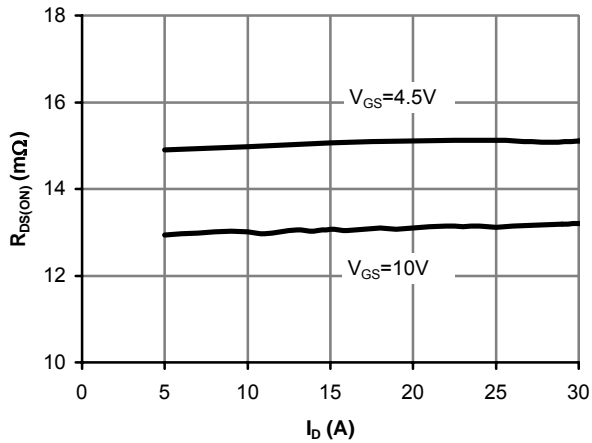


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

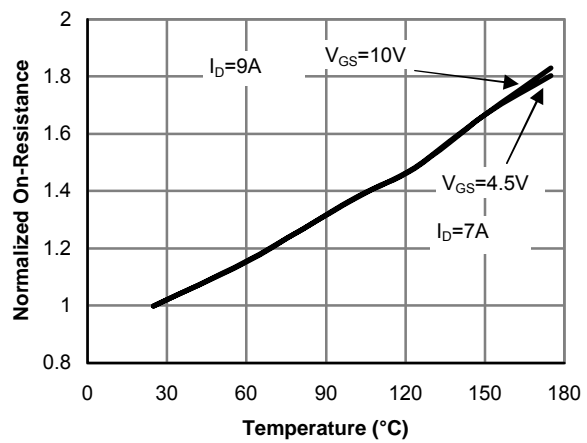


Figure 4: On-Resistance vs. Junction Temperature

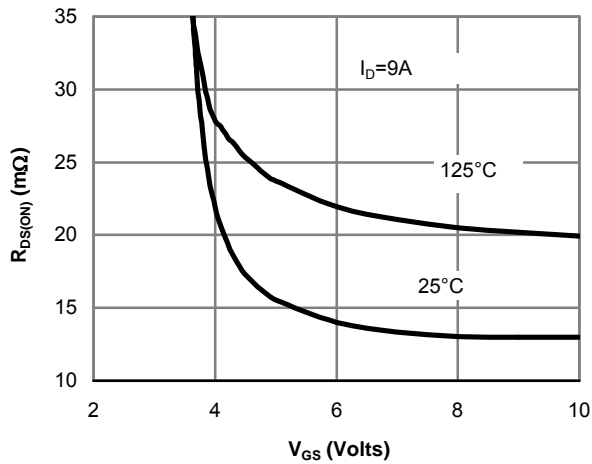


Figure 5: On-Resistance vs. Gate-Source Voltage

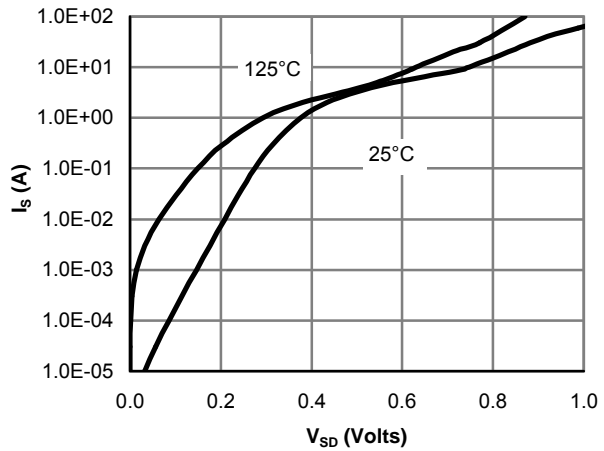


Figure 6: Body-Diode Characteristics

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

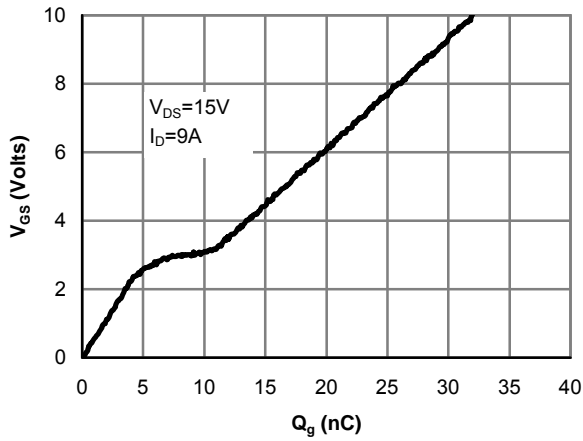


Figure 7: Gate-Charge Characteristics

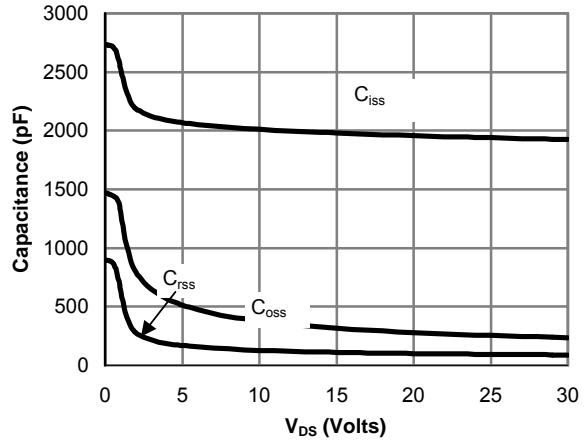


Figure 8: Capacitance Characteristics

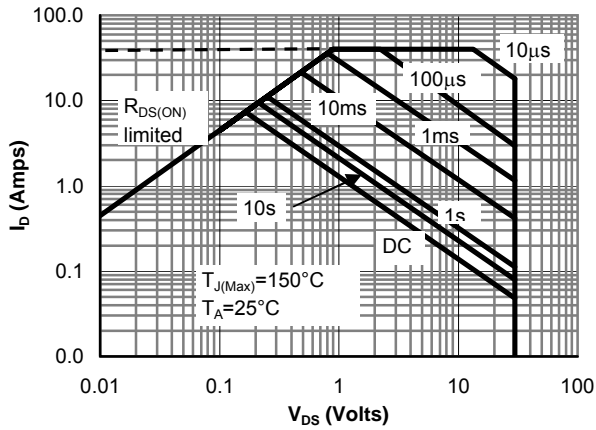


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

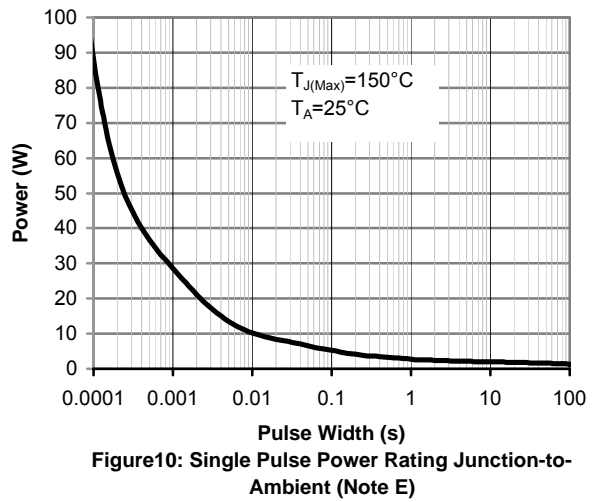


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

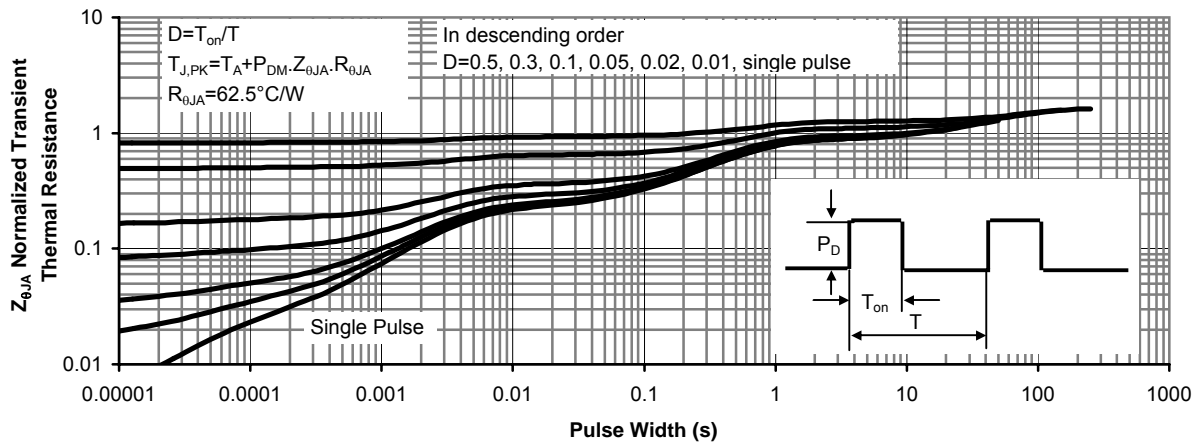


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

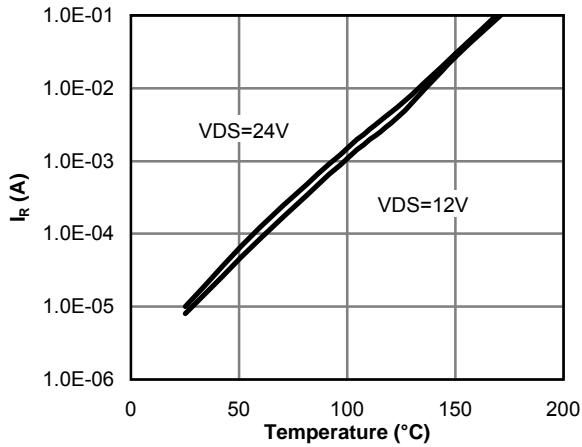


Figure 12: Diode Reverse Leakage Current vs. Junction Temperature

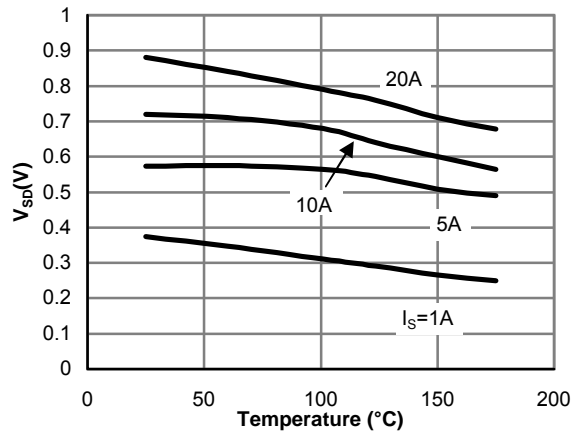


Figure 13: Diode Forward voltage vs. Junction Temperature

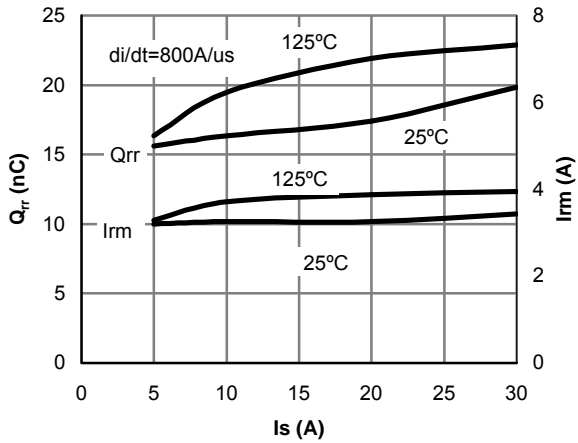


Figure 14: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

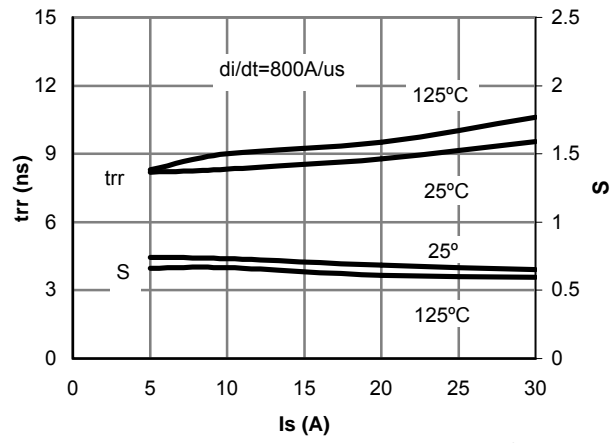


Figure 15: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

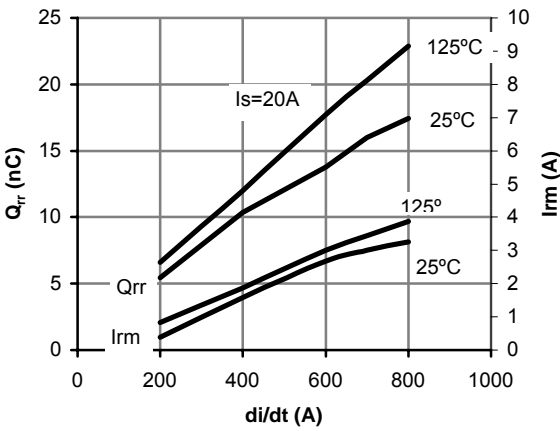


Figure 16: Diode Reverse Recovery Charge and Peak Current vs. di/dt

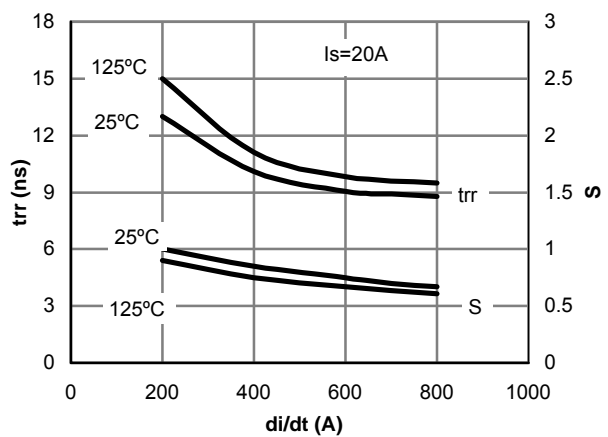


Figure 17: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

FET2 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		0.002	1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±12V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.7	1	1.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	40			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =7.3A T <sub>J</sub> =125°C		20 28	24 35	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		23.5	29	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5A		34.7	48	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =7.3A		26		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.71	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.8	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		900	1100	pF
C <sub>oss</sub>	Output Capacitance			88		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			65		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		0.95	1.5	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =7.3A		10	12	nC
Q <sub>gs</sub>	Gate Source Charge			1.8		nC
Q <sub>gd</sub>	Gate Drain Charge			3.75		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =2Ω, R <sub>GEN</sub> =6Ω		3.2		ns
t <sub>r</sub>	Turn-On Rise Time			3.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			21.5		ns
t <sub>f</sub>	Turn-Off Fall Time			2.7		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =7.3A, dI/dt=100A/μs		16.8	21	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =7.3A, dI/dt=100A/μs		8		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t<sub>s</sub> ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

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FET2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

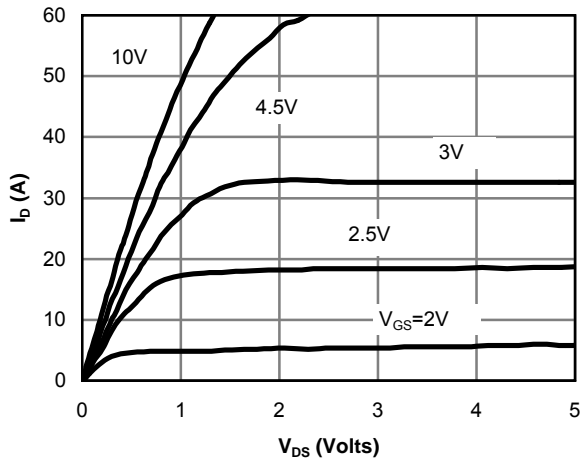


Figure 1: On-Region Characteristics

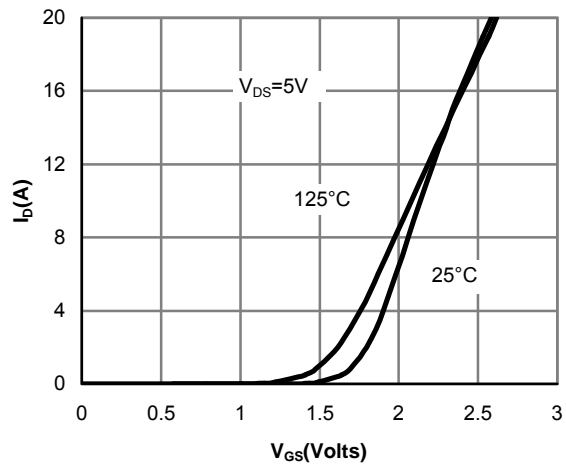


Figure 2: Transfer Characteristics

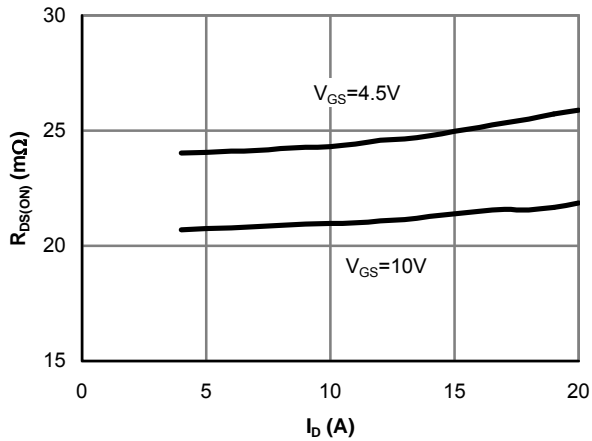


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

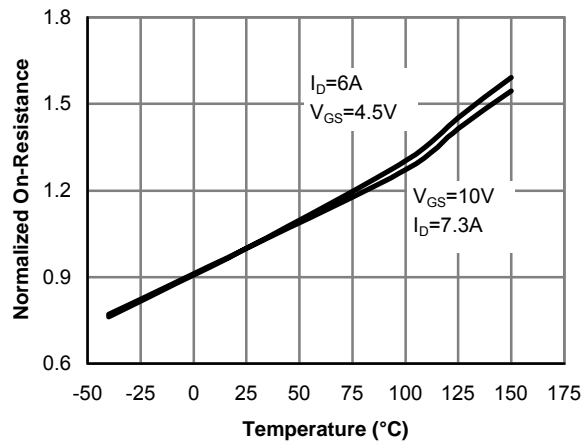


Figure 4: On-Resistance vs. Junction Temperature

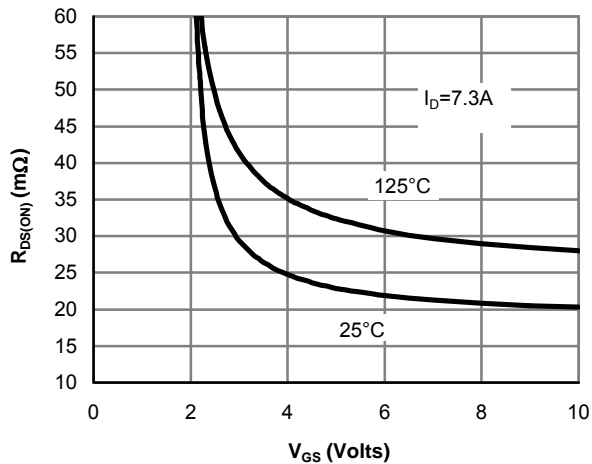


Figure 5: On-Resistance vs. Gate-Source Voltage

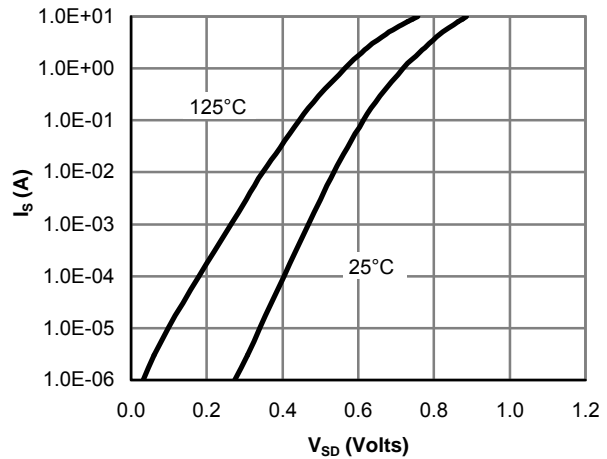


Figure 6: Body-Diode Characteristics

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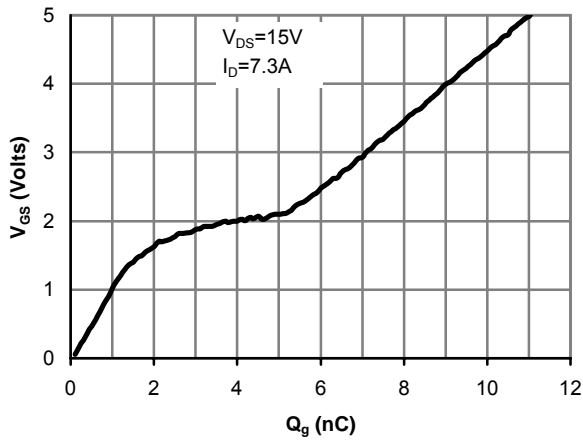


Figure 7: Gate-Charge Characteristics

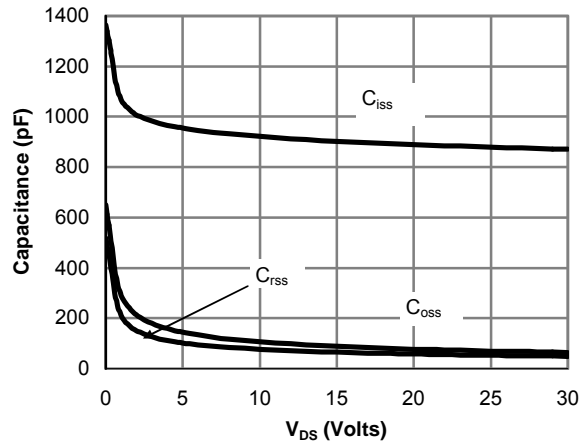


Figure 8: Capacitance Characteristics

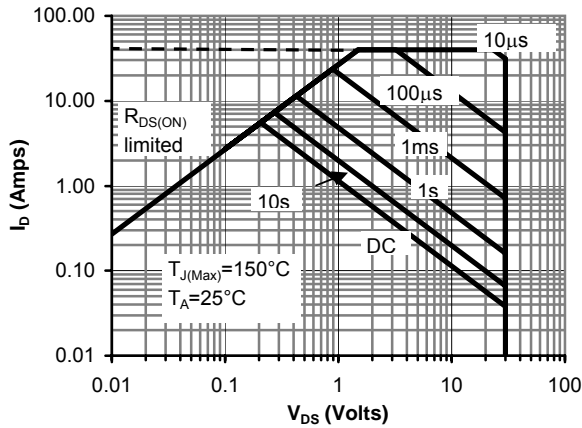


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

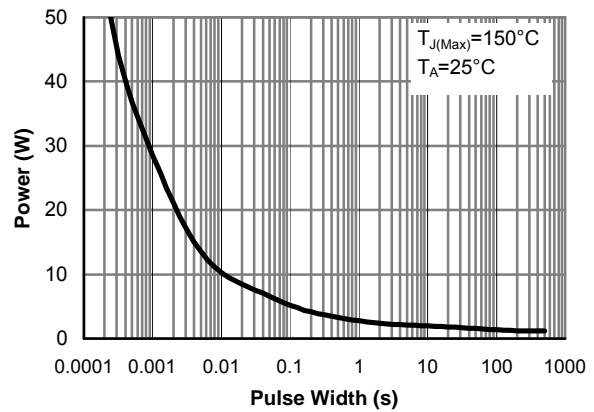


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

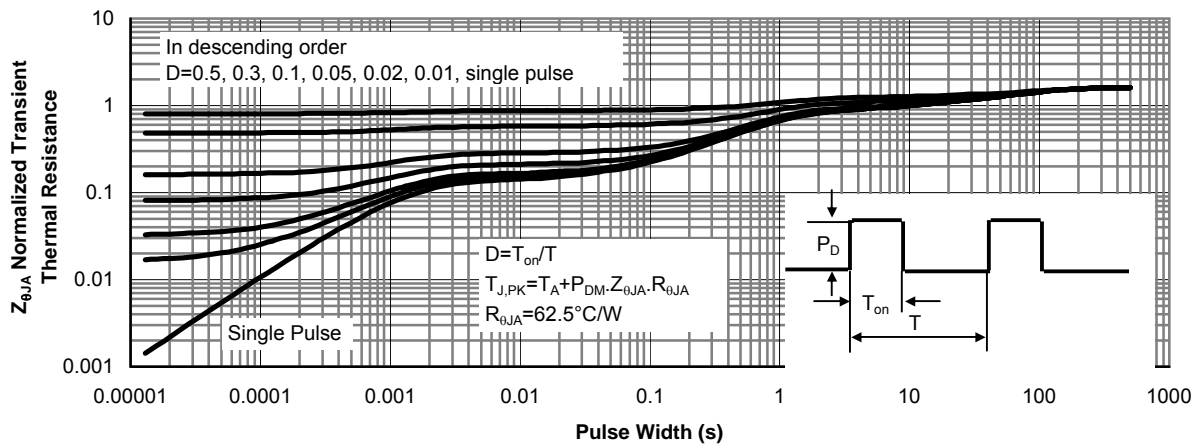


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)