TS8MED3260G

32MB 72-PIN EDO
SIMM With 16Mx8 3.3VOLT

Description

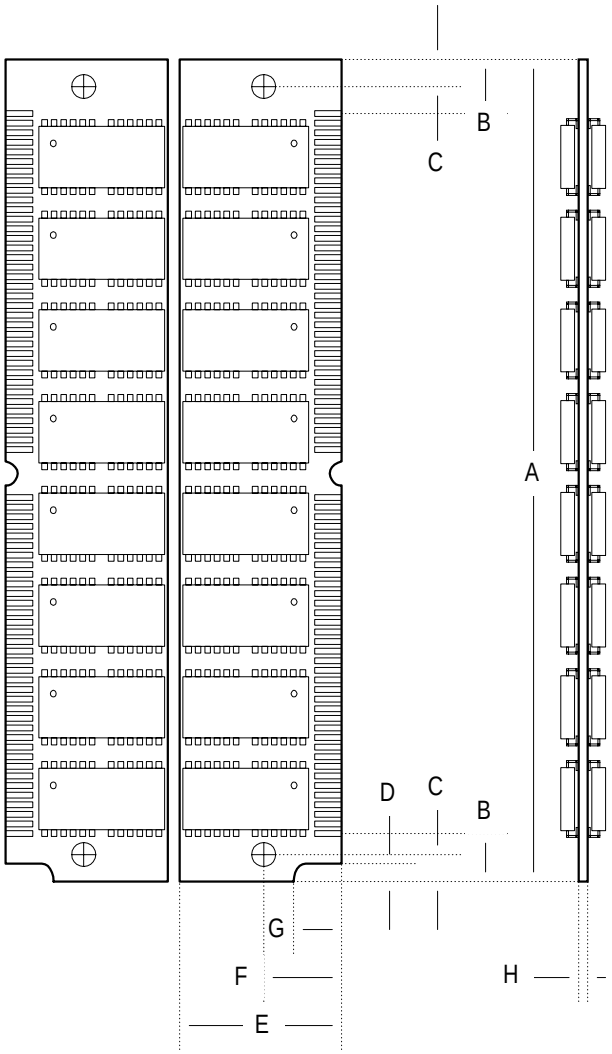
The TS8MED3260G is a 8M by 32-bit dynamic RAM module with 16 pcs of 4Mx4 DRAMs assembled on the printed circuit board.

The TS8MED3260G is optimized for application to systems which require high density and large capacity along with compact sizing.

Features

- Fast Page Mode with Extended Data Out
- Single +5.0V ± 10% power supply.
- 2,048 cycles refresh.
- Lower power consumption.
- CAS before RAS refresh, RAS only refresh, Hidden refresh, Fast Page Mode with EDO, Read_Modify_Write capability.
- DRAM Status : GM71C17403CJ-60
  M5M417405CJ-6
  NT5117405BJ-60
  HM5117405S-6

Placement

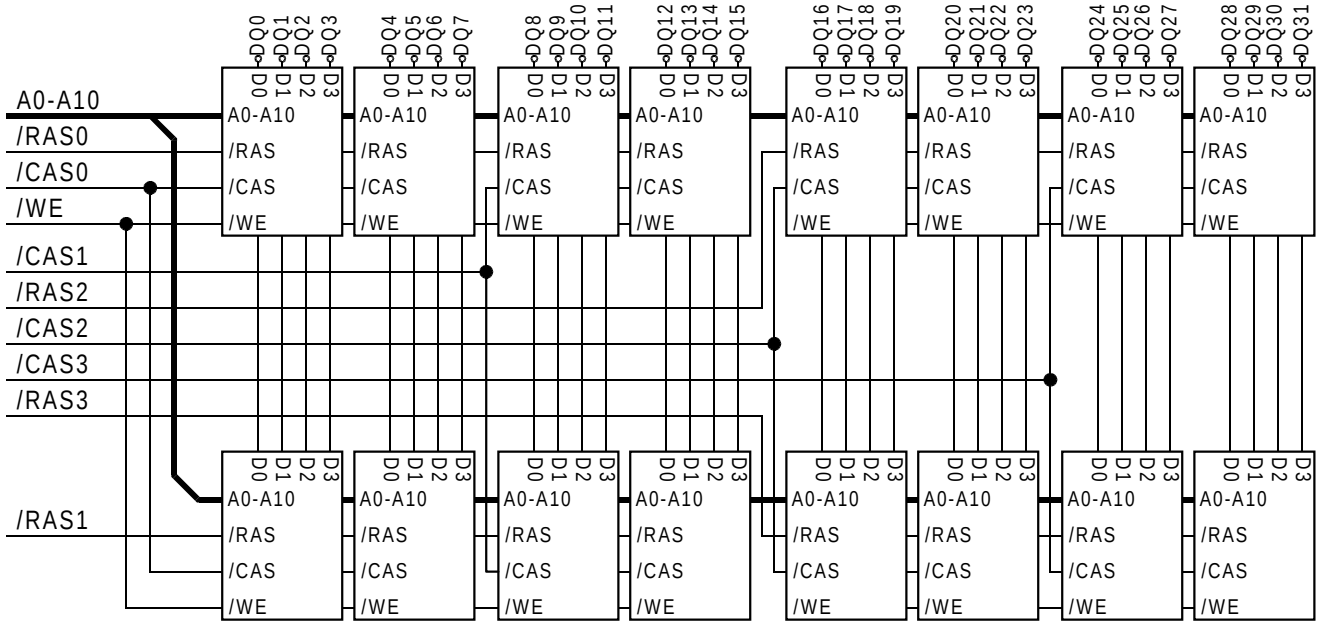


TS8MED3260G	
Access time from /RAS t_{RAC}	60ns
Access time from /CAS t_{CAC}	15ns
Random read/write cycle time t_{RC}	104ns
Hyper page mode cycle time t_{HPC}	25ns

Dimensions

Side	Millimeters	Inches
A	107.95 ± 0.500	4.520 ± 0.020
B	6.35	0.250
C	3.38	0.133
D	2.03	0.080
E	21.60 ± 0.500	0.850 ± 0.020
F	10.16	0.400
G	6.35	0.250
H	1.27 ± 0.080	0.050 ± 0.003

TS8MED3260G-- Block Diagram



Pinouts

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	25	DQ22	49	DQ8
02	DQ0	26	DQ7	50	DQ24
03	DQ16	27	DQ23	51	DQ9
04	DQ1	28	A7	52	DQ25
05	DQ17	29	NC	53	DQ10
06	DQ2	30	Vcc	54	DQ26
07	DQ18	31	A8	55	DQ11
08	DQ3	32	A9	56	DQ27
09	DQ19	33	/RAS3	57	DQ12
10	Vcc	34	/RAS2	58	DQ28
11	NC	35	NC	59	Vcc
12	A0	36	NC	60	DQ29
13	A1	37	NC	61	DQ13
14	A2	38	NC	62	DQ30
15	A3	39	Vss	63	DQ14
16	A4	40	/CAS0	64	DQ31
17	A5	41	/CAS2	65	DQ15
18	A6	42	/CAS3	66	NC
19	A10	43	/CAS1	67	PD1
20	DQ4	44	/RAS0	68	PD2
21	DQ20	45	/RAS1	69	PD3
22	DQ5	46	NC	70	PD4
23	DQ21	47	/WE	71	NC
24	DQ6	48	NC	72	Vss

Pin Identification

Symbol	Function
A0 ~ A10	Address inputs
DQ0 ~ DQ31	Common data inputs/outputs
/RAS0 ~ /RAS3	Row address strobes
/CAS0 ~ /CAS3	Column address strobes
/WE	Write enable
Vcc	+5.0 Volt power supply
Vss	Ground
NC	No connection
PD1 ~ PD4	Presence detection pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0~+7.0	V
Voltage on V_{CC} supply to Vss	V_{CC}	-1.0~+7.0	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss , T_A = 0 to 70℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	-	Vcc+1*[1]	V
Input low voltage	V_{IL}	-1.0*[2]	-	0.8	V

Note: 1. V_{CC} +2.0V/20ns, Pulse width is, measured at V_{CC} .
2. -2.0V/20ns, Pulse width is measured at V_{CC}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Min	Max	Unit
I_{CC1}	-	816	mA
I_{CC2}	-	32	mA
I_{CC3}	-	816	mA
I_{CC4}	-	816	mA
I_{CC5}	-	16	mA
I_{CC6}	-	816	mA
$I_{I(L)}$	-80	80	uA
$I_{O(L)}$	-10	10	uA
V_{OH}	2.4	-	V
V_{OL}	-	0.4	V

I_{CC1}: Operating Current* (/RAS, /CAS, Address cycling @t_{RC}=min)
I_{CC2}: Standby Current (/RAS=/CAS=/W=V_{IH})

I_{CC3}: /RAS only Refresh Current* (/CAS=V_{IH}, /RAS cycling @t_{RC}=min)
I_{CC4}: Fast Page Mode Current* (/RAS=V_{IL}, /CAS Address cycling: t_{PC}=min)
I_{CC5}: Standby Current (/RAS=/CAS=/W=VCC-0.2V)
I_{CC6}: /CAS-Before-/RAS Refresh Current* (/RAS and /CAS cycling @t_{RC}=min)
$I_{I(L)}$: Input Leakage Current (Any input 0≦VIN≦V_{CC}+0.5V, all other pins not under test=0V)
$I_{O(L)}$: **Output Leakage Current (Data Out is disabled, 0V**≦V_{OUT}≦V_{CC})
V_{OH}: Output High Voltage Level (I_{OH}= -5mA)
V_{OL}: Output Low Voltage Level (I_{OL}=4.2mA)

Note: **I_{CC1}**, **I_{CC3}**, **I_{CC4}** and **I_{CC6}** are dependent on output loading and cycle rates. Specified values are obtained with the output open. **I_{CC}** is specified as an average current. In **I_{CC1}** and **I_{CC3}**, address can be changed maximum once while /RAS=V_{IL}. In **I_{CC4}**, address can be changed maximum once within one mode cycle, t_{PC}.

CAPACITANCE (TA = 25°C, Vcc = 5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance (A_0~A_{10})	C_{IN1}	-	100	pF
Input capacitance (/WE)	C_{IN2}	-	130	pF
Input capacitance (/RAS0, /RAS2)	C_{IN3}	-	35	pF
Input capacitance (/CAS0~/CSA3)	C_{IN4}	-	30	pF
Data input/output capacitance (DQ0~DQ31)	C_{DQ}	-	20	pF

AC CHARACTERISTICS (0℃≦TA≦70℃, Vcc=5.0V±10%, See notes 1, 2)

Test condition: V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.4V/0.4V, Output loading CL=100pF

Parameter	Symbol	Min	Max	Unit	Note
Random read or write cycle time	t_{RC}	110		ns	
Access time from /RAS	t_{RAC}		60	ns	3,4
Access time from /CAS	t_{CAC}		15	ns	3,4,5
Access time from column address	t_{CLZ}		30	ns	3,10
/CAS to output in Low-Z	t_{RC}	0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	ns	6
Transition time (rise and fall)	t_T	3	50	ns	2
/RAS precharge time	t_{RP}	40		ns	
/RAS pulse width	t_{RAS}	60	10K	ns	
/RAS hold time	t_{RSH}	15		ns	
/CAS hold time	t_{CSH}	60		ns	
/CAS pulse width	t_{CAS}	10	10K	ns	
/RAS to /CAS delay time	t_{RCD}	20	45	ns	4

/RAS to column address delay time	tRAD	15	30	ns	10
/CAS to /RAS precharge time	tCRP	5		ns	
Row address set-up time	tASR	0		ns	
Row address hold time	tRAH	10		ns	
Column address set-up time	tASC	0		ns	
Column address hold time	tCAH	10			
Column address to /RAS lead time	tRAL	30			
Read command set-up time	tRCS	0		ns	
Read command hold referenced to /CAS	tRCH	0		ns	8
Read command hold referenced to /RAS	tRRH	0		ns	8
Write command hold time	tWCH	10		ns	
Write command pulse width	tWP	10		ns	
Write command to /RAS lead time	tRWL	15		ns	
Write command to /CAS lead time	tCWL	10		ns	
Date-in set-up time	tDS	0		ns	9
Date-in hold time	tDH	10		ns	9
Refresh period	tREF		32	ns	
Write command set-up time	tWCS	0		ns	7
/CAS setup time (/CAS-before-/RAS referesh)	tCSR	5		ns	
/CAS hold time (/CAS-before-/RAS referesh)	tCHR	10		ns	
/RAS precharge to /CAS hold time	tRPC	5		ns	
Access time from /CAS precharge	tCPA		35	ns	3
Fast page mode cycle time	tPC	40		ns	
/CAS precharge time (Fast page cycle)	tCP	10		ns	
/RAS pulse width (Fast page cycle)	tRASP	60	200K	ns	
/W to /RAS precharge time (C-B-R refresh)	tWRP	10		ns	
/W to /RAS hold time (C-B-R refresh)	tWRH	10		ns	
/CAS precharge (C-B-R counter test)	tCPT	20		ns	
Hold time /CAS low to /CAS high	tCLCH	5		ns	11

Note: 1. An initial pause of 200us is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.

2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. tWCS is non-restrictive operating parameter. It included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are refernced to the /CAS leading edge in early write cycle.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be me. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. In order to hold the address latched by the first /CAS going low, the parameter Tclch must be met.