

FEATURES

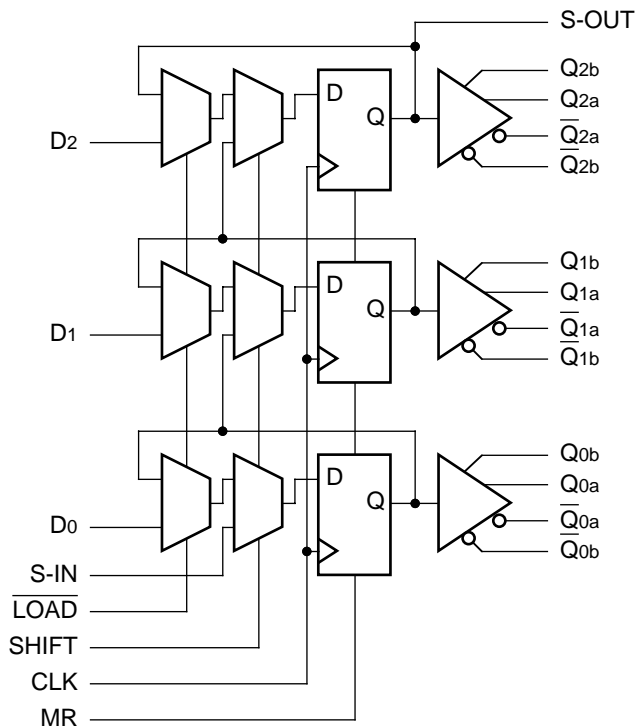
- Scannable version E112 driver
- Extended 100E VEE range of -4.2V to -5.5V
- 1025ps max. CLK to Output
- Dual differential outputs
- Master Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with industry standard 10KH, 100K ECL levels
- Fully compatible with Motorola MC10E/100E212
- Available in 28-pin PLCC package

DESCRIPTION

The SY10/100E212 are scannable registered ECL drivers typically used as fan-out memory address drivers for ECL cache driving. In a VLSI array-based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

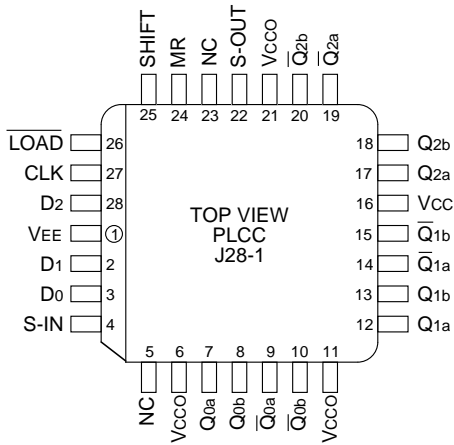
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D0 – D2	Data Inputs
S-IN	Scan Input
LOAD	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Master Reset
S-OUT	Scan Output
Q[0:2]a, Q[0:2]b	True Outputs
\overline{Q} [0:2]a, \overline{Q} [0:2]b	Inverting Outputs
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E212JC	J28-1	Commercial	SY10E212JC	Sn-Pb
SY10E212JCTR ⁽²⁾	J28-1	Commercial	SY10E212JC	Sn-Pb
SY100E212JC	J28-1	Commercial	SY100E212JC	Sn-Pb
SY100E212JCTR ⁽²⁾	J28-1	Commercial	SY100E212JC	Sn-Pb
SY10E212JZ ⁽³⁾	J28-1	Commercial	SY10E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E212JZTR ^(2, 3)	J28-1	Commercial	SY10E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E212JZ ⁽³⁾	J28-1	Commercial	SY100E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E212JZTR ^(2, 3)	J28-1	Commercial	SY100E212JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE

$\overline{\text{LOAD}}$	SHIFT	MR	Mode
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	10E	80	96	—	80	96	—	80	96	mA	—
		100E	80	96	—	80	96	—	92	110		

AC ELECTRICAL CHARACTERISTICS

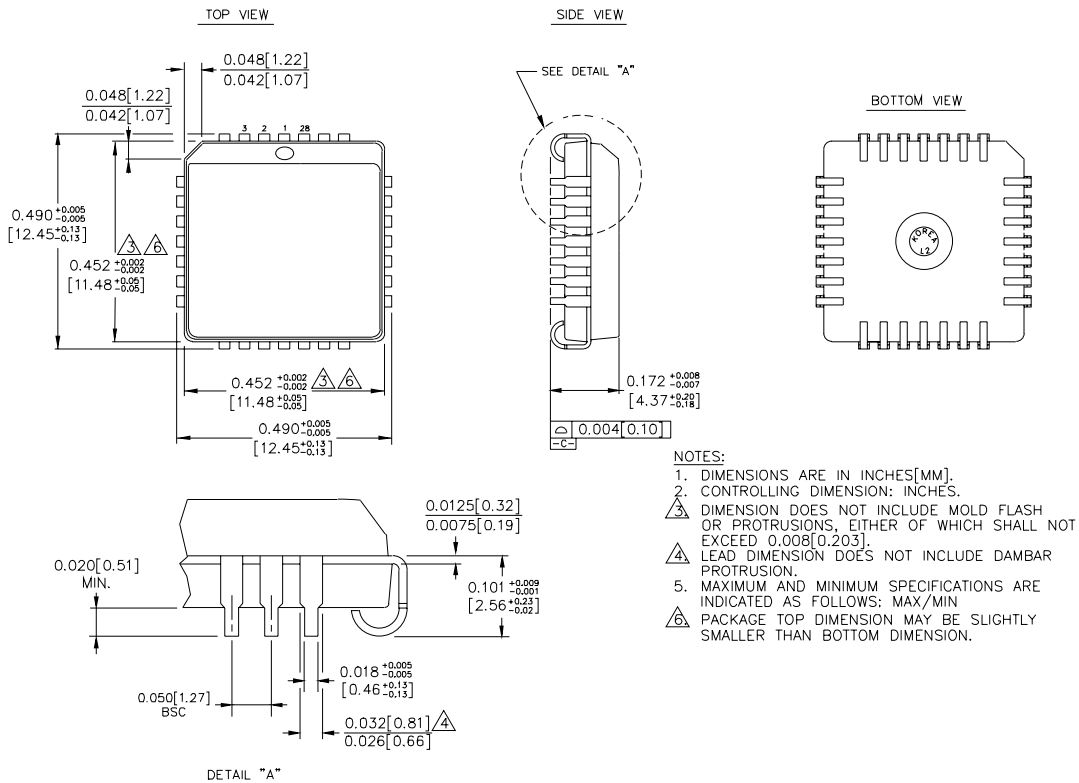
VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PD}	Propagation Delay to Output	575	800	1025	575	800	1025	575	800	1025	ps	—
	CLK	575	800	1025	575	800	1025	575	800	1025		
	MR	575	800	1025	575	800	1025	575	800	1025		
t _s	Set-up Time	175	25	—	175	25	—	175	25	—	ps	—
	D	150	-50	—	150	-50	—	150	-50	—		
	SHIFT	225	50	—	225	50	—	225	50	—		
	LOAD	150	-50	—	150	-50	—	150	-50	—		
t _H	Hold Time	250	25	—	250	25	—	250	25	—	ps	—
	D	300	100	—	300	100	—	300	100	—		
	SHIFT	225	0	—	225	0	—	225	0	—		
	LOAD	300	100	—	300	100	—	300	100	—		
t _{RR}	Reset Recovery	600	350	—	600	350	—	600	350	—	ps	—
t _{skew}	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	1
t _{skew}	Within-Gate Skew	—	50	—	—	50	—	—	50	—	ps	2
t _r t _f	Rise/Fall Times 20% to 80%	275	425	650	275	425	650	275	425	650	ps	—

Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

28-PIN PLCC (J28-1)



Rev. 03

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