

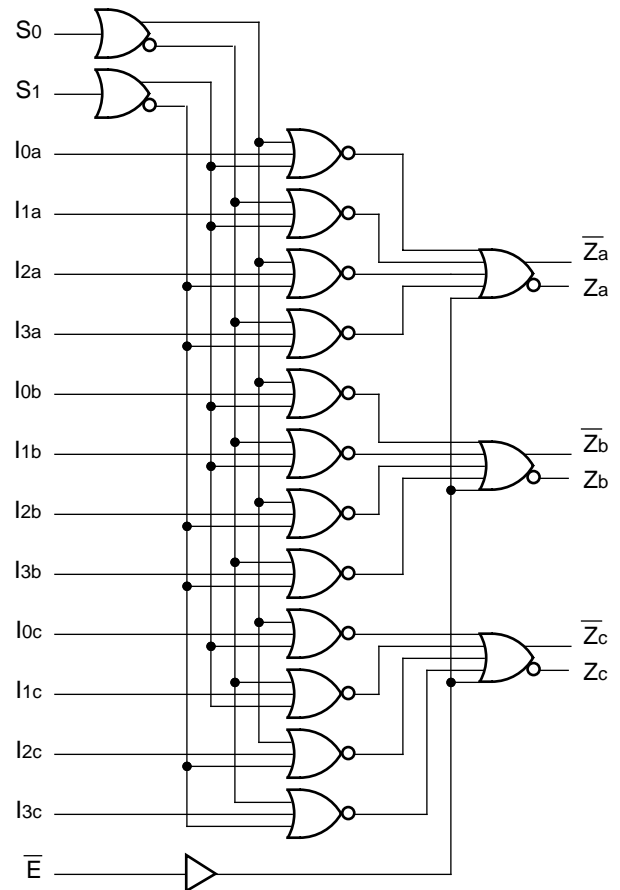
FEATURES

- Max. propagation delay of 1000ps
- IEE min. of -68mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 40% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S371 is an ultra-fast triple 4-input multiplexer with true and complementary outputs designed for use in high-performance ECL systems. The multiplexer is controlled by common select inputs S0 and S1. A logic HIGH on the Enable (\bar{E}) control input takes the outputs to a logic LOW. The inputs on the device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



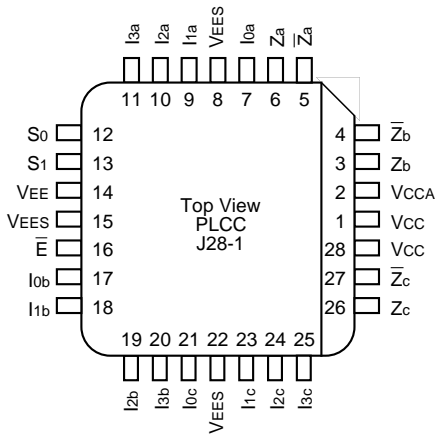
PACKAGE/ORDERING INFORMATION

Ordering Information

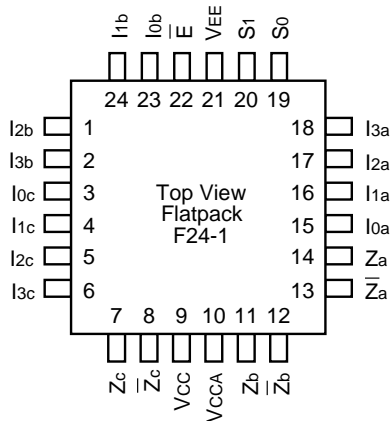
Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S371FC	F24-1	Commercial	SY100S371FC	Sn-Pb
SY100S371FCTR ⁽¹⁾	F24-1	Commercial	SY100S371FC	Sn-Pb
SY100S371JJC	J28-1	Commercial	SY100S371JJC	Sn-Pb
SY100S371JCTR ⁽¹⁾	J28-1	Commercial	SY100S371JJC	Sn-Pb
SY100S371JZ ⁽²⁾	J28-1	Commercial	SY100S371JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S371JZTR ^(1, 2)	J28-1	Commercial	SY100S371JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

PIN NAMES

Pin	Function
I _{0X} – I _{3X}	Data Inputs (x = a, b or c)
S ₀ , S ₁	Select Inputs
\bar{E}	Enable Input (Active LOW)
Z _a – Z _c	Data Outputs
\bar{Z}_a – \bar{Z}_c	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

TRUTH TABLE⁽¹⁾

Inputs			Outputs
\bar{E}	S ₀	S ₁	Z _n
L	L	L	I _{0X}
L	H	L	I _{1X}
L	L	H	I _{2X}
L	H	H	I _{3X}
H	X	X	L

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS

VEE = –4.2V to –5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current I _{0X} – I _{3X} S ₀ , S ₁ , \bar{E}	—	—	250 300	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	–68	–48	–34	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

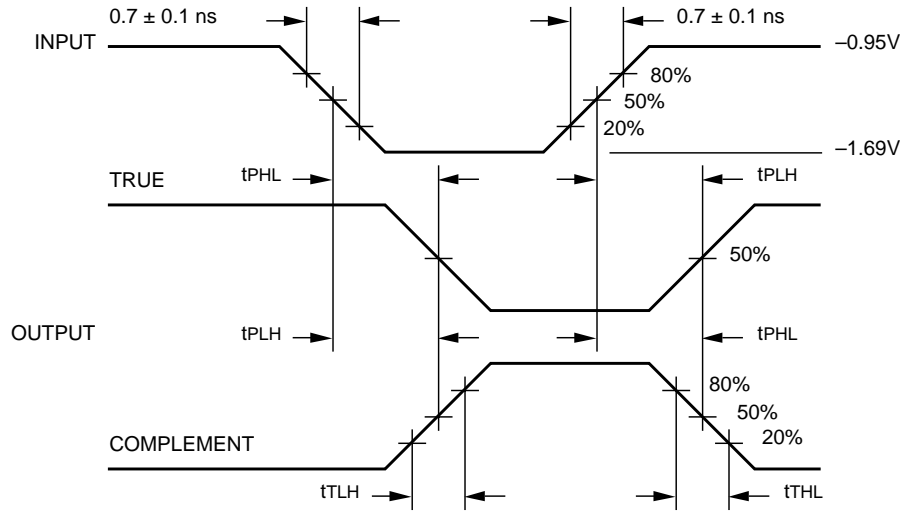
Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay I _{OX} – I _{3X} to Output	300	1100	300	1100	300	1100	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1500	400	1500	400	1500	ps	
tPLH tPHL	Propagation Delay \bar{S}_0 , S ₁ to Output	400	1400	400	1400	400	1400	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay I _{OX} – I _{3X} to Output	300	1000	300	1000	300	1000	ps	
tPLH tPHL	Propagation Delay S ₀ , S ₁ to Output	400	1400	400	1400	400	1400	ps	
tPLH tPHL	Propagation Delay \bar{S}_0 , S ₁ to Output	400	1300	400	1300	400	1300	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM

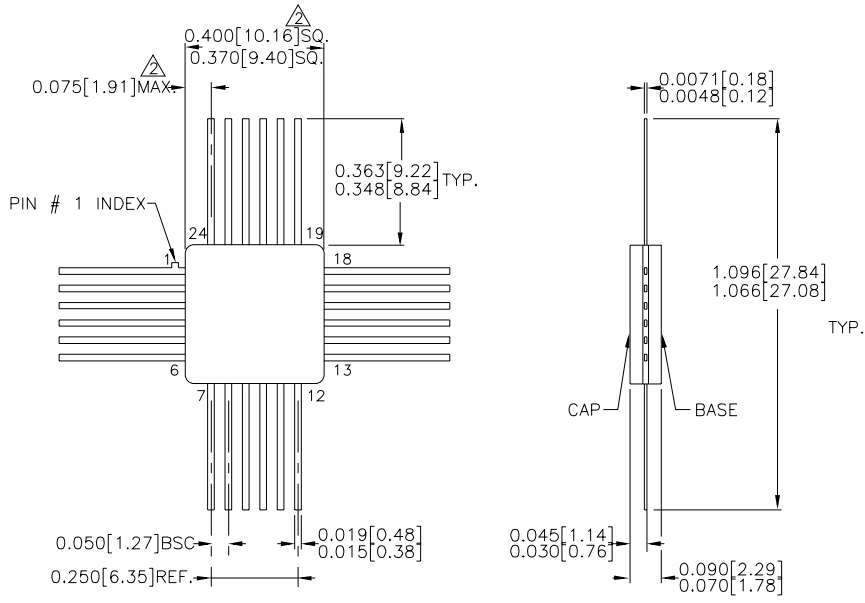


Propagation Delay and Transition Times

Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

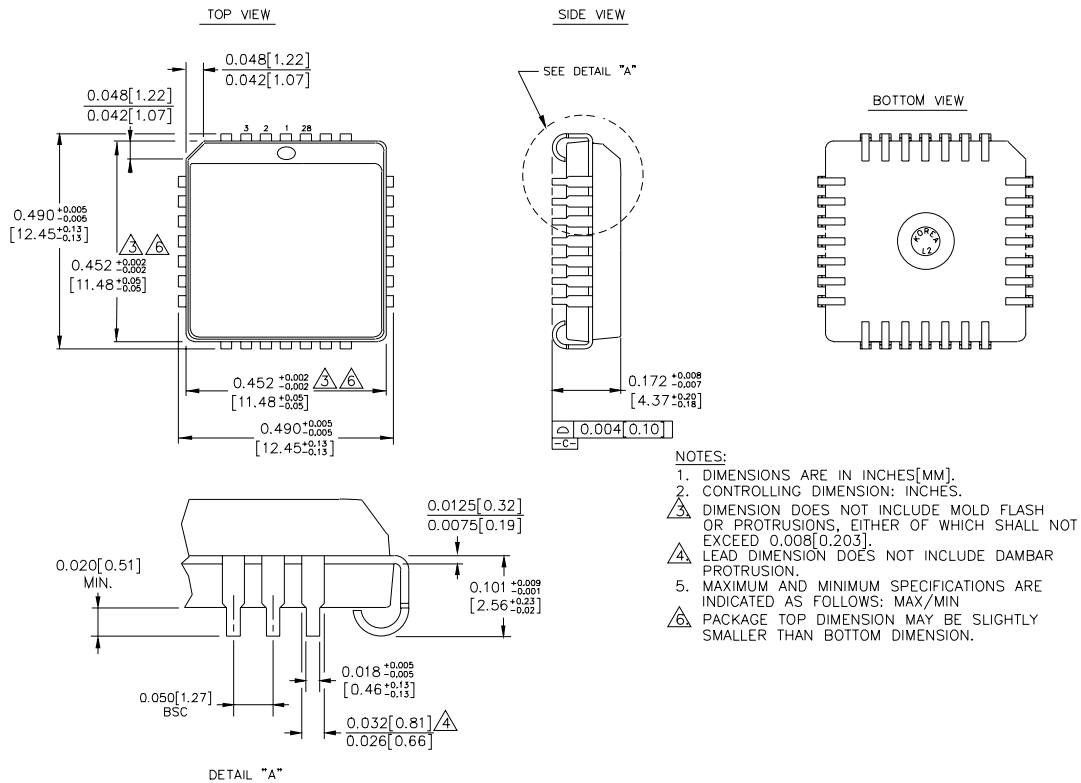
24-PIN CERPACK (F24-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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