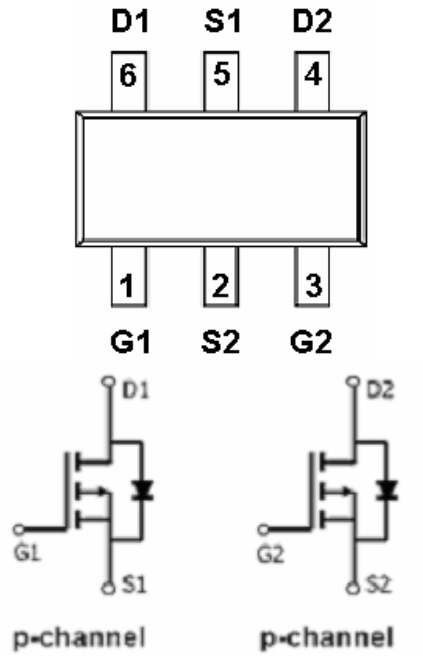
SPP6507
Dual P-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPP6507 is the Dual P-Channel enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching , low in-line power loss, and resistance to transients are needed.

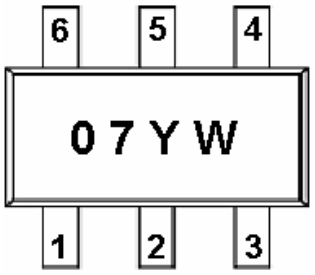
APPLICATIONS
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES
- P-Channel
  -30V/-2.8A,$R_{DS(ON)}$=105mΩ@V_{GS}=- 10V
  -30V/-2.5A,$R_{DS(ON)}$=115mΩ@V_{GS}=-4.5V
  -30V/-1.5A,$R_{DS(ON)}$=150mΩ@V_{GS}=-2.5V
  -30V/-1.0A,$R_{DS(ON)}$=215mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)



PART MARKING



Y : Year Code
W : Week Code

SPP6507
Dual P-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G1	Gate 1
2	S2	Source 2
3	G2	Gate 2
4	D2	Drain 2
5	S1	Source 1
6	D1	Drain1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP6507S26RG	SOT-23- 6L	07YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP6507S26RG : Tape Reel ; Pb – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

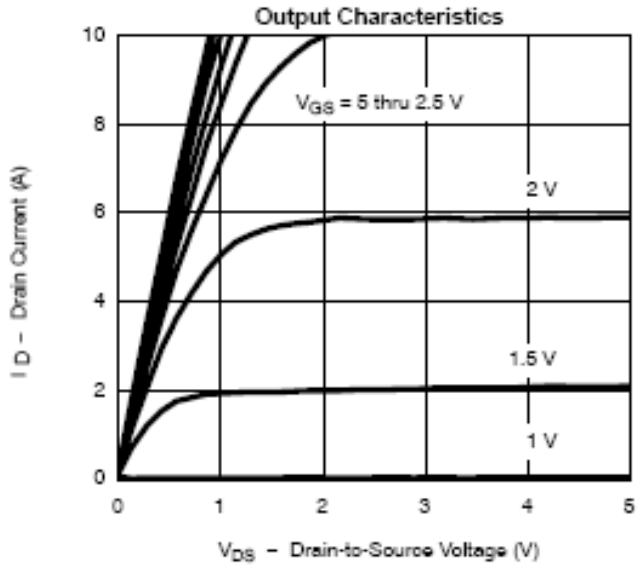
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-2.8	A
	T_A=70℃		-2.1	
Pulsed Drain Current		I_{DM}	-8	A
Continuous Source Current(Diode Conduction)		I_S	-1.4	A
Power Dissipation	T_A=25℃	P_D	1.15	W
	T_A=70℃		0.75	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient	T ≤ 10sec	$R_{\theta JA}$	52	℃/W
	Steady State		100	

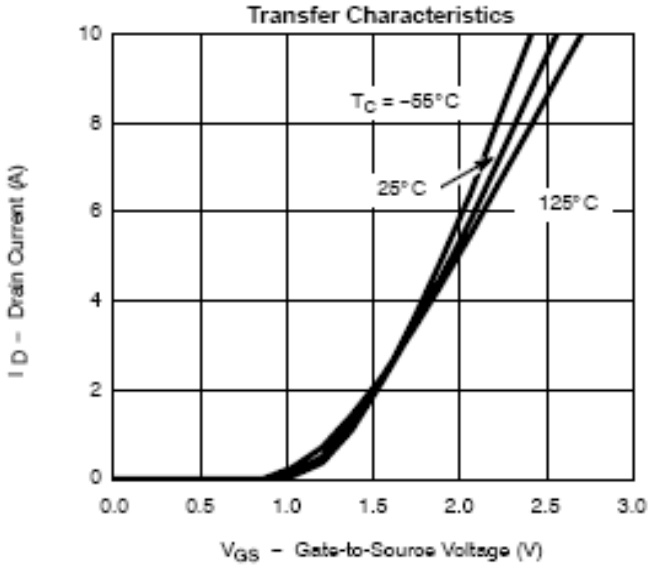
ELECTRICAL CHARACTERISTICS

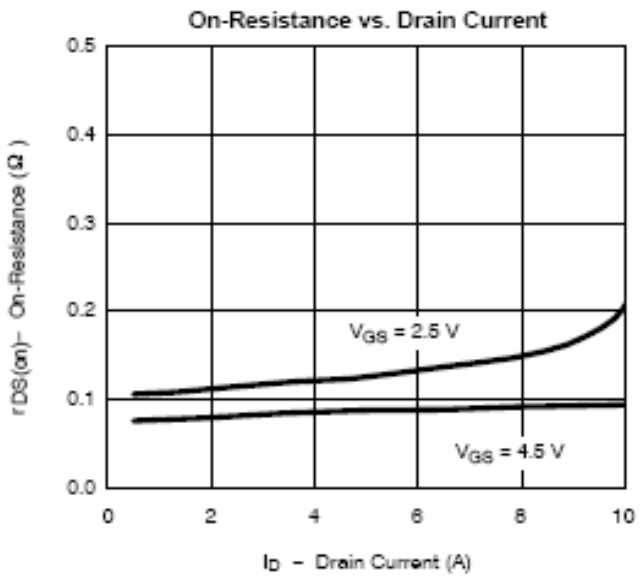
(T_A=25℃ Unless otherwise noted)

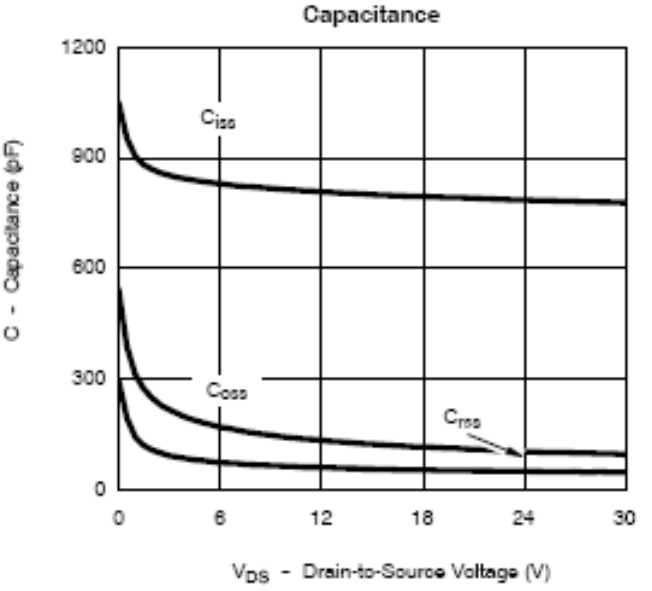
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-10uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.4		-1.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}= -5V,V_{GS} =-4.5V	-4			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-2.8A		0.085	0.105	Ω
		V_{GS}=-4.5V,I_D=-2.5A		0.100	0.115	
		V_{GS}=-2.5V,I_D=-1.5A		0.135	0.150	
		V_{GS}=-1.8V,I_D=-1.0A		0.185	0.215	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-2.8A		4.0		S
Diode Forward Voltage	V_{SD}	I_S=-1.2A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V ,V_{GS}=-4.5V I_D≡-2.0A		5.8		nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	V_{DS}=-15V ,V_{GS}=0V f=1MHz		380		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V ,R_L=15Ω I_D≡-1.0A ,V_{GEN}=-10V R_G=3Ω		6		ns
	t_r			3.9		
Turn-Off Time	$t_{d(off)}$			40		
	t_f			15		

TYPICAL CHARACTERISTICS

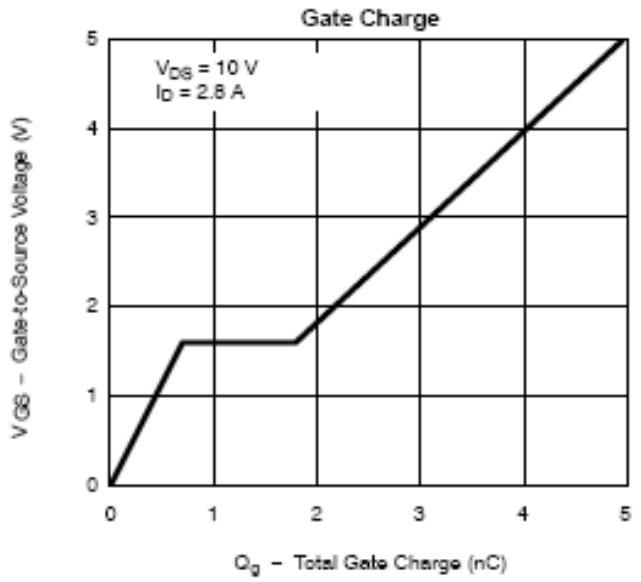


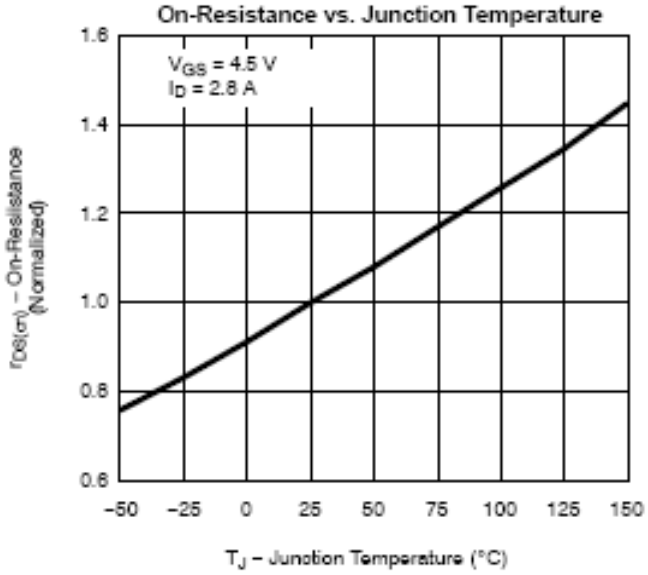


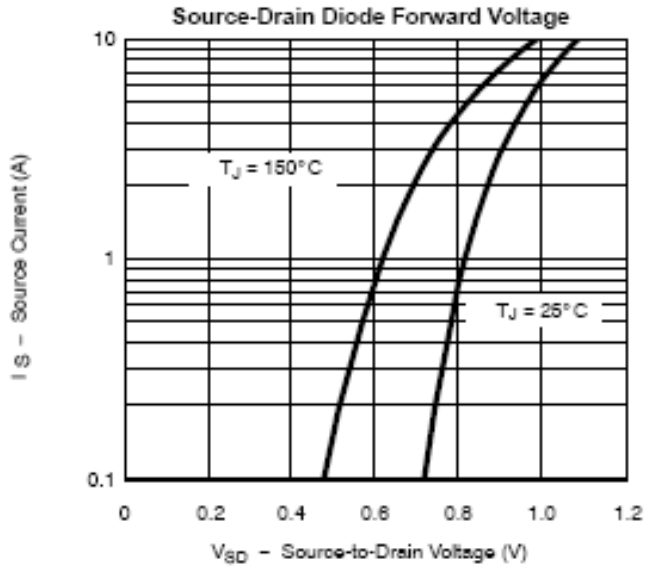


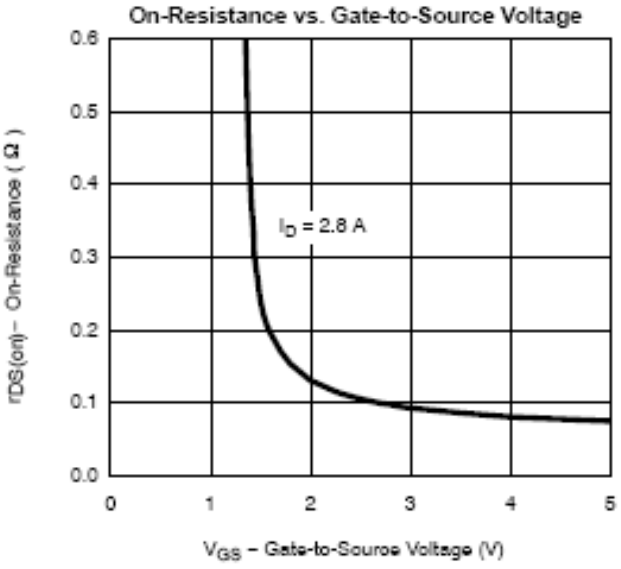


TYPICAL CHARACTERISTICS









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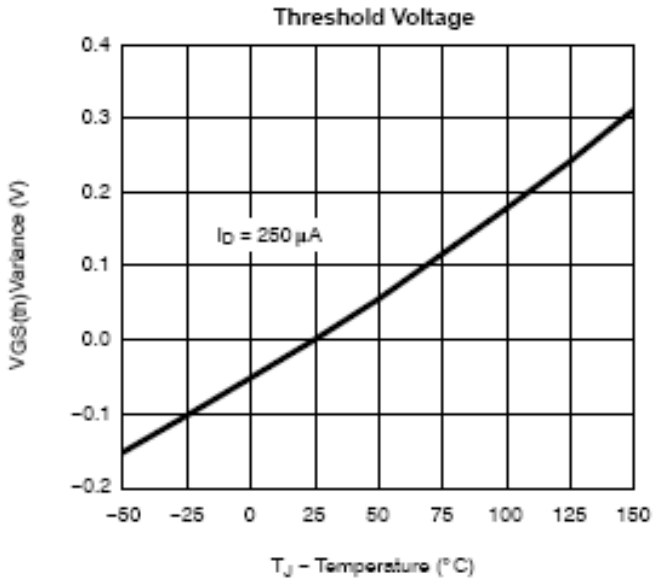
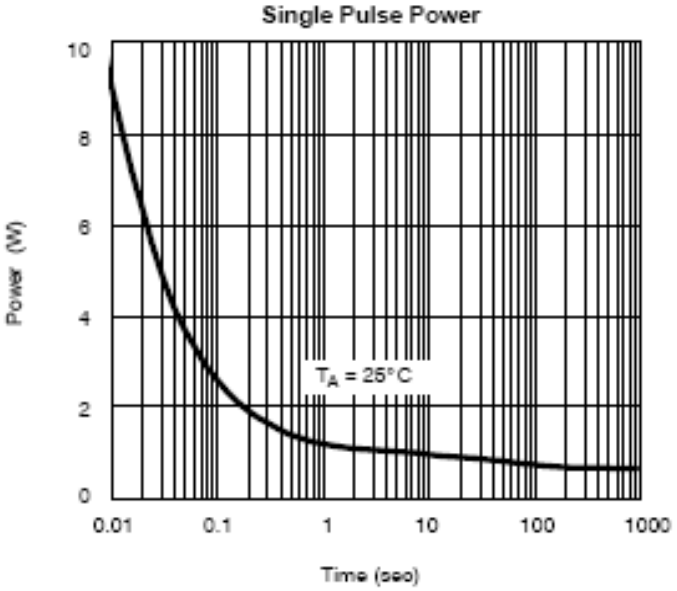
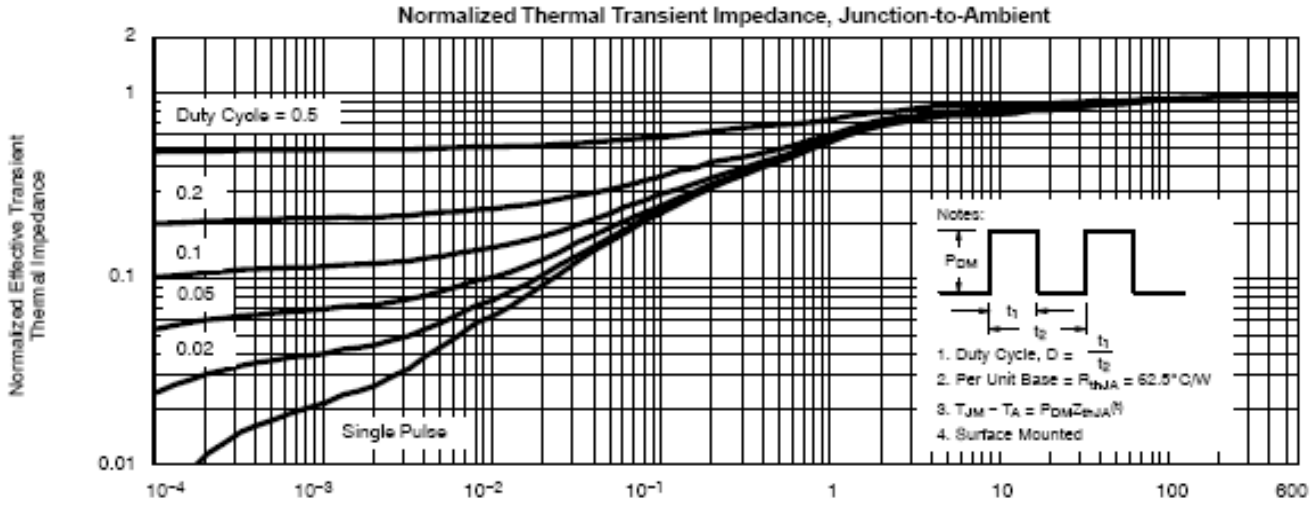
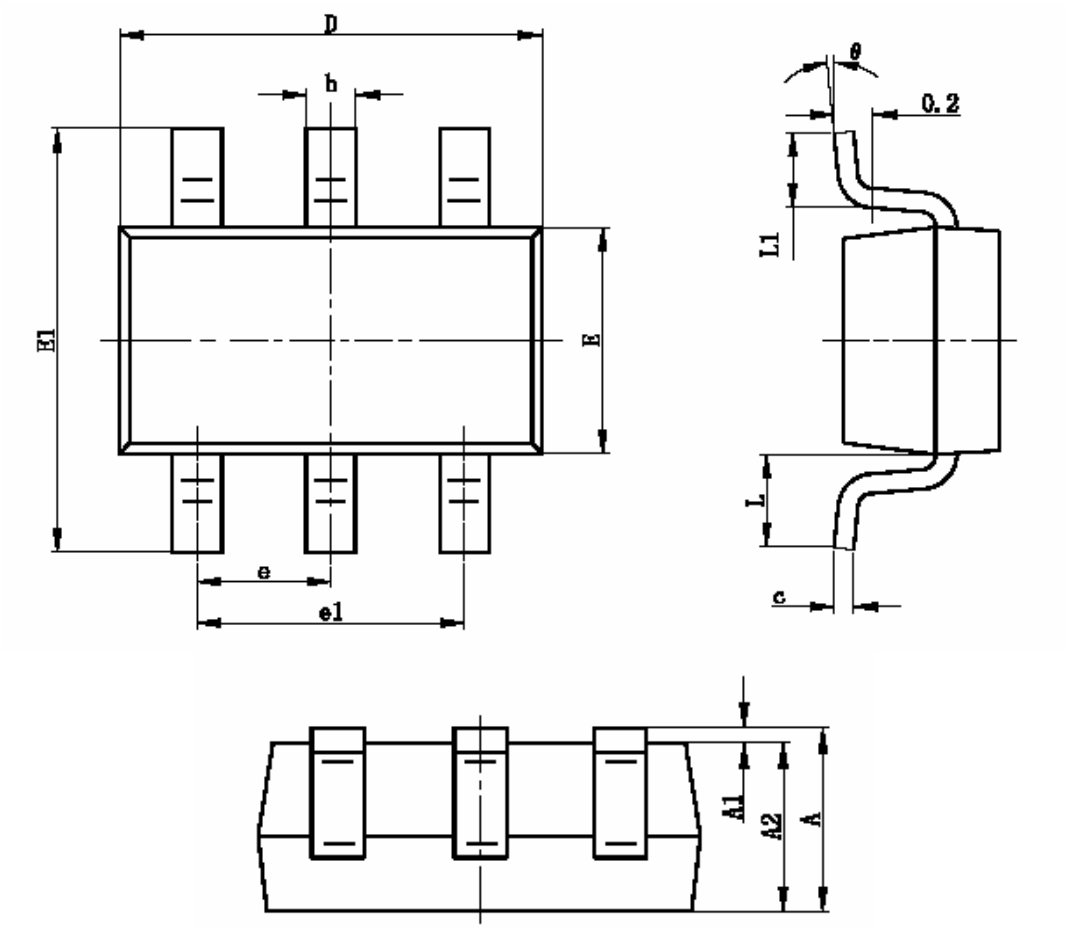






SOT-23-6L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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