4V Drive Nch+Pch MOSFET

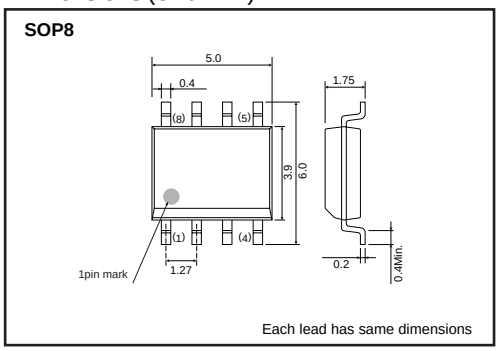
SP8M21

●Structure
Silicon N-channel MOSFET /
Silicon P-channel MOSFET

●Features
1) Low on-resistance.
2) Built-in G-S protection diode.
3) Small and surface mount package (SOP8).

●Applications
Switching

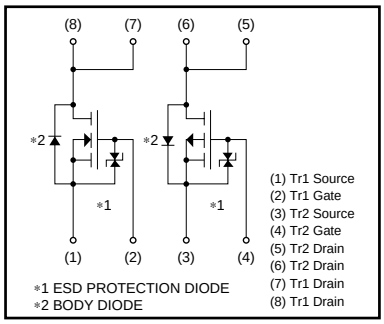
●Dimensions (Unit : mm)



●Package specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M21		○

●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	45	−45	V
Gate-source voltage		V_{GSS}	20	−20	V
Drain current	Continuous	I_D	±6.0	±4.0	A
	Pulsed	I_{DP}∗1	±24	±16	A
Source current (Body diode)	Continuous	I_S	1.0	−1.0	A
	Pulsed	I_{SP}∗1	24	−16	A
Total power dissipation		P_D∗2	2.0		W / TOTAL
			1.4		W / ELEMENT
Channel temperature		Tch	150		°C
Storage temperature		Tstg	−55 to +150		°C

∗1 Pw≤10µs, Duty cycle≤1%
∗2 Mounted on a ceramic board.

N-ch

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	10	μA	V_{GS}=20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	45	–	–	V	I_D= 1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}= 45V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	–	2.5	V	V_{DS}= 10V, I_D= 1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	–	18	25	mΩ	I_D= 6.0A, V_{GS}= 10V
		–	24	34	mΩ	I_D= 6.0A, V_{GS}= 4.5V
		–	26	37	mΩ	I_D= 6.0A, V_{GS}= 4.0V
Forward transfer admittance	$\|Y_{fs}\|$ *	6.0	–	–	S	V_{DS}= 10V, I_D= 6.0A
Input capacitance	C_{iss}	–	1400	–	pF	V_{DS}= 10V
Output capacitance	C_{oss}	–	310	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	175	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	19	–	ns	V_{DD}≒ 25V
Rise time	t_r *	–	30	–	ns	I_D= 3.0A
Turn-off delay time	$t_{d\ (off)}$ *	–	72	–	ns	V_{GS}= 10V R_L= 8Ω
Fall time	t_f *	–	27	–	ns	R_G=10Ω
Total gate charge	Q_g *	–	15.4	21.6	nC	V_{DD}≒ 25V, V_{GS}= 5V
Gate-source charge	Q_{gs} *	–	3.7	–	nC	I_D= 6.0A
Gate-drain charge	Q_{gd} *	–	6.5	–	nC	R_L= 4Ω, R_G= 10Ω

*Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}*	–	–	1.2	V	I_S= 6.0A, V_{GS}=0V

*Pulsed

P-ch

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	–10	μA	V_{GS}= –20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–45	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –45V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–1.0	–	–2.5	V	V_{DS}= –10V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	–	33	46	mΩ	I_D= –4.0A, V_{GS}= –10V
		–	43	60	mΩ	I_D= –4.0A, V_{GS}= –4.5V
		–	47	65	mΩ	I_D= –4.0A, V_{GS}= –4.0V
Forward transfer admittance	$\|Y_{fs}\|$ *	6.0	–	–	S	V_{DS}= –10V, I_D= –4.0A
Input capacitance	C_{iss}	–	2400	–	pF	V_{DS}= –10V
Output capacitance	C_{oss}	–	320	–	pF	V_{GS}= 0V
Reverse transfer capacitance	C_{rss}	–	200	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	23	–	ns	V_{DD}≒ –25V
Rise time	t_r *	–	23	–	ns	I_D= –2.0A
Turn-off delay time	$t_{d\ (off)}$ *	–	90	–	ns	V_{GS}= –10V
Fall time	t_f *	–	22	–	ns	R_L= 12.5Ω R_G= 10Ω
Total gate charge	Q_g *	–	20.0	28.0	nC	V_{DD}≒ –25V, V_{GS}= –5V
Gate-source charge	Q_{gs} *	–	6.5	–	nC	I_D= –4.0A
Gate-drain charge	Q_{gd} *	–	7.5	–	nC	R_L= 6Ω, R_G= 10Ω

*Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}*	–	–	–1.2	V	I_S= –4.0A, V_{GS}=0V

*Pulsed

N-ch

●Electrical characteristic curves

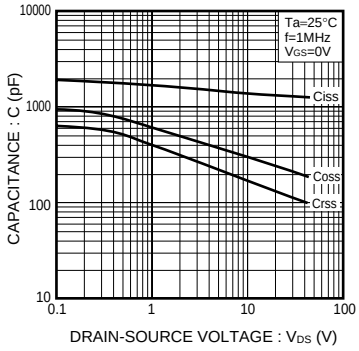


Fig.1 Typical Capacitance vs. Drain-Source Voltage

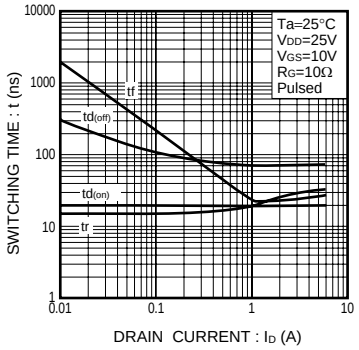


Fig.2 Switching Characteristics

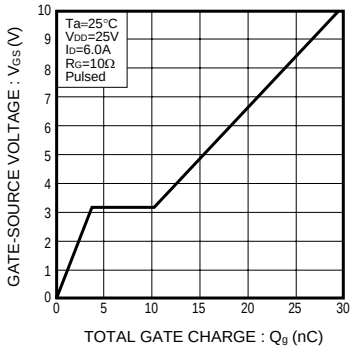


Fig.3 Dynamic Input Characteristics

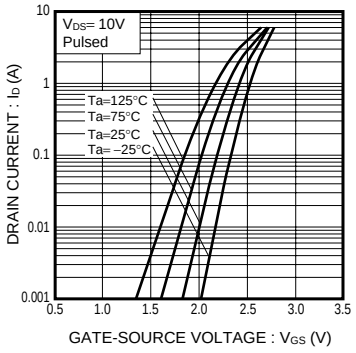


Fig.4 Typical Transfer Characteristics

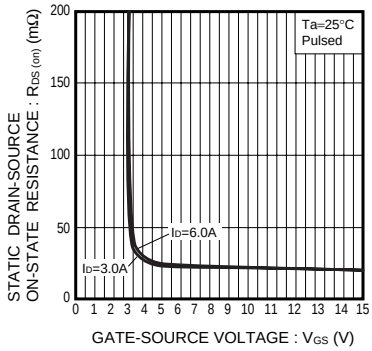


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

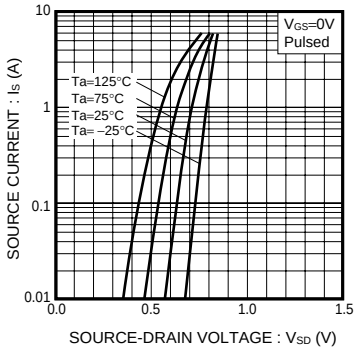


Fig.6 Source Current vs. Source-Drain Voltage

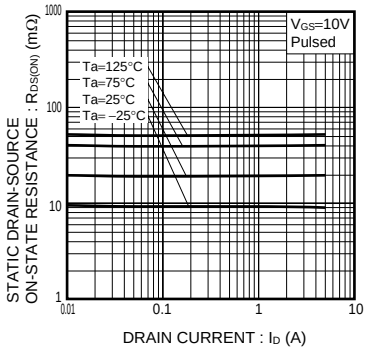


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

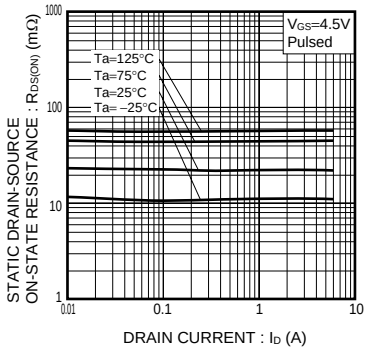


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

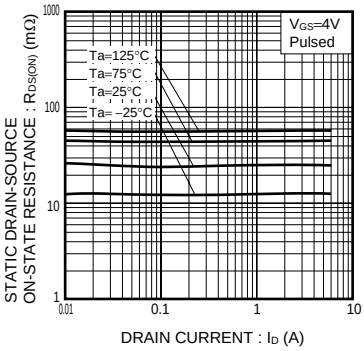


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

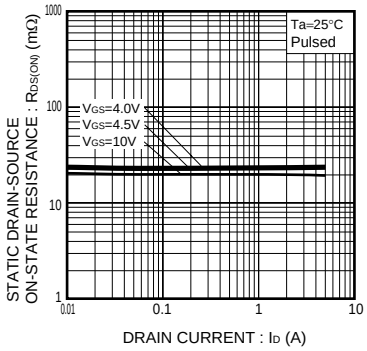


Fig.10 Static Drain-Source On-State Resistance vs. Drain Current (Ⅳ)

P-ch

●Electrical characteristic curves

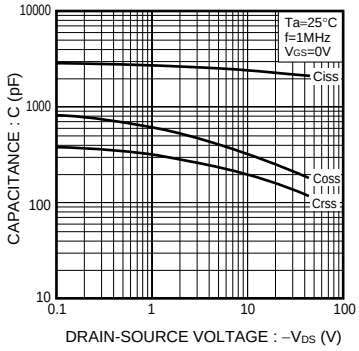


Fig.1 Typical Capacitance vs. Drain-Source Voltage

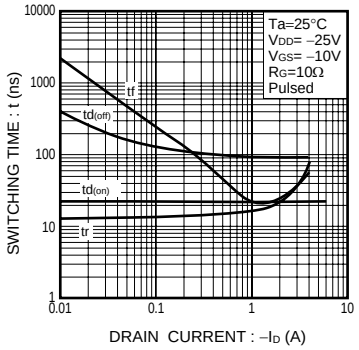


Fig.2 Switching Characteristics

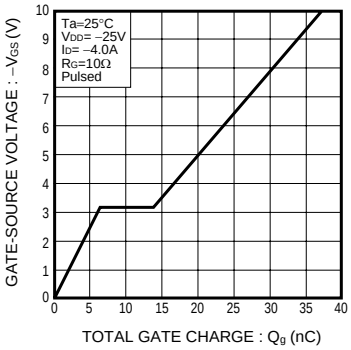


Fig.3 Dynamic Input Characteristics

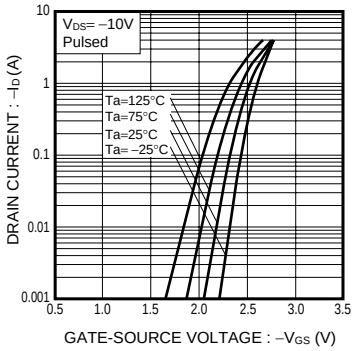


Fig.4 Typical Transfer Characteristics

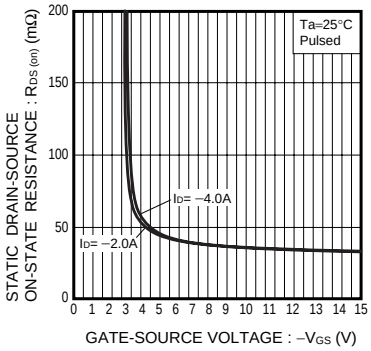


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

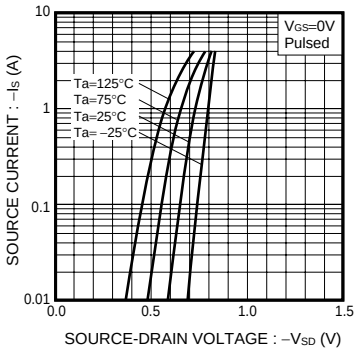


Fig.6 Source Current vs. Source-Drain Voltage

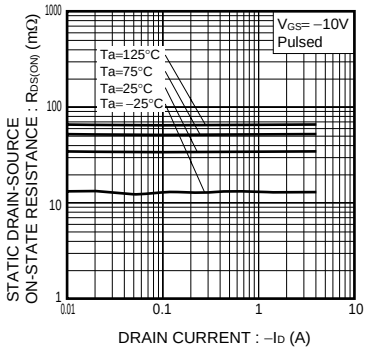


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (Ⅰ)

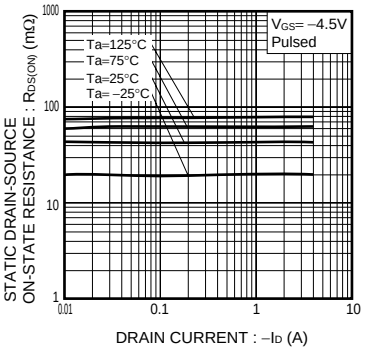


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (Ⅱ)

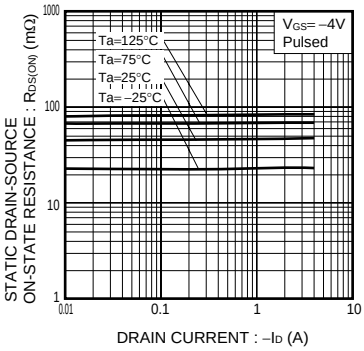


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (Ⅲ)

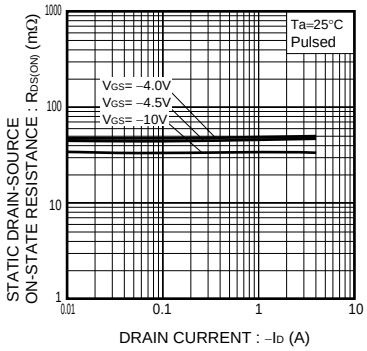


Fig.10 Static Drain-Source On-State Resistance vs. Drain Current (Ⅳ)

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