FAIRCHILD SEMICONDUCTOR®

RF1K49154

Data Sheet January 2002

2A, 60V, 0.130 Ohm, Dual N-Channel, LittleFET™ Power MOSFET

This Dual N-Channel power MOSFET is manufactured using the latest manufacturing process technology. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. These devices can be operated directly from integrated circuits.

Formerly developmental type TA49154.

Ordering Information

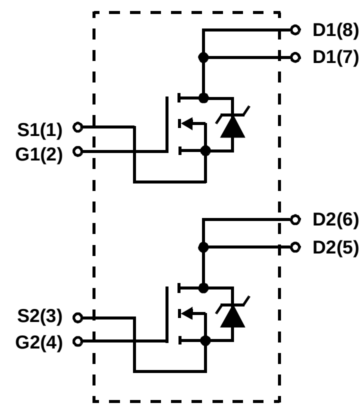
PART NUMBER	PACKAGE	BRAND
RF1K49154	MS-012AA	RF1K49154

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4915496.

Features

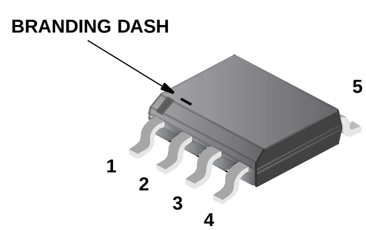
- 2A, 60V
- $r_{DS(ON)} = 0.130\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC MS-012AA



Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		RF1K49154	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ, Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (Pulse width = 5s)	I_D	2	A
Pulsed (Figure 5)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating (Figure 6)	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	2	W
Derate Above 25^oC		0.016	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V, (Figure 12)		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA, (Figure 11)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 55V, V_{GS} = 0V		-	-	1	µA
		V_{DS} = 50V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±10	µA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 2A, V_{GS} = 10V, (Figures 9, 10)		-	-	0.130	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D ≈ 2A, R_L = 15Ω, V_{GS} = 10V, R_{GS} = 25Ω (Figure 14)		-	-	50	ns
Turn-On Delay Time	$t_{d(ON)}$			-	10	-	ns
Rise Time	t_r			-	25	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	70	-	ns
Fall Time	t_f			-	35	-	ns
Turn-Off Time	t_{OFF}			-	-	155	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 2A, R_L = 24Ω (Figure 14)	-	26	32	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	14	17	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	0.8	1.0	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 13)		-	340	-	pF
Output Capacitance	C_{OSS}			-	140	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	40	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse Width = 1s Device Mounted on FR-4 Material		-	-	62.5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 2A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 100A/µs	-	-	62	ns

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

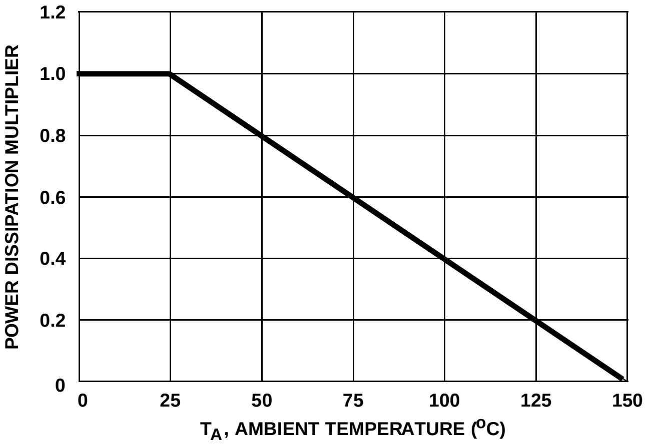


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

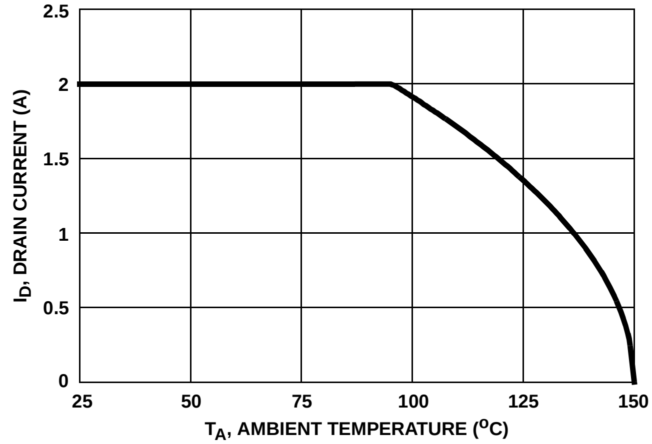


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

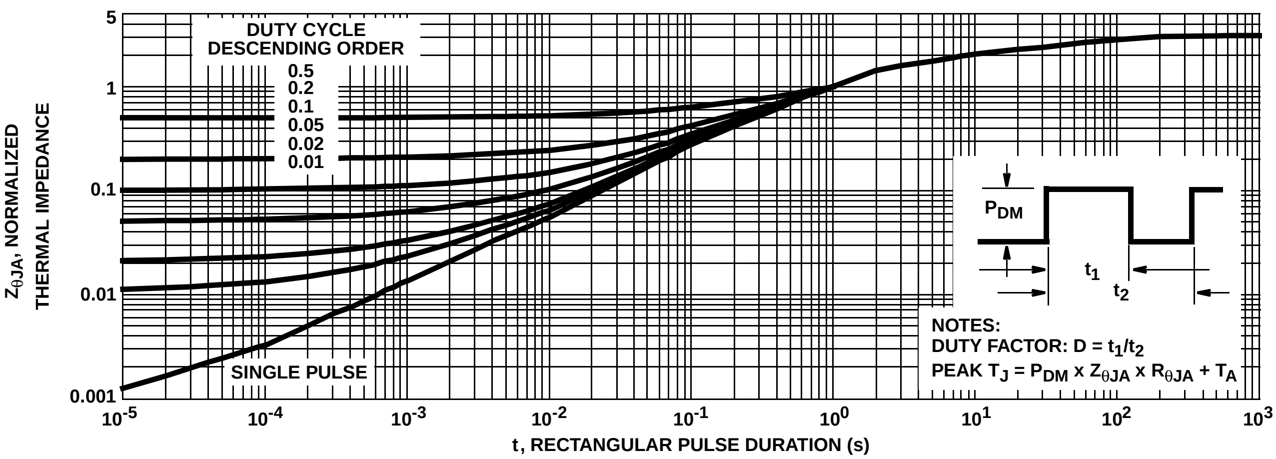


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

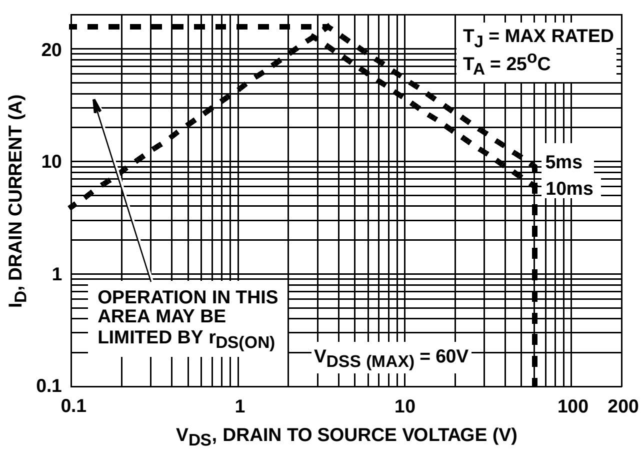


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

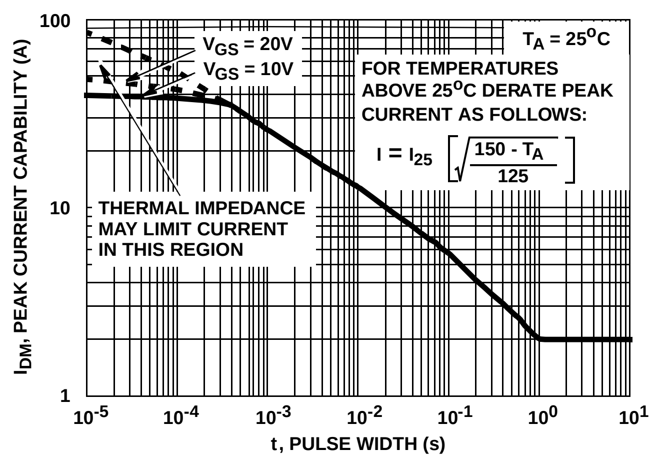
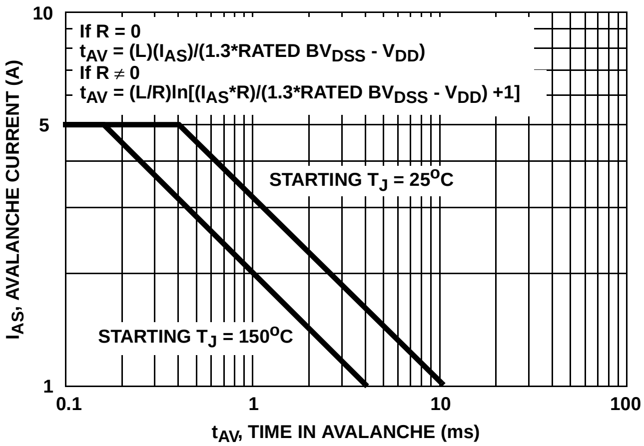


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

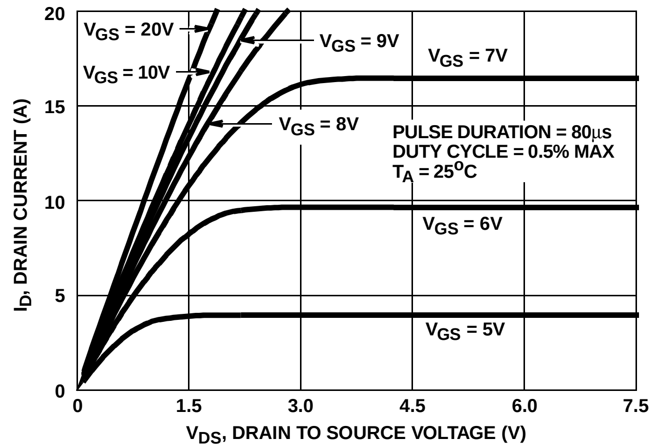


FIGURE 7. SATURATION CHARACTERISTICS

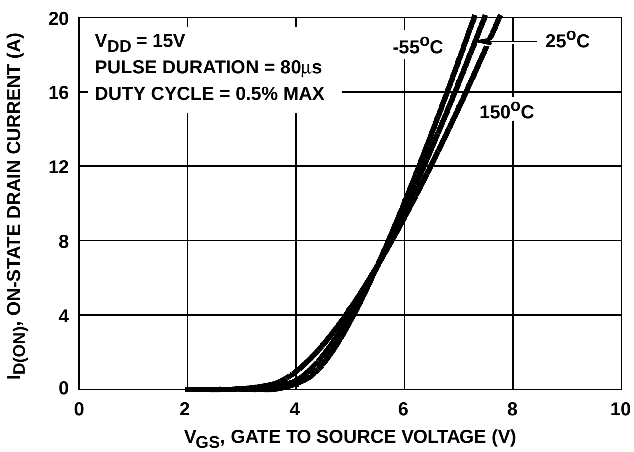


FIGURE 8. TRANSFER CHARACTERISTICS

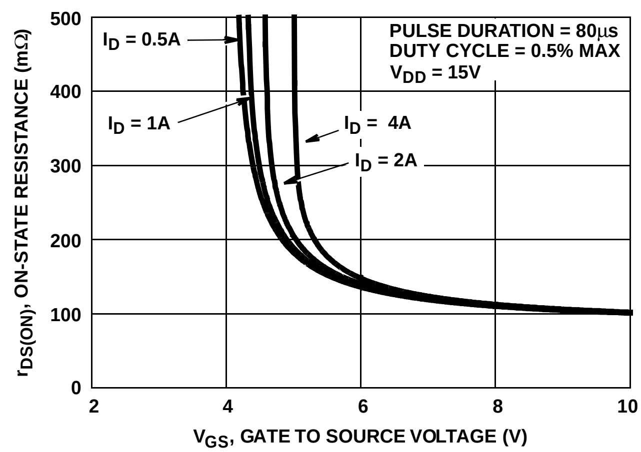


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

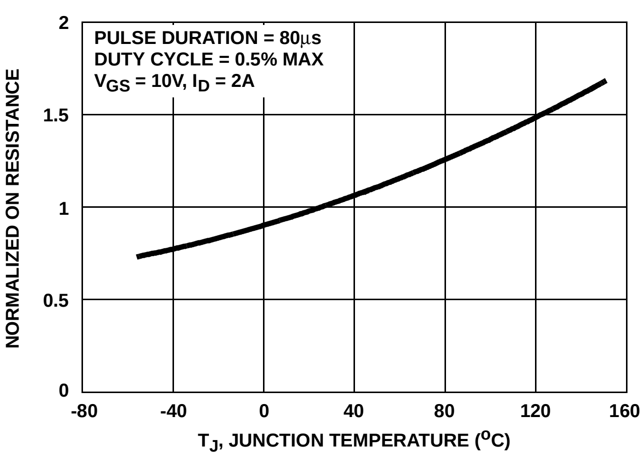


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

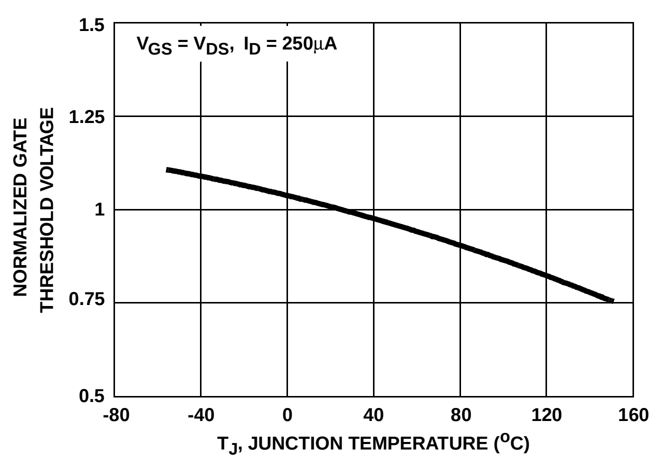


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

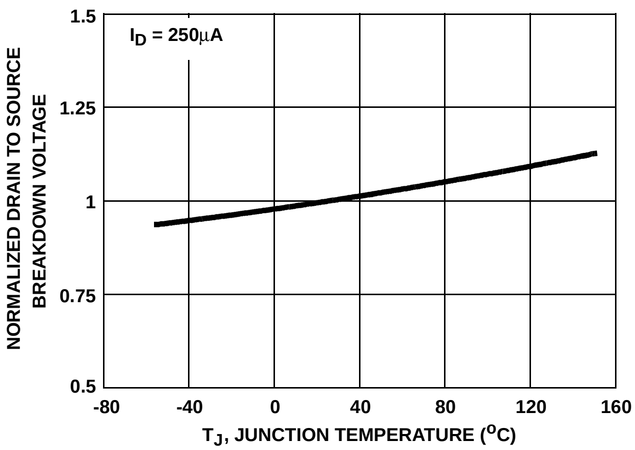


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

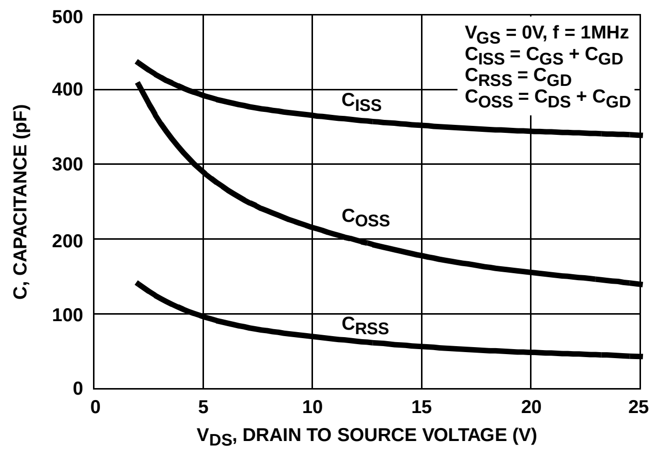
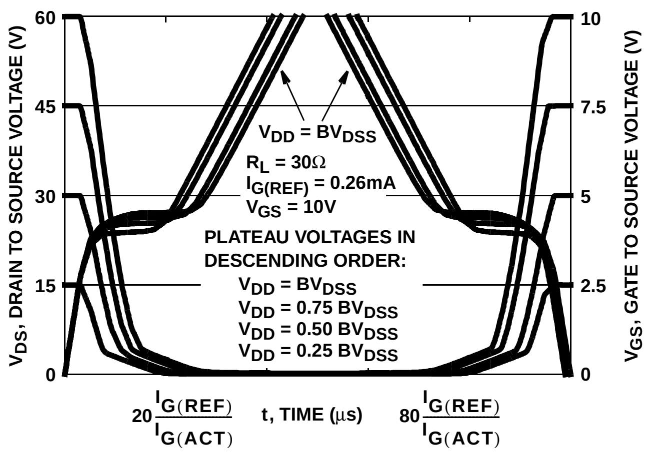


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

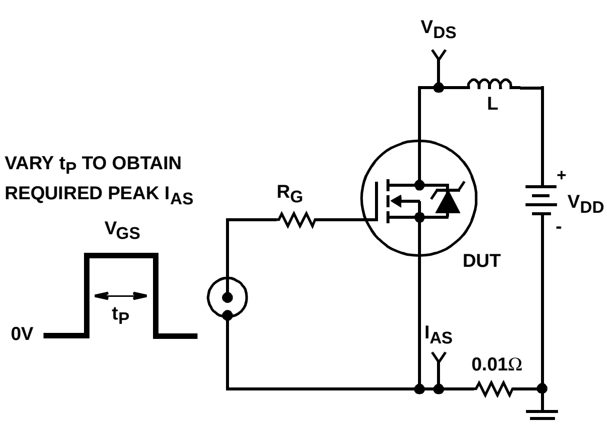


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

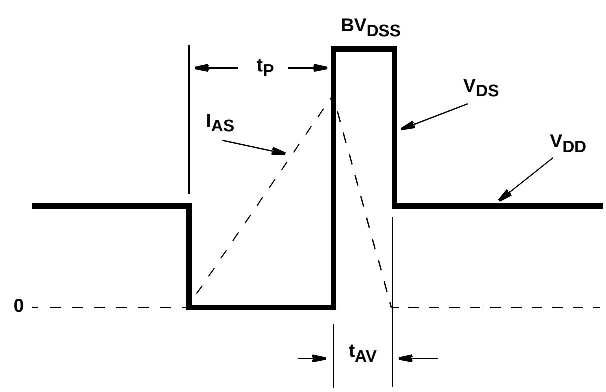


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

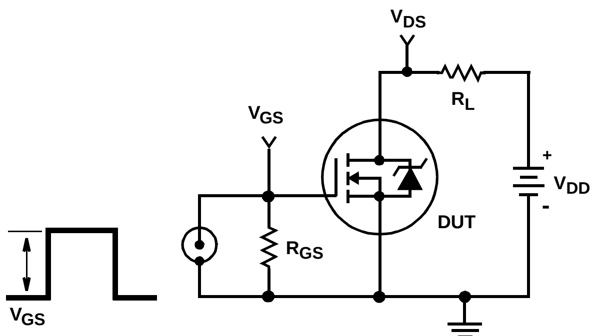


FIGURE 17. SWITCHING TIME TEST CIRCUIT

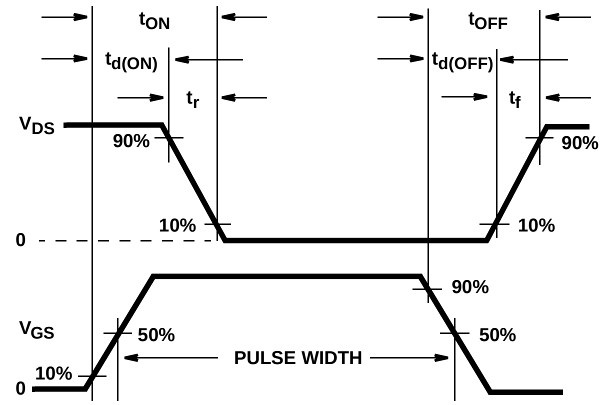


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

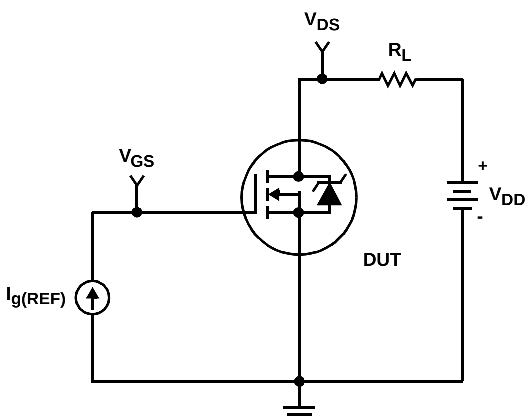


FIGURE 19. GATE CHARGE TEST CIRCUIT

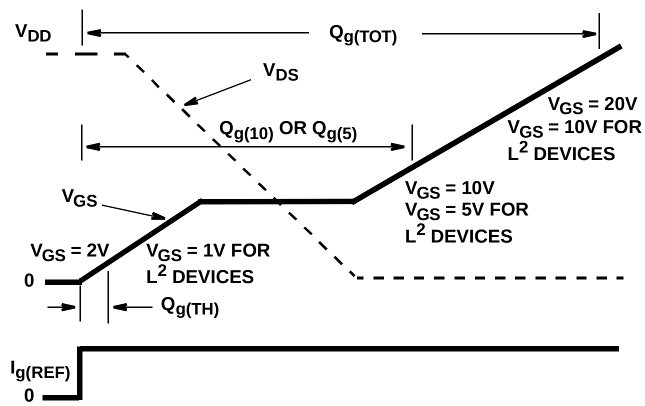
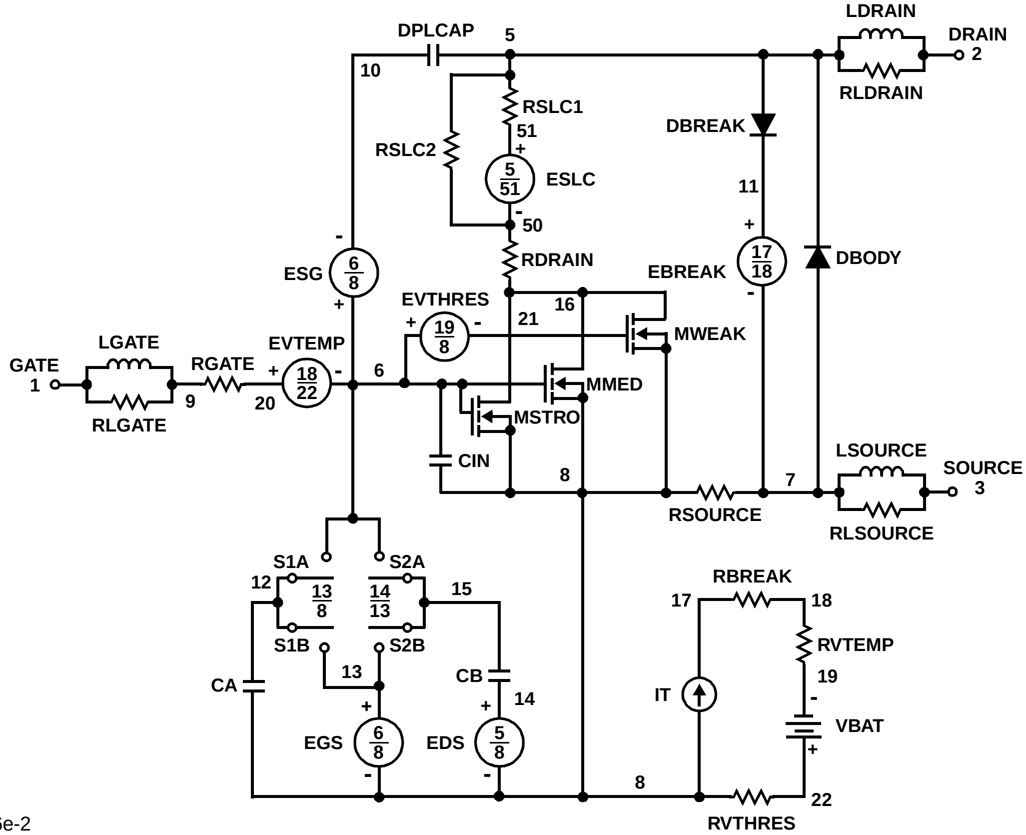


FIGURE 20. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

SUBCKT RF1K49154 2 1 3 ; rev 2/2/96

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CA 12 8 3.5e-10
CB 15 14 3.7e-10
CIN 6 8 2.26e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 63
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.4e-9
LSOURCE 3 7 3.1e-10
K1 LGATE LSOURCE 0.131

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 7.0e-3
RGATE 9 20 1.9
RLDRAIN 2 5 10
RLGATE 1 9 14
RLSOURCE 3 7 3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 5.6e-2
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*50),3))}

.MODEL DBODYMOD D (IS = 2.6e-13 RS = 2.34e-2 IKF = 5.5 N = 0.995 TRS1 = 2.8e-3 TRS2 = 1.1e-5 CJO = 3.7e-10 TT = 3.5e-8 M = 0.46
+ XTI = 5.5)
.MODEL DBREAKMOD D (RS = 0. 5IKF = 0.1 N = 1 TRS1 = 3e- 3TRS2 = -5e-5)
.MODEL DPLCAPMOD D (CJO = 5.6e-1 0IS = 1e-3 0N = 10 M = 0.92)
.MODEL MMEDMOD NMOS (VTO = 3.25 KP = 1.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.9)
.MODEL MSTROMOD NMOS (VTO = 3.68 KP = 13.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.83 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 19 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.08e- 3TC2 = 5e-7)
.MODEL RDRAINMOD RES (TC1 = 1.7e-2 TC2 = 1e-4)
.MODEL RSLCMOD RES (TC1 = 1e-9 TC2 = 1e-4)
.MODEL RSOURCEMOD RES (TC1 = 3.3e-3 TC2 = 1e-9)
.MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -4e-6)
.MODEL RVTEMPMOD RES (TC1 = -2.9e- 3TC2 = 2.2e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.1 VOFF= -4)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4 VOFF= -7.1)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.01 VOFF= 1.9)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.9 VOFF= 0.01)

.ENDS
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NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.