MX69F1602/1604C3T/B

16M-BIT [X16] FLASH AND 2M-BIT/4M-BIT [X16] SRAM MIXED MULTI CHIP PACKAGE MEMORY

FEATURES

- Supply voltage range: 2.7V to 3.6V
- Fast access time: Flash memory:70/90ns
  SRAM memory:70/85ns
- Operation temperature range: -40 ~ 85℃

FLASH

- Word mode only
- VCCf=VCCQ=2.7V~3.6V for read, erase and program operation
- VPP=12V for fast production programming
- Low power consumption
  - 9mA typical active read current, f=5MHz
  - 18mA typical program current (VPP=1.65~3.6V)
  - 21mA typical erase current (VPP=1.65~3.6V)
  - 7uA typical standby current under power saving mode
- Sector architecture
  - Sector structure : 4Kword x 2 (boot sectors), 4Kword x 6 (parameter sectors), 32Kword x 31 (main sectors)
  - Top/Bottom Boot
- Auto Erase and Auto Program
  - Automatically program and verify data at specified address
  - Auto sector erase at specified sector
- Automatic Suspend Enhance
  - Word write suspend to read
  - Sector erase suspend to word write
  - Sector erase suspend to read register report
- Automatic sector erase, word write and sector lock/unlock configuration
- 100,000 minimum erase/program cycles
- Boot Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Status Register feature for detection of program or erase cycle completion
- Data protection performance
  - Sectors to be locked/unlocked
- Common Flash Interface (CFI)
- 128-bit Protection Register
  - 64-bit Unique Device Identifier
  - 64-bit User-Programmable
- Latch-up protected to 100mA from -1V to VCC+1V

SRAM

- MX69F1602C3T/B: 128K wordx16 Bit
- MX69F1604C3T/B: 256K wordx16 Bit
- 70mA maximum active current
- 1uA typical standby current
- Data retention supply voltage: 2.0V~3.6V
- Byte data control : $\overline{LB}$s(Q0 to Q7) and $\overline{UB}$s(Q8 to Q15)

GENERAL DESCRIPTION

The MXIC's mixed multi chip memory combines Flash and SRAM into a single package. The mixed multi chip memory operates 2.7 to 3.6V power supply to allow for simple in-system operation.

The Flash memory of mixed multi chip memory manufactured with MXIC's advanced nonvolatile memory technology, the flash memory of mixed multi chip memory is designed to be re-programmed and erased in system or in standard EPROM programmers. The device offers access times of 70ns/90ns, and 7uA typical standby current.

Flash memories augment EPROM functionality with in-circuit electrical erasure and programming and use a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

Flash memory reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

The dedicated VPP pin gives complete data protection when VPP< VPPLK.

The Flash contains both a Command User Interface (CUI) and a Write State Machine (WSM). A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for erase, word write and sector lock/unlock configuration operations.

Flash erase automation allows sector erase operation to be executed using an industry-standard two-write command sequence to the CUI. A sector erase operation erases one of the device's 32K-word sectors typically within 1.0s, 4K-word sectors typically within 0.5s independent of other sectors. Each sector can be independently erased minimum 100,000 times. Sector erase suspend mode allows system software to suspend sector erase to read or write data from any other sector.

Flash program automation allows program operation to be executed using an industry-standard two-write command sequence to the CUI. Writing memory data is performed in word increments of the device's 32K-word sectors typically within 0.8s and 4K-word sectors typically within 0.1s. Word program suspend mode enables the system to read data or execute code from any other memory array location.

The Flash features with individual sectors locking by using a combination of thirty-nine sector lock-bits and $\overline{WP}$, to lock and unlock sectors.

The Flash status register indicates the status of the WSM when the sector erase, word program or lock configuration operation is done.

The Flash power saving mode feature substantially reduces active current when the device is in static mode (addresses not switching). In this mode, the typical ICCS current is 7uA (CMOS) at 3.0V VCC. As $\overline{CE}$f and $\overline{RESET}$ are at VCC, ICC CMOS standby mode is enabled. When $\overline{RESET}$ is at GND, the reset mode is enabled which minimize power consumption and provide data write protection.

The Flash require a reset time (tPHQV) from $\overline{RESET}$ switching high until outputs are valid. Similarly, the flash has a wake time (tPHEL) from $\overline{RESET}$-high until writes to the CUI are recognized. With $\overline{RESET}$ at GND, the WSM is reset and the status register is cleared.

The 2M-bit SRAM of MX69F1602C3T/B is organized as 128K-word by 16-bit. The 4M-bit SRAM of MX69F1604C3T/B is organized 256K-word by 16-bit. The advanced CMOS technology and circuit techniques provide both high speed and low power features of with a typical CMOS standby current of 1uA and maximum access time of 70ns/85ns in 3V operation.

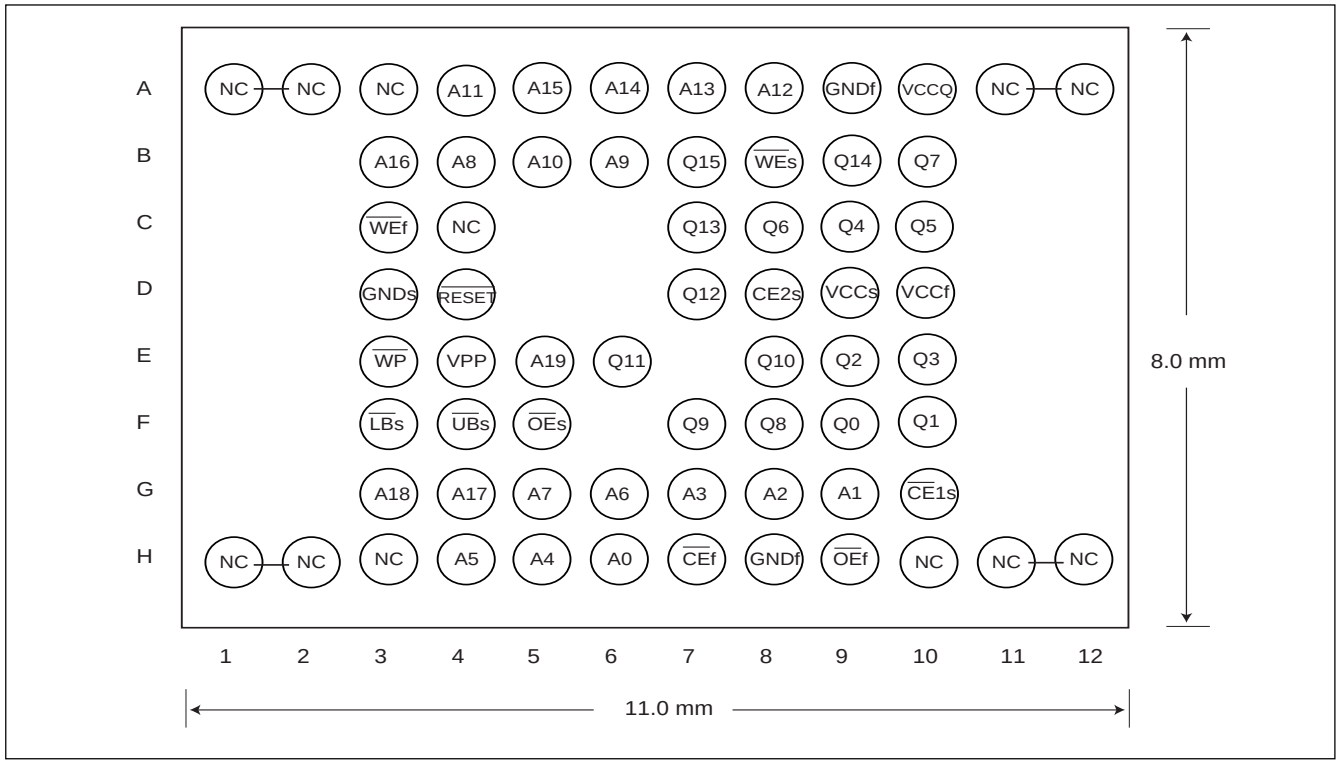
The mixed multi chip memory is available in 11mm x 8mm FBGA Package to suit a variety of design applications.

Feature Summary

Feature	MX69F1602/1604C3T/B	
Vcc Operating Voltage	2.7~3.6V	
Configuration	Flash	16M:1M Word x16bit
	SRAM	MX69F1602C3T/B:128K Word x16bit
		MX69F1604C3T/B:256K Word x16bit
Fast Access Time	- 70 :	Flash/70ns, SRAM/70ns
	- 90 :	Flash/90ns, SRAM/85ns
Block Architecture	Flash	2 x 4K Word Boot
		6 x 4K Word Parameter
		31 x 32K Word Main
Address Pin	Flash	A0~A19
	SRAM	MX69F1602C3T/B:A0~A16
		MX69F1604C3T/B:A0~A17
Manufacture Code	Flash	00C2H
Device ID Code	Flash	MX69F1602/1604C3T=88C2H
		MX69F1602/1604C3B=88C3H

PIN ASSIGNMENT

1.66-ball CSP for MX69F1602/1604C3T/B (Top View Balls Down, 11 x 8 x 1.4mm, Ball Pitch=0.8mm)



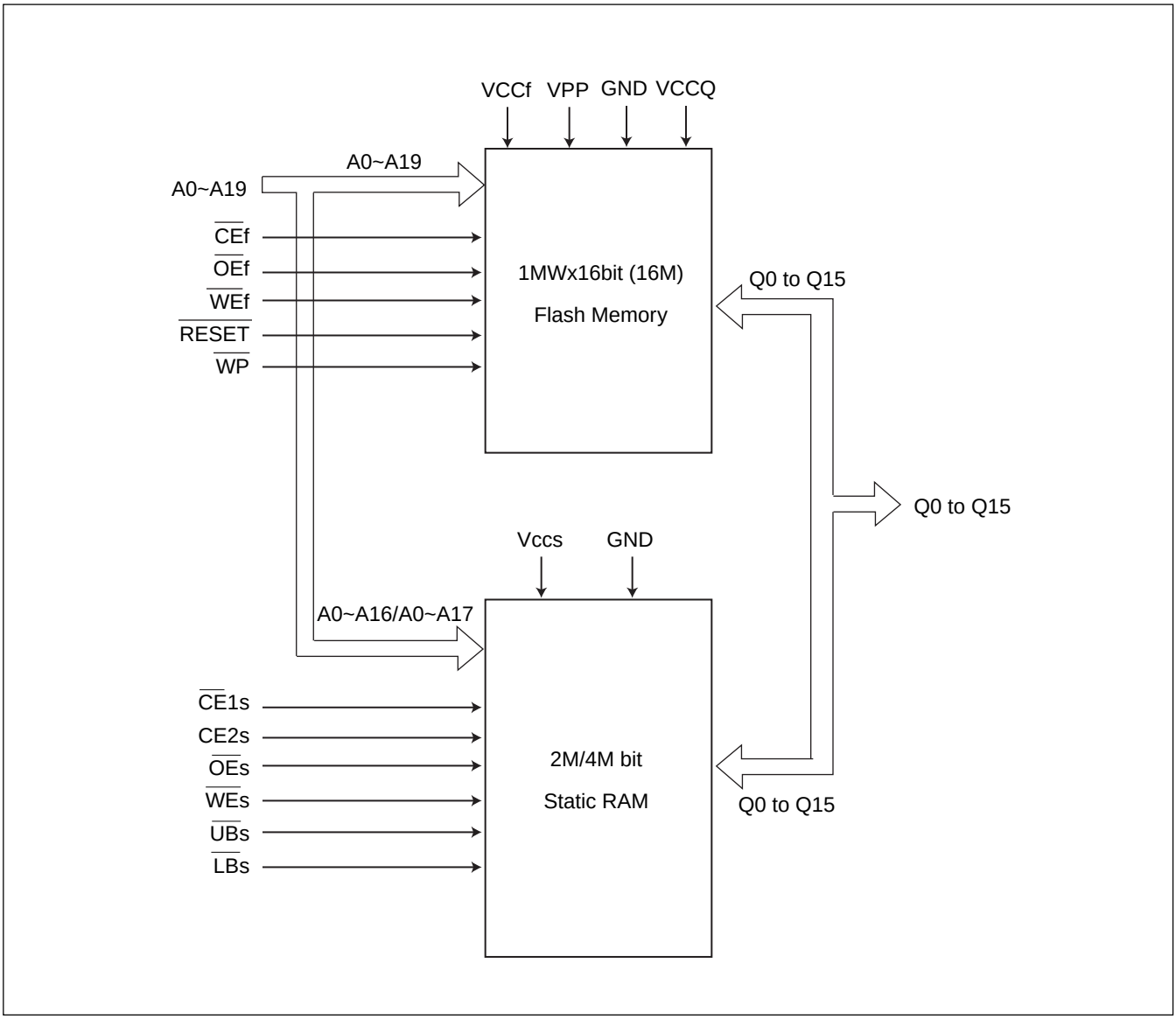
Notes:
1.To maintain compatibility with all JEDEC Variation B options for this ball location C6, this C6 land pad should be connected directly to the land pad for ball G4 (A17).

PIN DESCRIPTION

SYMBOL	PIN NAME
A0 to A16	Address Inputs (Common) for MX69F1602C3T/B
A0 to A17	Address Inputs (Common) for MX69F1604C3T/B
A17 to A19	Address Input (Flash) for MX69F1602C3T/B
A18 to A19	Address Input (Flash) for MX69F1604C3T/B
Q0 to Q15	Data Inputs/Outputs (Common)
$\overline{CE}$f	Chip Enable (Flash)
$\overline{CE}$1s	Chip Enable (SRAM)
CE2s	Chip Enable (SRAM)
$\overline{OE}$f	Output Enable (Flash)
$\overline{OE}$s	Output Enable (SRAM)

SYMBOL	PIN NAME
$\overline{WE}$f	Write Enable (Flash)
$\overline{WE}$s	Write Enable (SRAM)
$\overline{UB}$s	Upper Byte Control (SRAM)
$\overline{LB}$s	Lower Byte Control (SRAM)
$\overline{RESET}$	Hardware Reset Pin/Deep Power Down (Flash)
$\overline{WP}$	Write Protect
N.C.	No Connection
GND	Ground Pin (Common)
VCCf	Power Supply (Flash, 2.7V~3.6V)
VCCs	Power Supply (SRAM, 2.7V~3.6V)
VPP	Program/Erase Power Supply (1.65V~3.6V or 11.4V~12.6V)
VCCQ	I/O Power Supply (Flash) tied to VCCf

BLOCK DIAGRAM for MX69F1602/1604C3T/B



DEVICE BUS OPERATIONS for MX69F1602/1604C3T/B

		Notes	CEf (1)	$\overline{OEf}$	$\overline{WEf}$	$\overline{CE1s}$ (1)	CE2s (1)	$\overline{OEs}$	$\overline{WEs}$	$\overline{LBs}$	$\overline{UBs}$	Q0~ Q7	Q8~ Q15	$\overline{RESET}$
Full Standby		3,4	H	X	X	H	X	X	X	X	X	High Z	High Z	H
						X	L							
Flash Output Disable		3,4	L	H	H	H	X	X	X	X	X	High Z	High Z	H
						X	L							
Read from Flash	Array		L	L	H	H	X	X	X	X	X	Dout	Dout	H
						X	L							
	Query		L	L	H	H	X	X	X	X	X	Dout	Dout	H
						X	L							
	Configuration		L	L	H	H	X	X	X	X	X	ID(2)	ID(2)	H
						X	L							
	Status Register		L	L	H	H	X	X	X	X	X	Dout	Dout	H
						X	L							
Write to Flash		5,7	L	H	L	H	X	X	X	X	X	Din	Din	H
						X	L							
Reset		3,4,6	X	X	X	H	X	X	X	X	X	High Z	High Z	L
						X	L							

SRAM Output Disable	3,4	H	X	X	L	H	H	H	X	X	High Z	High Z	H
							X	X	H	H			
Read from SRAM		H	X	X	L	H	L	H	L	L	Dout	Dout	H
									H	L	High Z	Dout	H
									L	H	Dout	High Z	H
Write to SRAM		H	X	X	L	H	H	L	L	L	Din	Din	H
									H	L	X	Din	H
									L	H	Din	X	H

Legend:
L=VIL, H=VIH, X at control pins=VIL or VIH. See "ELECTRIAL CHARACTERISTICS 1.DC Characteristics" for voltage levels.

Notes:
1. Do not apply $\overline{CEf}$=VIL, $\overline{CE1s}$=VIL and CE2s=VIH at a time.
2. ID=Device Identifier Code. See "Table 3. Configuration Code"
3. Outputs are dependent on a seperate device controlling bus output.
4. Modes of the flash and SRAM can be interleaved so that while one is disabled the other controls outputs.
5. To program or erase the lockable sectors hold $\overline{WP}$ at VIH.
6. $\overline{RESET}$ at GND ± 0.2V to ensure the lowest power consumption.
7. Refer to Table 2 for valid Din during a write operation.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
During Read, Sector Erase, Word Write . . . . . -40°C to +85°C
Storage Temperature . . . . . .-65°C to +125°C
Voltage on Any Ball (except VCCf, VCCs, VCCQ and VPP) with respect to GND . . . . . .-0.5 V to VCC+0.5(1)
VPP Supply Voltage (for Sector Erase and Word Write) with respect to GND . . . . . .-0.5V to +13.5V(1,2,4)
VCCf, VCCs and VCCQ Supply Voltage with respect to GND. . . . . .-0.2V to +4.0V(1)
Output Short Circuit Voltage . . . . . .100mA(3)

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output balls to VCCf/VCCs/VCCQ+0.5V which during transition; may overshoot to VCCf/VCCs/VCCQ+2.0V for periods <20ns.
2. Maximum DC voltage on VPP may overshoot to +14.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. VPP voltage is normally 1.65V~3.6V. Connection to supply of 11.4V~12.6V can only be done for 1000 cycles on the main sectors and 2500 cycles on the parameter sectors during program/erase. VPP may be connected to 12V for a total of 80 hours maximum.

Operating Conditions (Temperature and VCC Operating Conditions)

Symbol	Parameter	Min.	Max.	Unit	Notes
TA	Operating Temperature	-40	+85	°C	
VCCf	Flash VCC Supply Voltage	2.7	3.6	V	1
VCCs	SRAM VCC Supply Voltage	2.7	3.6	V	
VCCQ	Flash I/O Supply Voltage	2.7	3.6	V	1
VPP1	Supply Voltage	1.65	3.6	V	1
VPP2	Supply Voltage	11.4	12.6	V	1,2
Cycling	Sector Erase Cycling	100,000			2

NOTE:
1.VCCf and VCCQ must share the same supply.
2.Applying VPP=11.4~12.6V during a program/erase can only be done for a maximum of 1000 cycles on the main sectors and 2500 cycles on the parameter sectors. VPP may be connected to 12V for a total of 80 hours maximum.

Capacitance (1) (TA=+25°C, f=1MHz)

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
CIN	Input Capacitance	16	18	pF	VIN=0.0V
COUT	Output Capacitance	20	22	pF	VOUT=0.0V

NOTE:
1.Sampled, not 100% tested.

FLASH SECTOR STRUCTURE (MX69F1602/1604C3T)

Sector	Sector Size	Address Range (h)
Boot Sector 0	4K Word	FF000 ~ FFFFF
Boot Sector 1	4K Word	FE000 ~ FEFFF
Parameter Sector 0	4K Word	FD000 ~ FDFFF
Parameter Sector 1	4K Word	FC000 ~ FCFFF
Parameter Sector 2	4K Word	FB000 ~ FBFFF
Parameter Sector 3	4K Word	FA000 ~ FAFFF
Parameter Sector 4	4K Word	F9000 ~ F9FFF
Parameter Sector 5	4K Word	F8000 ~ F8FFF
Main Sector 0	32K Word	F0000 ~ F7FFF
Main Sector 1	32K Word	E8000 ~ EFFFF
Main Sector 2	32K Word	E0000 ~ E7FFF
Main Sector 3	32K Word	D8000 ~ DFFFF
Main Sector 4	32K Word	D0000 ~ D7FFF
Main Sector 5	32K Word	C8000 ~ CFFFF
Main Sector 6	32K Word	C0000 ~ C7FFF
Main Sector 7	32K Word	B8000 ~ BFFFF
Main Sector 8	32K Word	B0000 ~ B7FFF
Main Sector 9	32K Word	A8000 ~ AFFFF
Main Sector 10	32K Word	A0000 ~ A7FFF
Main Sector 11	32K Word	98000 ~ 9FFFF
Main Sector 12	32K Word	90000 ~ 97FFF
Main Sector 13	32K Word	88000 ~ 8FFFF
Main Sector 14	32K Word	80000 ~ 87FFF
Main Sector 15	32K Word	78000 ~ 7FFFF
Main Sector 16	32K Word	70000 ~ 77FFF
Main Sector 17	32K Word	68000 ~ 6FFFF
Main Sector 18	32K Word	60000 ~ 67FFF
Main Sector 19	32K Word	58000 ~ 5FFFF
Main Sector 20	32K Word	50000 ~ 57FFF
Main Sector 21	32K Word	48000 ~ 4FFFF
Main Sector 22	32K Word	40000 ~ 47FFF
Main Sector 23	32K Word	38000 ~ 3FFFF
Main Sector 24	32K Word	30000 ~ 37FFF
Main Sector 25	32K Word	28000 ~ 2FFFF
Main Sector 26	32K Word	20000 ~ 27FFF
Main Sector 27	32K Word	18000 ~ 1FFFF
Main Sector 28	32K Word	10000 ~ 17FFF
Main Sector 29	32K Word	08000 ~ 0FFFF
Main Sector 30	32K Word	00000 ~ 07FFF

FLASH SECTOR STRUCTURE (MX69F1602/1604C3B)

Sector	Sector Size	Address Range (h)
Boot Sector 0	4K Word	00000 ~ 00FFF
Boot Sector 1	4K Word	01000 ~ 01FFF
Parameter Sector 0	4K Word	02000 ~ 02FFF
Parameter Sector 1	4K Word	03000 ~ 03FFF
Parameter Sector 2	4K Word	04000 ~ 04FFF
Parameter Sector 3	4K Word	05000 ~ 05FFF
Parameter Sector 4	4K Word	06000 ~ 06FFF
Parameter Sector 5	4K Word	07000 ~ 07FFF
Main Sector 0	32K Word	08000 ~ 0FFFF
Main Sector 1	32K Word	10000 ~ 17FFF
Main Sector 2	32K Word	18000 ~ 1FFFF
Main Sector 3	32K Word	20000 ~ 27FFF
Main Sector 4	32K Word	28000 ~ 2FFFF
Main Sector 5	32K Word	30000 ~ 37FFF
Main Sector 6	32K Word	38000 ~ 3FFFF
Main Sector 7	32K Word	40000 ~ 47FFF
Main Sector 8	32K Word	48000 ~ 4FFFF
Main Sector 9	32K Word	50000 ~ 57FFF
Main Sector 10	32K Word	58000 ~ 5FFFF
Main Sector 11	32K Word	60000 ~ 67FFF
Main Sector 12	32K Word	68000 ~ 6FFFF
Main Sector 13	32K Word	70000 ~ 77FFF
Main Sector 14	32K Word	78000 ~ 7FFFF
Main Sector 15	32K Word	80000 ~ 87FFF
Main Sector 16	32K Word	88000 ~ 8FFFF
Main Sector 17	32K Word	90000 ~ 97FFF
Main Sector 18	32K Word	98000 ~ 9FFFF
Main Sector 19	32K Word	A0000 ~ A7FFF
Main Sector 20	32K Word	A8000 ~ AFFFF
Main Sector 21	32K Word	B0000 ~ B7FFF
Main Sector 22	32K Word	B8000 ~ BFFFF
Main Sector 23	32K Word	C0000 ~ C7FFF
Main Sector 24	32K Word	C8000 ~ CFFFF
Main Sector 25	32K Word	D0000 ~ D7FFF
Main Sector 26	32K Word	D8000 ~ DFFFF
Main Sector 27	32K Word	E0000 ~ E7FFF
Main Sector 28	32K Word	E8000 ~ EFFFF
Main Sector 29	32K Word	F0000 ~ F7FFF
Main Sector 30	32K Word	F8000 ~ FFFFF

FLASH

1.0 PRINCIPLES OF OPERATION

The product includes an on-chip WSM to manage sector erase, word write and lock-bit configuration functions.

After initial device power-up or return from reset mode (see section on Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the VPP voltage. All functions associated with altering memory contents - sector erase, word write, sector lock/unlock, status and identifier codes - are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the sector erase, word write and sector lock/unlock. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Address is latched at falling edge of $\overline{CE}$f and data latched at rising edge of $\overline{WE}$f. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of sector erase, word write and sector lock/unlock can be stored in any sector. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Sector erase suspend allows system software to suspend a sector erase to read/write data from/to sectors other than that which is suspend. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

With the mechanism of sector lock, memory contents cannot be altered due to noise or unwanted operation. When $\overline{RESET}$=VIH and VCCf<VLKO (lockout voltage), any data write alteration can be failure. During read operation, if write VPP voltage is below VPPLK, then hardware level data protection is achieved. With CUI's two-step command sequence sector erase, word write or sector lock/unlock, software level data protection is achieved also.

2.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

2.1 Read

Information can be read from any sector, configuration codes or status register independent of the VPP voltage. $\overline{RESET}$ can be at VIH.

The first task is to write the appropriate read mode command (Read Array, Read Configuration, Read Query or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset, the device automatically resets to read array mode. In order to read data, control pins set for $\overline{CE}$f, $\overline{OE}$f, $\overline{WE}$f, $\overline{RESET}$ and $\overline{WP}$ must be driven to active. $\overline{CE}$f and $\overline{OE}$f must be active to obtain data at the outputs. $\overline{CE}$f is the device selection control. $\overline{OE}$f is the data output (Q0-Q15) control and active drives the selected memory data onto the I/O bus, $\overline{WE}$f must be VIH, $\overline{RESET}$ must be VIH, $\overline{WP}$ must be at VIL or VIH.

2.2 Output Disable

With $\overline{OE}$f at a logic-high level (VIH), the device outputs are disabled. Output pins (Q0-Q15) are placed in a high-impedance state.

2.3 Standby

$\overline{CE}$f at a logic-high level (VIH) places the device in standby mode which substantially reduces device power consumption. Q0~Q15 outputs are placed in a high-impedance state independent of $\overline{OE}$f. If deselected during sector erase, word write or sector lock/unlock, the device continues functioning, and consuming active power until the operation completes.

2.4 Reset

As $\overline{RESET}$=VIL, it initiates the reset mode. The device enters reset/deep power down mode. However, the data stored in the memory has to be sustained at least 100ns in the read mode before the device becomes deselected

and output high impedance state.

In read modes, RESET-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RESET must be held low for a minimum of 100ns. Time tPHQV is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval tPHEL or tPHWL, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H. Sector lock bit is set at lock status.

During sector erase, word write or sector lock/unlock modes, RESET-low will abort the operation. Memory contents being altered are no longer valid; the data may be partially erased or written.

In addition, CUI will go into either array read mode or erase/write interrupted mode. When power is up and the device reset subsequently, it is necessary to read status register in order to assure the status of the device. Recognizing status register (SR.7~0) will assure if the device goes back to normal reset and enters array read mode.

2.5 Read Configuration Codes

The read configuration codes operation outputs the manufacturer code, device code, sector lock configuration codes, and the protection register. Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The sector lock codes identify locked and unlocked sectors.

2.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When VCCf=2.7V-3.6V and VPP within VPP1 or VPP2 range, the CUI additionally controls sector erase, word write and sector lock/unlock.

The Sector Erase command requires appropriate command data and an address within the sector to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word Write command requires the command and address of the location to be written. Set Sector lock/unlock commands require the command and address within the device or sector within the device (Sector Lock) to be locked. The Clear Sector Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WEf and CEf are active (whichever goes high first). The address and data needed to execute a command are latched on the rising edge of WEf or CEf. Standard microprocessor write timings are used.

3.0 COMMAND DEFINITIONS

The flash memory has four read modes: read array, read configuration, read status, read query, and two write modes: program, erase. These read modes are accessible independent of the VPP voltage. But write modes are disable during VPP<VPPLK. Placing VPP on VPP1/2 enables successful sector erase, word write and sector lock/unlock.

Device operations are selected by writing specific commands into the CUI. Table 2 defines these commands.

Table 2. Command Definition (1)

Command	Bus Cycles Required	Notes	First Bus Cycle			Second Bus Cycle		
			Operation (1)	Address (2)	Data (3)	Operation (1)	Address (2)	Data (3)
Read Array	1		Write	X	FFH			
Read Configuration	≥ 2	2,4	Write	X	90H	Read	IA	ID
Read Query	2	2,7	Write	X	98H	Read	QA	QD
Read Status Register	2	3	Write	X	70H	Read	X	SRD
Clear Status Register	1	3	Write	X	50H			
Sector Erase/Confirm	2		Write	X	20H	Write	SA	D0H
Word Write	2	2,5	Write	X	40H/10H	Write	WA	WD
Program/Erase Suspend	1		Write	X	B0H			
Program/Erase Resume	1		Write	X	D0H			
Sector Lock	2		Write	X	60H	Write	SA	01H
Sector Unlock	2	6	Write	X	60H	Write	SA	D0H
Lock-Down Sector	2		Write	X	60H	Write	SA	2FH
Protection Program	2		Write	X	C0H	Write	PA	PD
Lock Protection Register	2		Write	X	C0H	Write	PA	FFFD

Notes:
1. Bus operation are defined at page 6 and referred to AC Timing Waveform.
2. X=Any address within device.
   IA=ID-Code Address (refer to Table 3).
   ID=Data read from identifier code.
   SA=Sector Address within the sector being erased.
   WA=Address of memory location to be written.
   WD=Data to be written at location WA.
   PA=Program Address, PD=Program Data
   QA=Query Address, QD=Query Data.
3. Data is latched from the rising edge of $\overline{WE}$f or $\overline{CE}$f (whichever goes high first)
   SRD=Data read from status register, see Table 5 for description of the status register bits.
4. Following the Read Configuration codes command, read operation access manufacturer, device codes, sector lock/unlock codes, see chapter 4.2.
5. Either 40H or 10H command is recognized by the WSM as word write setup.
6. The sector unlock operation simultaneously clear all sector lock.
7. Read Query Command is read for CFI query information.

3.1 Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a sector erase, word write or sector lock configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via a Sector Erase Suspend or Word Write Suspend command. If RESET=VIL device is in read Read Array command mode, this read operation no longer requires VPP. The Read Array command functions independently of the VPP voltage and RESET can be VIH.

3.2 Read Configuration Codes Command

The configuration code operation is initiated by writing the Read Configuration Codes command (90H). To return to read array mode, write the Read Array Command (FFH). Following the command write, read cycles from addresses shown in Table 3 retrieve the manufacturer, device, sector lock configuration codes and the protection register(see Table 3 for configuration code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Configuration Codes command functions independently of the VPP voltage and RESET can be VIH. Following the Read Configuration Codes command, the information is shown:

Table 3. Configuration Code

Code	Address (A19-A0)	Data (Q15-Q0)
Manufacturer Code	00000H	00C2H
Device Code(Top/Bottom)	00001H	88C2/88C3H
Sector Lock Configuration	XX002H	LocK
- Sector is unlocked		Q0=0
- Sector is locked		Q0=1
- Sector is locked-down		Q1=1
Protection Register Lock	80	PR-LK
Protection Register	81-88	PR

3.3 Read Status Register Command

CUI writes read status command (70H). The status register may be read to determine when a sector erase, word write or lock-bit configuration is complete and whether the operation completed successfully. (refer to table 5) It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of CEf or OEf, whichever occurs last. CEf or OEf must toggle to VIH before further reads to update the status register latch. The Read Status Register command functions independently of the VPP voltage. RESET can be VIH.

3.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command (50H). These bits indicate various failure conditions (see Table 5). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple sectors or writing several words in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written on CUI. It functions independently of the applied VPP Voltage. RESET can be VIH. This command is not functional during sector erase or word write suspend modes.

3.5 Sector Erase Command

Erase is executed one sector at a time and initiated by a two-cycle command. A sector erase setup is first written (20H), followed by a sector erase confirm (D0H). This command sequence requires appropriate sequencing and an address within the sector to be erased. Sector preconditioning, erase, and verify are handled internally by the WSM. After the two-cycle sector erase sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect sector erase completion by analyzing the output data of the status register bit SR.7.

When the sector erase is complete, status register bit SR.5 should be checked. If a sector erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that sector contents are not accidentally erased. An invalid sector Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable sector erasure can only occur when 2.7V~3.6V and VPP=VPP1/2. In the absence of this high voltage, sector contents are protected against erasure. If sector erase is attempted while VPP≤VPPLK SR.3 and SR.5 will be set to "1". To successfully erase the boot sector, the corresponding sector lock-bit must be clear first. In parameter and sectors case, it must be cleared the corresponding sector lock-bit. If sector erase is attempted when the excepting above sector being locked conditions, SR.1 and SR.5 will be set to "1". Sector erase is not functional.

3.6 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data. The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect the completion of the word write event by analyzing the status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when VCCf=2.7V~3.6V and VPP=VPP1/2. If VPP is not within acceptable limits, the WSM doesn't execut the program command. If word write is attempted while VPP≤VPPLK, status register bits SR.3 and SR.4 will be set to "1". Successful word write requires for boot sector that WP is VIH the corresponding sector lock-bit be cleared. In parameter and main sectors case, it must be cleared the corresponding sector lock-bit. If word write is attempted when the excepting above sector being clocked conditions, SR.1 and SR.4 will be set to "1". Word write is not functional.

3.7 Sector Erase Suspend Command

The Sector Erase Suspend command (50H) allows sector-erase interruption to read or word write data in another sector of memory. Once the sector erase process starts, writing the Sector Erase Suspend command requests that the WSM suspend the sector erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Sector Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the sector erase operation has been suspended (both will be set to "1"). Specification tWHRH2/tEHRH2 defines the sector erase suspend latency.

When Sector Erase Suspend command is written to the CUI, if sector erase was finished, the device would be placed read array mode. Therefore, after Sector Erase Suspend command is written to the CUI, Read Status Register command (70H) has to be written to CUI, then status register bit SR.6 should be checked if/when the device is in suspend mode.

At this point, a Read Array command can be written to read data from sectors other than that which is suspended. A Word Write commands sequence can also be issued during erase suspend to program data in other sectors. Using the Word Write Suspend command (see Section 4.9), a word write operation can also be suspended. During a word write operation with sector erase suspended, status register bit SR.7 will return to "0".

However, SR.6 will remain "1" to indicate sector erase suspend status.

The only other valid commands while sector erase is suspended are Read Status Register, Read Configuration, Read Query, Program Setup, Program Resume, Sector Lock, Sector Unlock, Sector Lock-Down and sector erase Resume. After a Sector Erase Resume command is written to the flash memory, the WSM will continue the sector erase process. Status register bits SR.6 and SR.7 will automatically be cleared. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 9). VPP must remain at VPP1/2 while sector erase is suspended. RESET must also remain at VIH (the same RESET level used for sector erase). Sector cannot resume until word write operations initiated during sector erase suspend has completed.

If the time between writing the Sector Erase Resume command and writing the Sector Erase Suspend command is shorter than 15ms and both commands are written repeatedly, a longer time is required than standard sector erase until the completion of the operation.

3.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the Word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). Specification tWHRH1/tEHRH1 defines the word write suspend latency.

When Word Write Suspend command write to the CUI, if word write was finished, the device places read array mode. Therefore, after Word Write Suspend command write to the CUI, Read Status Register command (70H) has to be written to CUI, then status register bit SR.2 should be checked for if/when the device is in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register Read Configuration, Read Query and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the Word write process. Status register bits SR.2 and SR.7 will automatically be cleared. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 7). VPP must remain at VPP1/2 while in word write suspend mode. RESET must also remain at VIH (the same RESET level used for word write).

If the time between writing the Word Write Resume command and writing the Word Write Suspend command is short and both commands are written repeatedly, a longer time is required than standard word write until the completion of the operation.

3.9 Sector Lock/Unlock /Lockdown Command

3.9.1 Sector Locked State

The default status of all sectors upon power-up or reset is locked. Any attempt on program or erase operations will result in an error on bit SR.1 of a locked sector. The status of a locked sector can be changed to unlocked or lock-down using software commands. An unlocked sector can be locked by writing the sector lock command sequence, 60H followed by 01H.

3.9.2 Sector Unlocked State

An unlocked sector can be programmed or erased. All unlocked sector return to the locked state when the device is either reset or powered down. The status of an unlocked sector can be changed to locked or locked-down using software commands. A locked sector can be unlocked by writing unlock command sequence, 60H followed by D0H.

3.9.3 Sector Locked-Down State

Sectors which are locked-down are protected from program and erase operation; however, the protection status of these sectors cannot be changed using software commands alone. Any sector locked or unlocked can be locked-down by writing the lock-down command sequence, 60H followed by 2FH. When the device is reset or powered down, the locked-down sectors will revert to the locked state.

The status of $\overline{WP}$ will determine the function of sector lock-down and is summarized is followed:

$\overline{WP}$	Sector Lock-down Description
$\overline{WP}$=0	- sectors are protected from program, erase, and lock status changes
$\overline{WP}$=1	- the sector lock-down function is disabled - an individual lock-down sector can be unlocked and relocked via software command. Once $\overline{WP}$ goes low, sectors that previously locked-down returns to lock-down state regardless of any changes when $\overline{WP}$ was high.

In addition, sector lock-down is cleared only when the device is reset or powered down.

3.9.4 Read Sector Lock Status

The lock status of every sector can be read through Read Configuration mode. To enter this mode, first command write 90H to the device. The subsequent reads at sector address +00002 will output the lock status of this sector. The lock status can be read from the lowest two output pins Q0 and Q1. Q0 indicates the sector lock/unlock status and set by the lock command and cleared by the unlock command. When entering lock-down, the lock status is automatically set. Q1 indicates lock-down status and is set by the lock-down command. It cannot be further cleared by software, only by device reset or power-down.

Sector Lock Configuration Table

Lock Status	Data
Sector is unlocked	Q0=0
Sector is locked	Q0=1
Sector is locked-down	Q1=1

3.9.5 Sector Locking while Erase Suspend

The sector lock status can be performed during an erase suspend by using standard locking command sequences to unlock, lock, or lock-down a sector.

In order to change sector locking during an erase operation, the write erase suspend command (B0H) is placed first; then check the status register until it is shown that the actual erase operation has been suspended. Subsequent writing the desired lock command sequence to a sector and the lock status will be changed. When completing any desired lock, read or program operation, resume the erase operation with the Erase Resume Command (D0H).

If a sector is locked or locked-down during the same sector is being placed in erase suspend, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

Locking operation cannot be performed during a program suspend.

3.9.6 Status Register Error Checking

The operation of locking system for this device can be used the term "state (X,Y,Z)" to specify locking status, where X=value of $\overline{WP}$, Y=bit Q1 of the sector lock status register, and Z=bit Q0 of the sector lock status register. Q0 indicates if a sector is locked (1) or unlocked (0). Q1 indicates if a sector has been locked-down(1) or not (0).

Table 4. Sector Locking State Transitions

Current State (X, Y, Z)=				Erase/Prog. Operation if	Lock Command Input Result (Next State) (X, Y, Z)=		
$\overline{WP}$	Q1	Q0	Name	Enable ?	Lock	Unlock	Lock-Down
0	0	0	Unlocked	Yes	(001)	Unchanged	(011)
0	0	1	Locked (default)	No	Unchanged	(000)	(011)
0	1	1	Locked-Down	No	Unchanged	Unchanged	Unchanged
1	0	0	Unlocked	Yes	(101)	Unchanged	(111)
1	0	1	Locked	No	Unchanged	(100)	(111)
1	1	0	Lock-Down Disabled	Yes	(111)	Unchanged	(111)
1	1	1	Lock-Down Disabled	No	Unchanged	(110)	Unchanged

Note:
At power-up or device reset, all sectors default to locked state (001) (if $\overline{WP}$=0).
Holding $\overline{WP}$=0 is the recommended default.

Table 5. Status Register Definition

WSMS	SESS	ES	PS	VPPS	PSS	SLS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

NOTES:
Check WSM bit first to determine word program or sector Erase completion, before checking Program or Erase Status bits.

SR.6 = SECTOR ERASE SUSPEND STATUS (SESS)
1 = Sector ERASE Suspended
0 = Sector Erase in Progress/Completed

When Sector Erase Suspend is issued, WSM halts execution and sets both WSMS and SESS bits to "1". SESS bit remains set to "1" until an Sector Erase Resume command is issued.

SR.5 = ERASE STATUS (ES)
1 = Error in Programming
0 = Successful Sector Erase or Clear Sector Lock-Bits

When this bit (SR.5) is set to "1", it means WSM is unable to verify successful sector erasure.

SR.4 = PROGRAM STATUS (PS)
1 = Error in Programming
0 = Successful Programming

When this bit is set to "1", WSM has attempted but failed to program a word.

SR.3 = VPP STATUS (VPPS)
1 = VPP Low Detect, Operation Abort
0 = VPP OK

The WSM interrogates VPP level only after the Program or Erase command sequences have been entered and informs the system if VPP has not been switched on. SR.3 bit is not guaranteed to report accurate feedback between VPPLK and VPP1 min.

SR.2 = PROGRAM SUSPEND STATUS (PSS)
1 = Program Suspended
0 = Program in Progress/Completed

When program suspend is issued, WSM halts the execution and sets both WSMS and PSS bits to "1". SR.2 remains set to "1" until a Program Resume command is issued.

SR.1 = SECTOR LOCK STATUS (SLS)
1 =Program/Erase attempted an a locked sector; operation aborted
0 = No operation to locked sectors

If a program or erase operation is attempted to one of the locked sectors, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR. 0 is reserved for future use and should be masked out when polling the status register.

4.0 128-Bit Protection Register

The 128 bits of protection register are divided into two 64-bit segments. One of the segments is programmed at MXIC side with unique 64-bit number; where changes are forbidden. The other segment is left empty for customer to program. Once the customer segment is programmed, it can be locked to prevent further reprogramming.

4.1 Protection Register Read & Programming

The protection register is read in the configuration read mode, which follows the stated Command Bus Definitions.

The device is switched to this read mode by writing the Read Configuration command (90H). Once in this mode, read cycles from addresses shown in Table 6 will retrieve the specified information. To return to read array mode, write the Read Array Command (FFH).

Two-cycle Protection Program Command is used to program protection register bits. The 64-bit number is programmed 16 bits at a time. First, write C0H Protection Program Setup command. The next write to the device will latch in address and data and program the specified location. The allowable address are also shown in Table 6. Refer to Figure 11 for the Protection Register Programming Flowchart.

Any attempt to address Protection Program command onto undefined protection register address space will result in a Status Register error (SR.4 set to "1"). In addition, attempting to program to a previously locked protection register segment will result in a status register error (SR.4=1, SR.1=1).

Table 6. Word-Wide Protection Register Addressing

Word	User	A7	A6	A5	A4	A3	A2	A1	A0
Lock	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	Customer	1	0	0	0	0	1	0	1
5	Customer	1	0	0	0	0	1	1	0
6	Customer	1	0	0	0	0	1	1	1
7	Customer	1	0	0	0	1	0	0	0

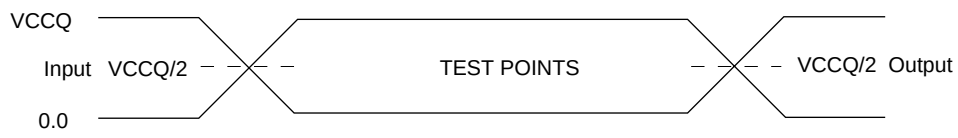
4.2 Protection Register Locking

The user-programmable segment of the protection register is lockable by programming Bit 1 of the PR-Lock location to 0. Bit 0 of this location is programmed to 0 at MXIC to protect the unique device number. This bit is set using the protection program command to program "FFFD" to PR-LOCK location. After these bits have been programmed, no further changes can be made to the value stored in the protection register. Protection Program command to a locked section will result in a status register error (Program Error bit SR.4 and Lock Error bit SR.1 will be set to 1). Protection register lockout state is not reversible.

Table 7. Protection Register Memory Map

Protection Register Bit Address	Purpose
88H~85H	4 words User Program Register
84H~81H	4 words Factory Program Register
80H(Bit0 & Bit1)	Protection Register Lock

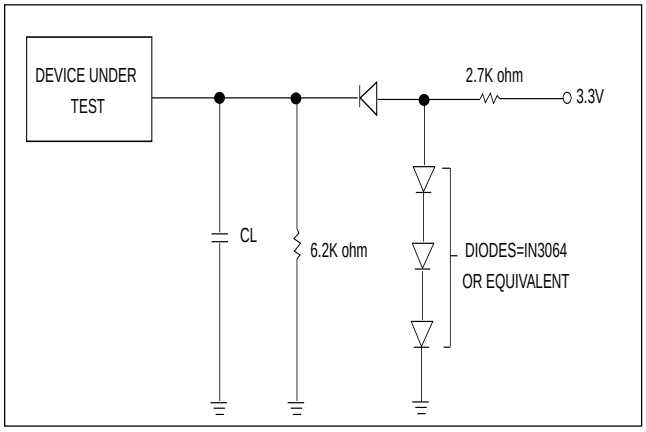
AC Input/Output Test Conditions



Note:AC test inputs are driven at VCCQ/2 for a Logic "1" and 0.0V for a Logic "0".

Figure 1. Transient Input/Output Reference Waveform

Figure 2. SWITCHING TEST CIRCUITS



TEST SPECIFICATIONS

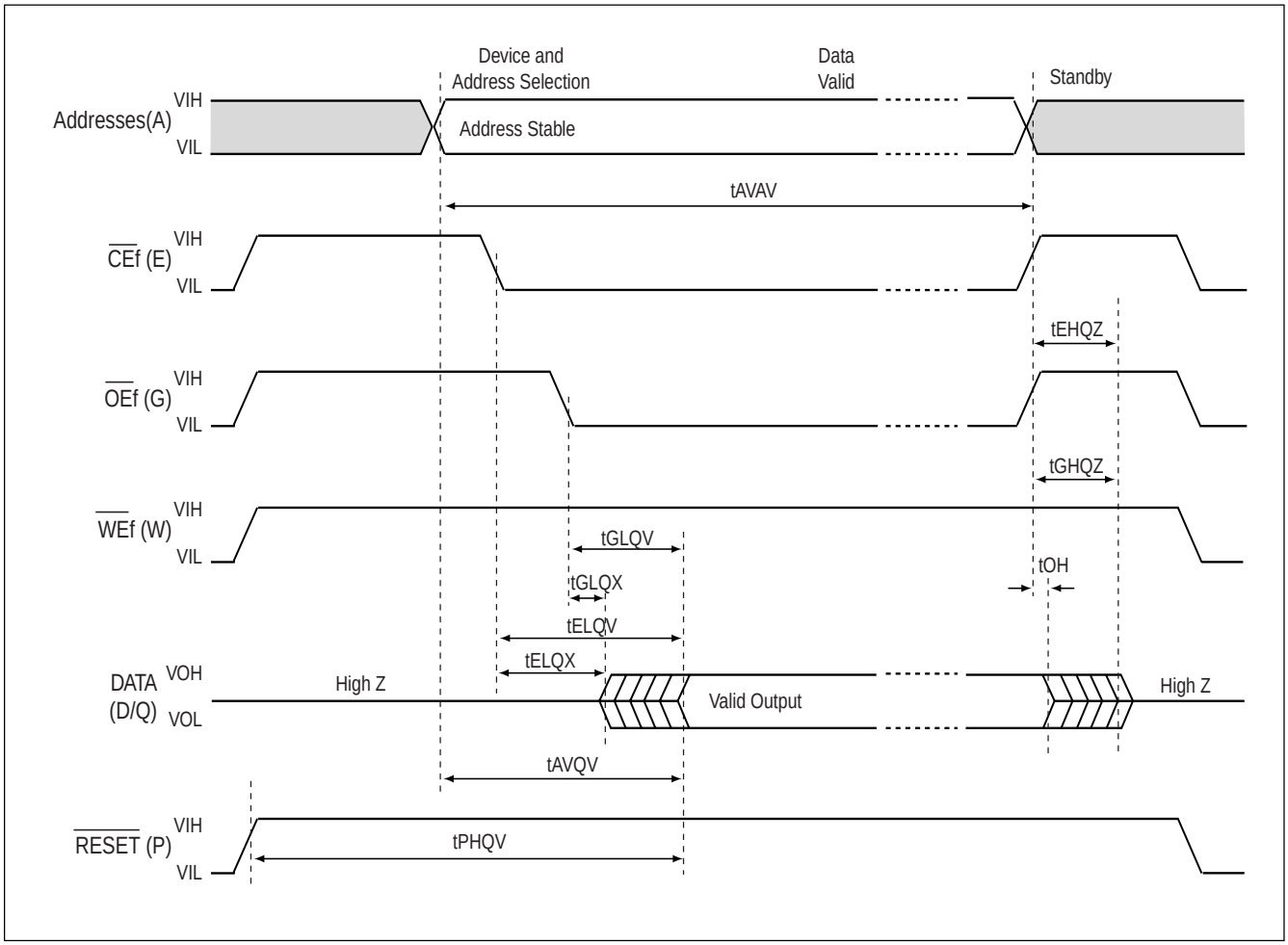
Test Condition	70	90	Unit
Output Load	1 TTL gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

AC Characteristic -- Read Only Operation (1)

Sym.	Parameter	Notes	-70		-90		Unit
			Min.	Max.	Min.	Max.	
tAVAV	Read Cycle Time		70		90		ns
tAVQV	Address to Output Delay			70		90	ns
tELQV	$\overline{CE}$f to Output Delay	2		70		90	ns
tGLQV	$\overline{OE}$f to Output Delay	2		20		30	ns
tPHQV	$\overline{RESET}$ to Output Delay			150		150	ns
tELQX	$\overline{CE}$f to Output in Low Z	3	0		0		ns
tGLQX	$\overline{OE}$f to Output in Low Z	3	0		0		ns
tEHQZ	$\overline{CE}$f to Output in High Z	3		20		20	ns
tGHQZ	$\overline{OE}$f to Output in High Z	3		20		20	ns
tOH	Output Hold from Address, $\overline{CE}$f, or $\overline{OE}$f Change, Whichever Occurs First	3	0		0		ns

Notes:
1. See AC Waveform: Read Operations at Figure 3.
2. $\overline{OE}$f may be delayed up to tELQV-tGLQV after the falling edge of $\overline{CE}$f without impact on tELQV.
3. Sampled, but not 100% tested.
4. See test Configuration.

Figure 3. READ-ONLY OPERATION AC WAVEFORM

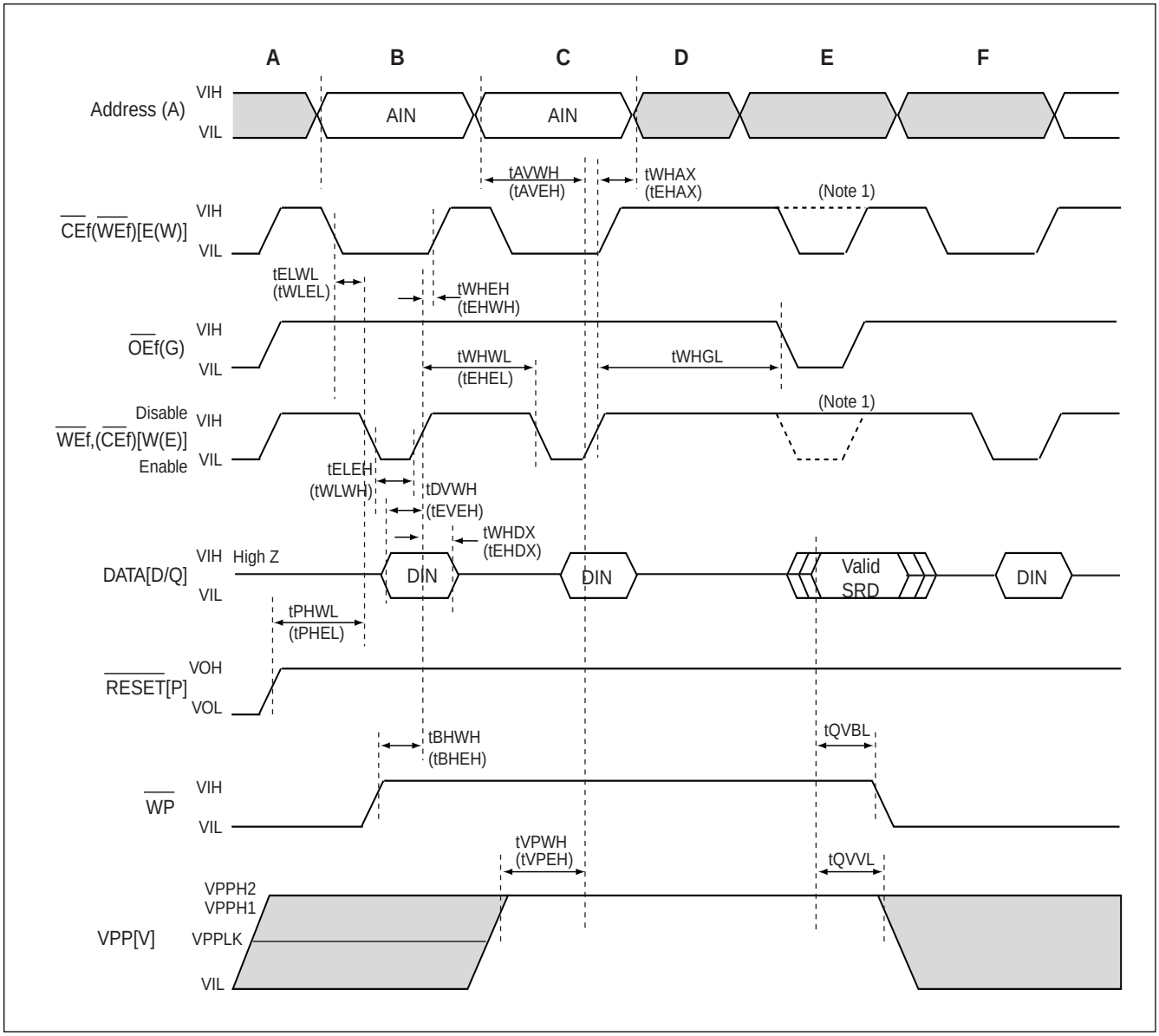


AC Characteristic -- Write Operation

Sym.	Parameter	Note	-70 Min.	-90 Min.	Unit
tPHWL/tPHEL	$\overline{RESET}$ High Recovery to $\overline{WE}$f($\overline{CE}$f) Going Low		150	150	ns
tELWL/tWLEL	$\overline{CE}$f($\overline{WE}$f) Setup to $\overline{WE}$f($\overline{CE}$f) Going Low		0	0	ns
tWLWH/tELEH	$\overline{WE}$f($\overline{CE}$f) Pulse Width	4	45	60	ns
tDVWH/tDVEH	Data Setup to $\overline{WE}$f($\overline{CE}$f) Going High	2	40	50	ns
tAVWH/tAVEH	Address Setup to $\overline{WE}$f($\overline{CE}$f) Going High	2	50	60	ns
tWHEH/tEHWH	$\overline{CE}$f($\overline{WE}$f) Hold Time from $\overline{WE}$f($\overline{CE}$f) High		0	0	ns
tWHDX/tEHDX	Data Hold Time from $\overline{WE}$f($\overline{CE}$f) High	2	0	0	ns
tWHAX/tEHAX	Address Hold Time from $\overline{WE}$f($\overline{CE}$f) High	2	0	0	ns
tWHWL/tEHEL	$\overline{WE}$f($\overline{CE}$f) Pulse Width High	4	25	30	ns
tVPWH/tVPEH	VPP Setup to $\overline{WE}$f($\overline{CE}$f) Going High	3	200	200	ns
tQVVL	VPP Hold from Valid SRD	3	0	0	ns
tBHWH/tBHEH	$\overline{WP}$ Setup to $\overline{WE}$f($\overline{CE}$f)Going High	3	0	0	ns
tQVBL	$\overline{WP}$ Hold from Valid SRD	3	0	0	ns
tWHGL	$\overline{WE}$f High to $\overline{OE}$f Going Low	3	30	30	ns

Notes:
1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. Refer to Table 4 for valid AIN or DIN.
3. Sampled, not 100% tested.
4. Write pulse width (tWP) is defined from $\overline{CE}$f or $\overline{WE}$f going low (whichever goes low last) to $\overline{CE}$f or $\overline{WE}$f going high (whichever goes high first). Hence, tWP=tWLWH=tELEH=tWLEH=tELWH. Similarly, Write pulse width high (tWPH) is defined from $\overline{CE}$f or $\overline{WE}$f going high (whichever goes high first) to $\overline{CE}$f or $\overline{WE}$f going low (whichever goes low first). Hence, tWPH=tWHWL=tEHEL=tWHEL=tEHWL.
5. See Test Configuration.

Figure 4. WRITE AND ERASE OPERATION AC WAVEFORM



Notes:

1. $\overline{CE}$f must be toggled low when reading Status Register Data. $\overline{WE}$f must be inactive (high) when reading Status Register Data.

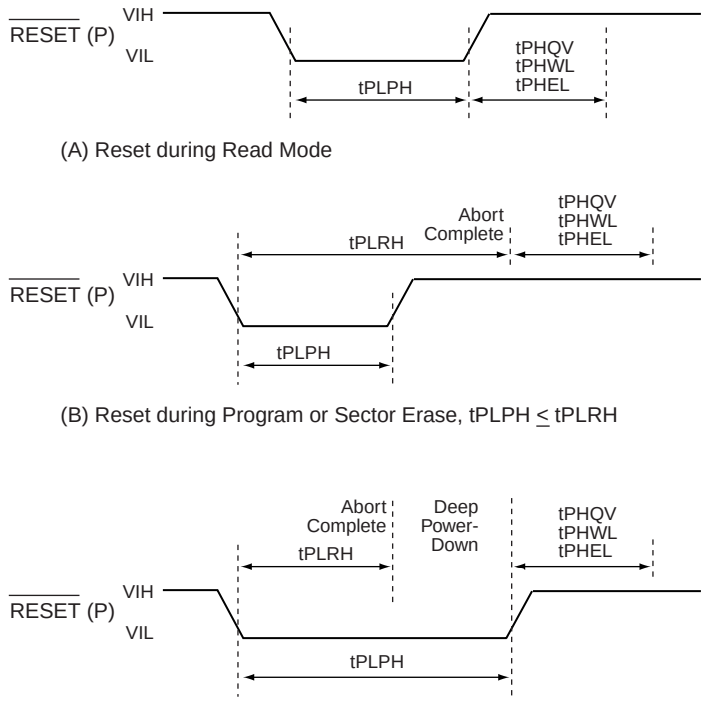
A.VCCf Power-Up and Standby.
B.Write Program or Erase Setup Command.
C.Write Valid Address and Data (for Program) or Erase Confirm Command.
D.Automated Program or Erase Delay.
E.Read Status Register Data (SRD): reflects completed program/erase operation.
F.Write Read Array Command.

Erase and Program Timing (1)

Symbol	Parameter	Vpp Note	1.65V-3.6V		11.4V-12.6V		Unit
			Typ(1)	Max	Typ(1)	Max	
tBWPB	4-KW Parameter Sector Word Program Time	2,3	0.10	0.30	0.03	0.12	s
tBWMB	32-KW Main Sector Word Program Time	2,3	0.8	2.4	0.24	1	s
tWHQV1/ tEHQV1	Word Program Time	2,3	12	200	8	185	us
tWHQV2/ tEHQV2	4-KW Parameter Sector Erase Time	2,3	0.5	4	0.4	4.0	s
tWHQV3/ tEHQV3	32-KW Main Sector Erase Time	2,3	1	5	0.6	5	s
tWHRH1/ tEHRH1	Program Suspend Latency	3	15	20	15	20	us
tWHRH2/ tEHRH2	Erase Suspend Latency	3	15	20	15	20	us

Notes:
1. Typical values measured at TA=+25℃ and nominal voltage.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.

Figure 5. $\overline{\text{RESET}}$ WAVEFORM



AC Characteristic -- Under Reset Operation

Sym.	Parameter	VCCf=2.7V~3.6V		Unit	Notes
		Min.	Max.		
tPLPH	$\overline{\text{RESET}}$ Low to Reset during Read (If $\overline{\text{RESET}}$ is tied to VCCf, this specification is not applicable)	100		ns	1,3
tPLRH1	$\overline{\text{RESET}}$ Low to Reset during Sector Erase		22	us	1,4
tPLRH2	$\overline{\text{RESET}}$ Low to Reset during Program		12	us	1,4

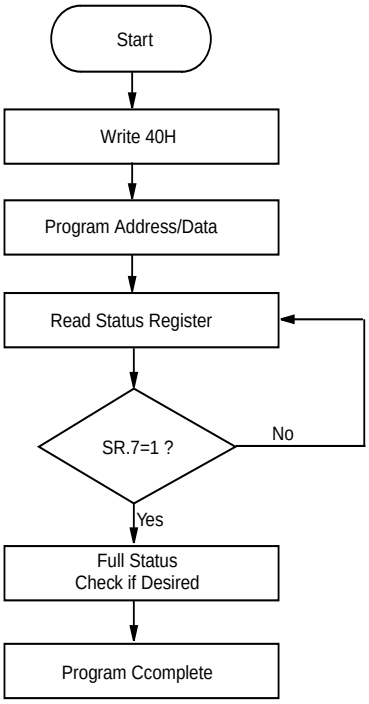
Notes:
1. See Section 3.4 for a full description of these conditions.
2. If tPLPH is < 100ns the device may still reset but this is not guaranteed.
3. If $\overline{\text{RESET}}$ is asserted while a sector erase or word program operation is not executing, the reset will complete within 100ns.
4. Sampled, but not 100% tested.

DC Characteristics

Sym.	Parameter	VCCf / VCCQ	2.7V-3.6V / 2.7V-3.6V		Unit	Test Conditions
		Note	Typ.	Max.		
ILI	Input Load Current	1,2		± 1	uA	VCCf=VCCf Max. ; VCCQ=VCCQ Max. VIN=VCCQ or GND
ILO	Output Leakage Current	1,2	0.2	± 10	uA	VCCf=VCCf Max. ; VCCQ=VCCQ Max. VIN=VCCQ or GND
ICCS	VCC Standby Current	1	7	15	uA	VCCf=VCCf Max. ; $\overline{CE}$f=$\overline{RESET}$=VCCQ or during Program/Erase Suspend $\overline{WP}$=VCCQ or GND
ICCD	VCC Power-Down Current	1,2	7	15	uA	VCCf=VCCf Max. ; VCCQ=VCCQ Max VIN=VCCQ or GND $\overline{RESET}$=GND±0.2V
ICCR	VCC Read Current	1,2,3	9	18	mA	VCCf=VCCf Max. ; VCCQ=VCCQ Max $\overline{OE}$f=VIH, $\overline{CE}$f=VIL, f=5MHz, IOUT=0mA, Inputs=VIL or VIH
IPPD	VPP Deep Power-Down Current	1	0.2	5	uA	$\overline{RESET}$=GND±0.2V VPP ≤ VCCf
IPPR	VPP Read Current	1,4	2	±15	uA	VPP ≤ VCCf
			50	200	uA	VPP > VCCf
ICCW+ IPPW	VCC+VPP Program Current	1,4	18	55	mA	VPP=VPP1, Program in Progress
			10	30	mA	VPP=VPP2(12V), Program in Progress
ICCE+ IPPE	VCC+VPP Erase Current	1,4	21	45	mA	VPP=VPP1, Erase in Progress
			16	45	mA	VPP=VPP2(12V), Erase in Progress
ICCES or ICCWS	VCC Program or Erase Suspend Current	1,4	7	15	uA	$\overline{CE}$f=VCCf, Program or Erase Suspend in Progress
VIL	Input Low Voltage		-0.4	VCCf*0.22V	V	
VIH	Input High Voltage		2.0	VCCQ+0.3V	V	
VOL	Output Low Voltage		-0.1	0.1	V	VCCf=VCCf Min, VCCQ=VCCQ Min IOL=100uA
VOH	Output High Voltage		VCCQ -0.1V		V	VCCf=VCCf Min, VCCQ=VCCQ Min IOH=-100uA
VPPLK	VPP Lock-Out Voltage	6		1.0	V	Complete Write Protection
VPP1	VPP during Program/ Erase Operations	6	1.65	3.6	V	
VPP2		6	11.4	12.6	V	
VLKO	VCC Prog/Erase Lock Voltage		1.5		V	
VLKO2	VCCQ Prog/Erase Lock Voltage		1.2		V	

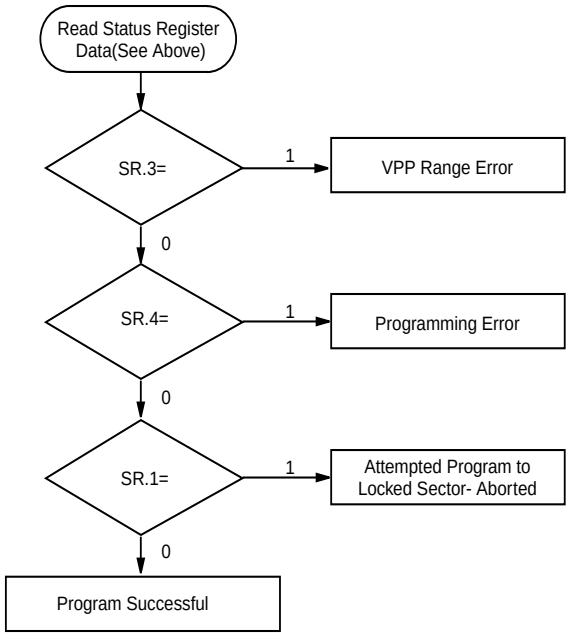
Notes:
1. All currents are in RMS unless otherwise noted. Typical values at nominal VCCf, TA=+25°C.
2. The test conditions VCCf Max, VCCQ Max, VCCf Min, and VCCQ Min refer to the maximum or minimum VCCf or VCCQ voltage listed at the top of each column.
3. Power Savings (Mode) reduces ICCR to approximately standby levels in static operation (CMOS inputs).
4. Sampled, but not 100% tested.
5. ICCES and ICCWS are specified with device de-selected. If device is read while in erase suspend, current draw is sum of ICCES and ICCR. If the device is read while in program suspend, current draw is the sum of ICCWS and ICCR.
6. Erase and Program are inhibited when VPP<VPPLK.

Figure 6. Automated Word Programming Flowchart



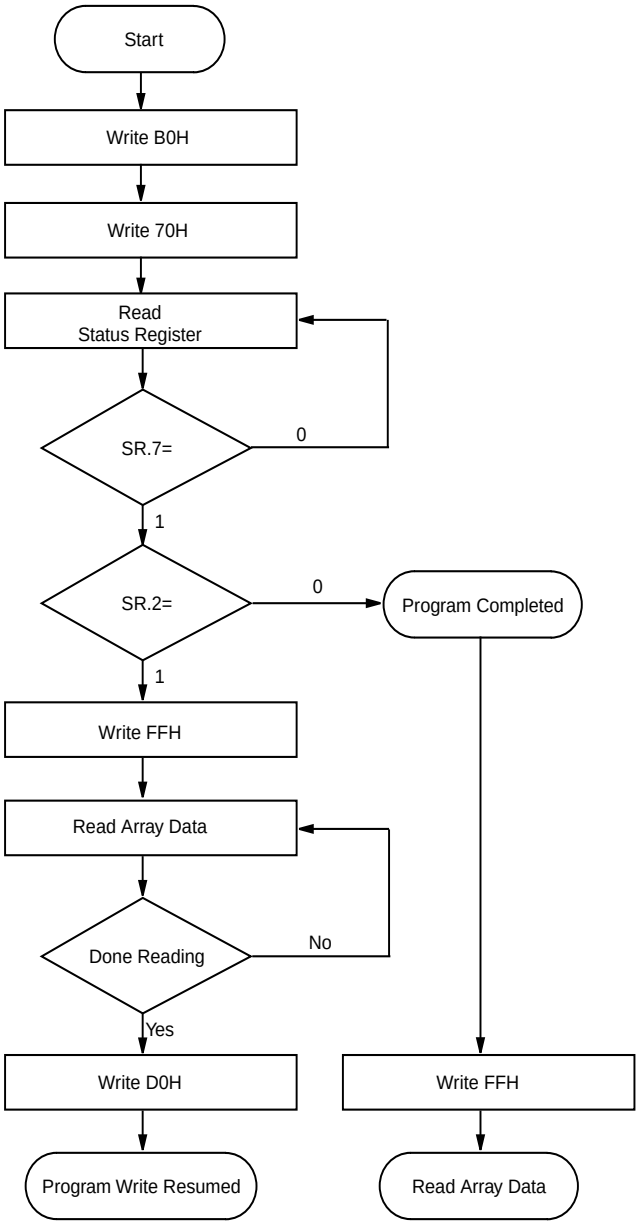
Bus Operation	Command	Comments
Write	Program Setup	Data=40H
Write	Program	Data=Data to Program Addr=Location to Program
Read		Status Register Data Toggle $\overline{CE}$f or $\overline{OE}$f to Update Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent programming operations. SR full status check can be done after each program or after a sequence of program operations. Write FFH after the last program operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



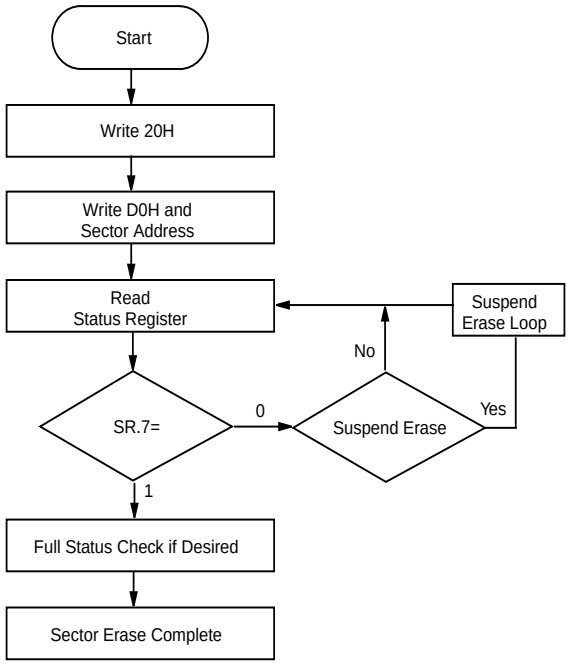
Bus Operation	Command	Comments
Standby		Check SR.3 1=VPP Low Detect
Standby		Check SR.4 1=VPP Program Error
Standby		Check SR.1 1=Attempted Program to Locked Sector-Program Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command, in cases where multiple bytes are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 7. Program Suspend/Resume Flowchart



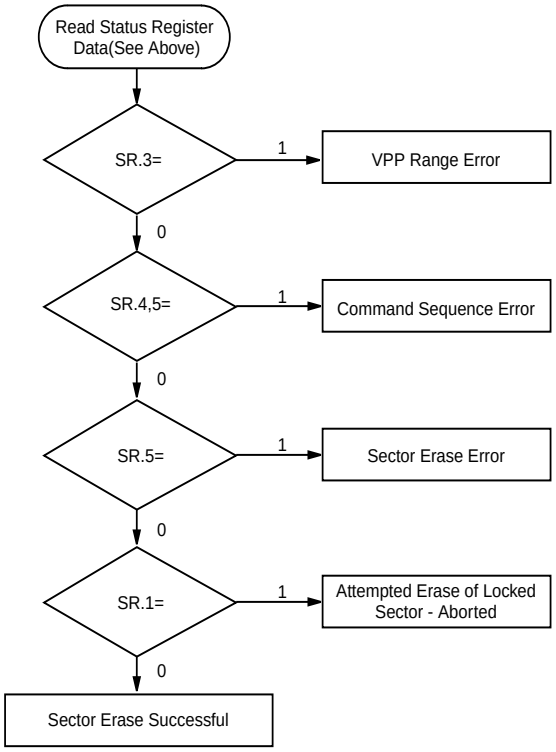
Bus Operation	Command	Comments
Write	Program Suspend	Data=B0H Addr=X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle $\overline{CE}$f or $\overline{OE}$f to Update Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Stanby		Check SR.2 1=Program Suspended 0=Program Completed
Write	Read Array	Data=FFH Addr=X
Read		Read array data from sector other than the one being programmed.
Write	Program Resume	Data=D0H Addr=X

Figure 8. Automated Sector Erase Flowchart



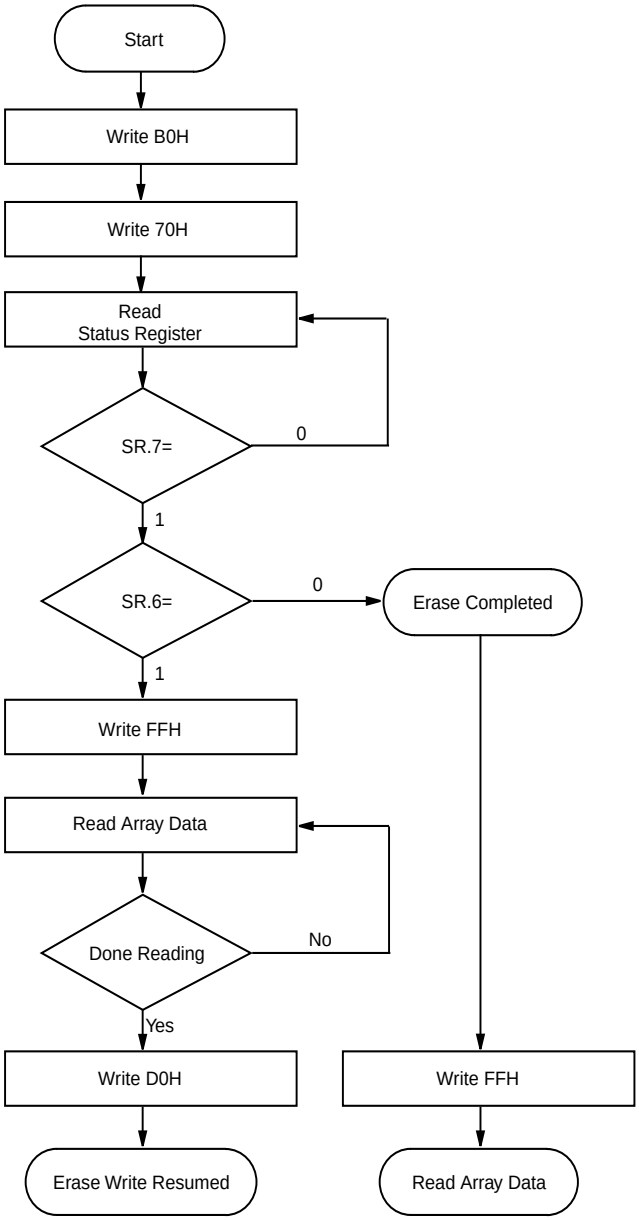
Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Sector to Be Erased
Write	Erase Confirm	Data=D0H Addr=Within Sector to Be Erased
Read		Status Register Data Toggle $\overline{CE}$f or $\overline{OE}$f to Update Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent sector erasures. Full status check can be done after each sector erase or after a sequence of sector erasures. Write FFH after the last write operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



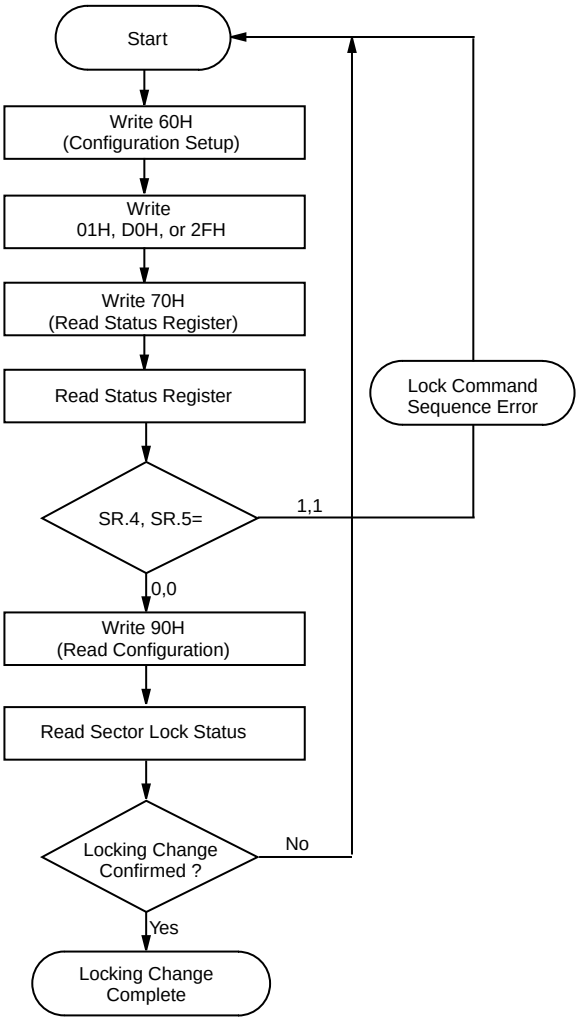
Bus Operation	Command	Comments
Standby		Check SR.3 1=VPP Low Detect
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Sector Erase Error
Standby		Check SR.1 1=Attempted Erase of Locked Sector- Erase Aborted
SR.1 and SR.3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine. SR.1,3,4,5 are only cleared by the Clear Status Register Command, in cases where multiple bytes are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 9. Erase Suspend/Resume Flowchart



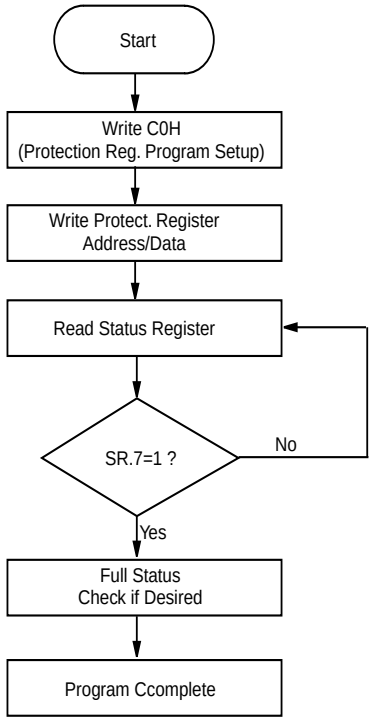
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Write	Read Status	Data=70H Addr=X
Read		Status Register Data Toggle $\overline{CE}$f or $\overline{OE}$f to Update Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Stanby		Check SR.6 1=Erase Suspended 0=Erase Completed
Write	Read Array	Data=FFH Addr=X
Read		Read array data from sector other than the one being erased.
Write	Erase Resume	Data=D0H Addr=X

Figure 10. Locking Operations Flowchart



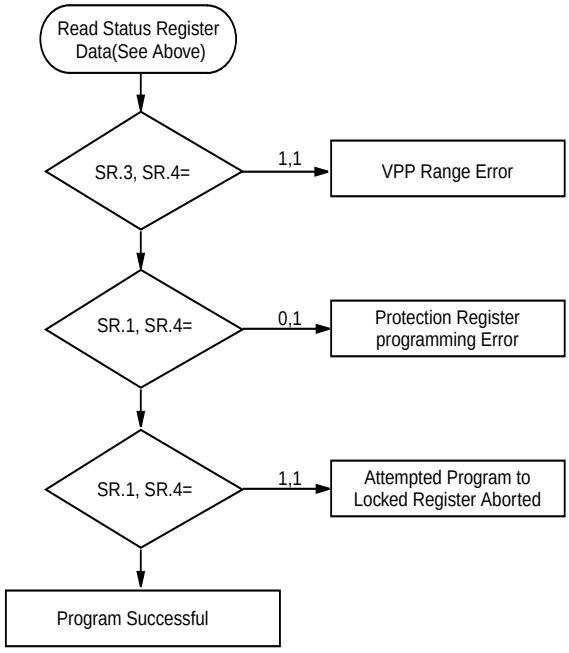
Bus Operation	Command	Comments
Write	Config. Setup	Data=60H Addr=X
Write	Lock, unlock or Lockdown	Data=01H (Sector Lock) D0H(Sector Unlock) 2FH(Sector Lockdown) Addr=Within sector to lock
Write (Optional)	Read Status Register	Data=70H Addr=X
Read (Optional)		Status Register Register Addr=X
Stanby (Optional)		Check Status Register 80H=no error 30H=Lock Command Sequence Error
Write (Optional)	Read Configuration	Data=90H Addr=X
Read (Optional)	Sector Lock Status	Sector Lock Status Data Addr=Second addr of sector
Stanby		Confirm Locking Change on Q1, Q0 (See Sector Locking State Table for valid combinations.)

Figure 11. Protection Register Programming Flowchart



Bus Operation	Command	Comments
Write	Protection Program Setup	Data=C0H
Write	Protection Program	Data=Data to Program Addr=Location to Program
Read		Status Register Data Toggle $\overline{CE}$f or $\overline{OE}$f to Update Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Protection Program operations can only be addressed within the protection register address space. Addresses outside the defined space will return an error. Repeat for subsequent programming operations. SR Full Status Check can be done after each program or after a sequence of program operations. Write FFH after the last operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		SR.1, SR.3, SR.4 0 1 1 VPP Low
Standby		0 0 1 Prot. Reg. Prog. Error
Stanby		1 0 1 Register Locked: Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.1,3,4 are only cleared by the Clear Status Register Command, in cases of multiple protection register program operations before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

5.0 VPP Program and Erase Voltage

MX69F1602/1604C3T/B product provides in-system programming and erase in the 1.65V~3.6V of VPP range. In addition, VPP pin on 12V provides fast production programming.

5.1 VPP Fast manufacturing Programming

When VPP is between 1.65V and 3.6V, all program and erase current is drawn through the VCCf pin. If VPP is driven by a logic signal, VIH=1.65V. That is, VPP must remain above 1.65V to perform in-system flash update/ modifications. When VPP is connected to a 12V power supply, the device draws program and erase current directly from the VPP pin.

5.2 Protection Under VPP<VPPLK

VPP can off additional hardware write protection. The VPP programming voltage can be kept low for the absolute hardware protection of all sector in the flash device. As VPP is below VPPLK, any program or erase operation will result in a error, prompting the corresponding status register bit (SR.3) to be set.

6.0 QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX69F1602/1604C3T/B is capable of operating in the CFI mode. This mode allows the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 2.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Program Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, Program Suspend or read ID mode. The command is valid only when the device is in the CFI mode.

Table 8-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address h	Data h
Query-unique ASCII string "QRY"	10	0051
	11	0052
	12	0059
Primary vendor command set and control interface ID code	13	0003
	14	0000
Address for primary algorithm extended query table	15	0035
	16	0000
Alternate vendor command set and control interface ID code (none)	17	0000
	18	0000
Address for secondary algorithm extended query table (none)	19	0000
	1A	0000

Table 8-2. CFI Mode: System Interface Data Values

Description	Address h	Data h
VCC supply, minimum (2.7V)	1B	0027
VCC supply, maximum (3.6V)	1C	0036
VPP supply, minimum (11.4V)	1D	00B4
VPP supply, maximum (12.6V)	1E	00C6
Typical timeout for single word write (2^N us)	1F	0005
Typical timeout for maximum size buffer write (2^N us)	20	0000
Typical timeout for individual sector erase (2^N ms)	21	000A
Typical timeout for full chip erase (2^N ms) (not supported)	22	0000
Maximum timeout for single word write times (2^N X Typ)	23	0004
Maximum timeout for maximum size buffer write times (2^N X Typ)	24	0000
Maximum timeout for individual sector erase times (2^N X Typ)	25	0003
Maximum timeout for full chip erase times (not supported)	26	0000

Table 8-3. CFI Mode: Device Geometry Data Values

Description	Address h	Data h
Device size (2^n bytes)	27	0015
Flash device interface code (asynchronous x16)	28	0001
	29	0000
Maximum number of bytes in write buffer=2^n (not supported)	2A	0000
	2B	0000
Number of erase sector regions within device (one or more continuous same-size erase sectors at one sector region)	2C	0002
		T B
Erase Sector Region 1 information	2D	1E 07
[2E,2D] = number of same-size sectors in region 1-1	2E	00 00
[30, 2F] = region erase sector size in multiples of 256-bytes	2F	00 20
	30	01 00
		T B
Erase Sector Region 2 information	31	07 1E
[32,31] = number of same-size sectors in region 2-1	32	00 00
[34,33] = region erase sector size in multiples of 256-bytes	33	20 00
	34	00 01

Table 8-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address h	Data h
Query-unique ASCII string "PRI"	35	0050
	36	0052
	37	0049
Major version number, ASCII	38	0031
Minor version number, ASCII	39	0030
Optional Feature & Command Support	3A	66
bit 0 Chip Erase Supported (1=yes, 0=no)	3B	00
bit 1 Suspend Erase Supported (1=yes, 0=no)	3C	00
bit 2 Suspend Program Supported (1=yes, 0=no)	3D	00
bit 3 Lock/Unlock Supported (1=yes, 0=no)		
bit 4 Queued Erase Supported (1=yes, 0=no)		
bit 5 Instant individual sector locking supported (1=yes, 0=no)		
bit 6 Protection bits supported (1=yes, 0=no)		
bit 7 Page mode read supported (1=yes, 0=no)		
bit 8 Synchronous read support (1=yes, 0=no)		
bits 9-31 revered for future use; undefined bits are "0"		
Supported functions after suspend	3E	01
bit 0 Program supported after erase suspend (1=yes, 0=no)		
bit 1-7 Reserved for other supported options; undefined bits are "0"		
Sector Lock Status	3F	03
Define which bits in the sector status Register section of the Query are	40	00
implemented.		
bit 0 sector Lock Status Register Lock/Unlock bit (bit 0) active; (1=yes, 0=no)		
bit 1 sector Lock Status Register Lock-Down bit (bit 1) active; (1=yes, 0=no)		
Bits 2-15 reserved for future use. Undefined bits are "0".		
VCC Logic Supply Optimum Program/Erase Voltage (highest performance)	41	33
bits 7-4 BCD value in volts		
bits 3-0 BCD value in 100mV		
VPP Supply Optimum Program/Erase Voltage	42	C0
bits 7-4 HEX value in volts		
bits 3-0 BCD value in 100mV		
Number of protection register in JEDEC ID space "00" indicates that	43	01
256 protection bytes are available		
Protection Description		
bit 0-7 = Lock/bytes JEDEC-plane physical low address	44	80
bit 8-15 = Lock/bytes JEDEC-plane physical high address	45	00
bit 16-23 = "n" such that 2^n=factory pre-programmed bytes	46	03
bit 24-31 = "n" such that 2^n=user programmed bytes	47	03

2. SRAM--DESCRIPTION

The SRAM of mixed multi chip memory is a high performance, very low power CMOS Static Random Access Memory.

The SRAM of MX69F1602/1604C3T/B is organized as 131,072 words by 16 bits / 262,144 words by 16 bits and operates from a very low range of 2.7V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 1uA and maximum access time of 70ns in 3V operation.

Easy memory expansion is provided by an active HIGH chip enable 2(CE2s) active LOW chip enable ($\overline{CE}$1s) and active LOW output enable ($\overline{OE}$s) and three-state output drivers.

The SRAM of MX69F1602/1604C3T/B has an autmatic power down feature, reducing the power consumption significantly when chip is deselected.

DC ELECTRICAL CHARACTERISTICS

Parameter Name	Parameter	Test Conditions		MIN.	TYP. (1)	MAX.	Units
VIL	Guaranteed Input Low Voltage (2)			-0.3	-	0.6	V
VIH	Guaranteed Input High Voltage (2)			2.2	-	Vcc+0.3	V
IIL	Input Leakage Current	Vccs=Max, VIN=0V to Vcc		-	-	±1	uA
IOL	Output Leakage Current VI/O=0V to Vcc	Vccs=Max, $\overline{CE}$1s=VIH or CE2s=VIL or $\overline{LB}$=$\overline{UB}$=VIH or $\overline{OE}$s=VIH, VI/O=0V to Vcc		-	-	±1	uA
VOL	Output Low Voltage	Vccs=Max, IOL=2mA		-	-	0.4	V
VOH	Output High Voltage	Vccs=Min, IOH=-0.5mA		2.4	-	-	V
ICC1	Active supply current (AC, MOS level)	$\overline{LB}$s and $\overline{UB}$s≤0.2V, $\overline{CE}$1s≤0.2V CE2s≥(Vccs)-0.2V other inputs≤0.2V or ≥(Vccs)-0.2V Output-open (duty 100%)	f=10MHz	-	50	70	mA
			f=1MHz	-	7	15	mA
ICC2	Active supply current (AC, TTL level)	$\overline{LB}$s and $\overline{UB}$s=VIL, $\overline{CE}$1s=VIL CE2s=VIH other inputs=VIH or VIL Output-open (duty 100%)	f=10MHz	-	50	70	mA
			f=1MHz	-	7	15	mA
ICC3	Standby Power Suppply Current (AC, CMOS)	Vcc=max, $\overline{CE}$1s=VIH or CE2s=VIL IDQ=0mA		-	1	40	uA
ICC4	Standby supply current (AC, TTL)	1)CE2s=VIL, Other inputs=0 - Vccs 2)$\overline{CE}$1s=VIH, CE2s=VIH or VIL, Other inputs=0 - Vccs 3) $\overline{LB}$s and $\overline{UB}$s=VIH, $\overline{CE}$1s=VIH or VIL CE2s=VIH or VIL, Other inputs=0 Vccs		-	-	1.0	mA

1.Typical characteristics are at TA=25℃ and Vcc=3.0V
2.These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3.Fmax=1/tRC.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

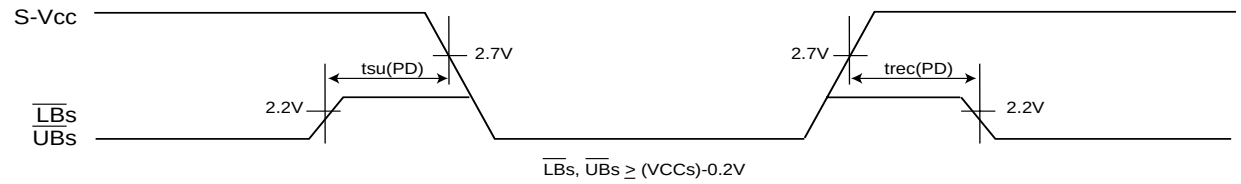
Symbol	Parameter	Test Conditions		Limits MIN.	Limits TYP.	Limits MAX.	Units
S-Vcc(PD)	Power down supply voltage			2.0			V
VI(S-BC)	Byte control input $\overline{LB}$s, $\overline{UB}$s			2.0			V
VI($\overline{CE}$1s)	Chip select input $\overline{CE}$1s			2.0			V
VI(CE2s)	Chip select input CE2s					0.2	V
ICC(PD)	Power Down supply current		+70 ~ +85℃	-	-	30	uA
		VCCs=3.0V	+40 ~ +70℃	-	-	15	uA
		CE2s≤0.2V	+25 ~ +40℃	-	1	3	uA
		other inputs=0~3V	-40 ~ +25℃	-	0.3	1	uA

(2) TIMING REQUIREMENTS

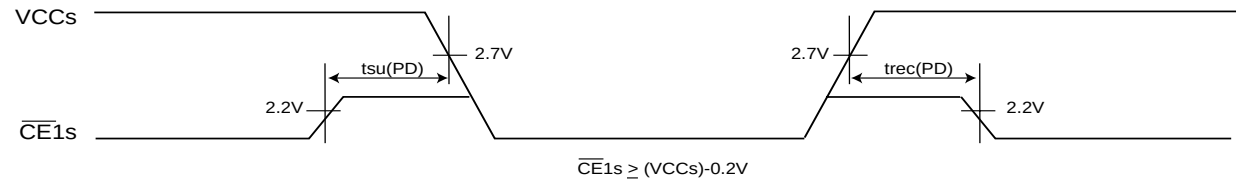
Symbol	Parameter	Test Conditions	Limits MIN.	Limits TYP.	Limits MAX.	Units
tsu(PD)	Power down set up time		0			ns
trec(PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

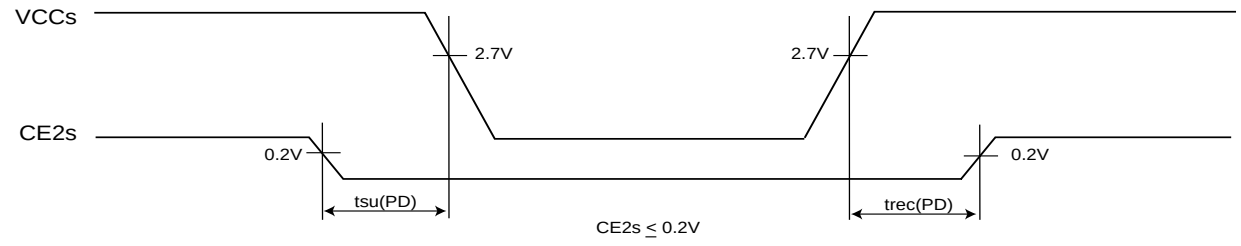
$\overline{LB}$s, $\overline{UB}$s control mode



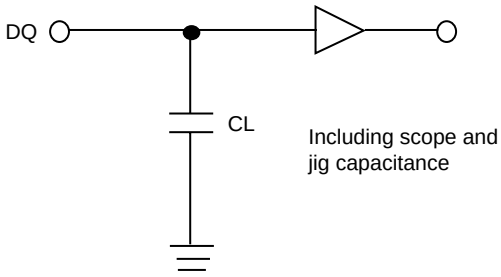
$\overline{CE}$1s control mode



CE2s control mode



AC TEST LOADS AND WAVEFORMS



Output loads: CL=30pF
CL=5pF (for ten. tdis)

FIGURE 1. Output load

AC TEST LOADS AND WAVEFORMS

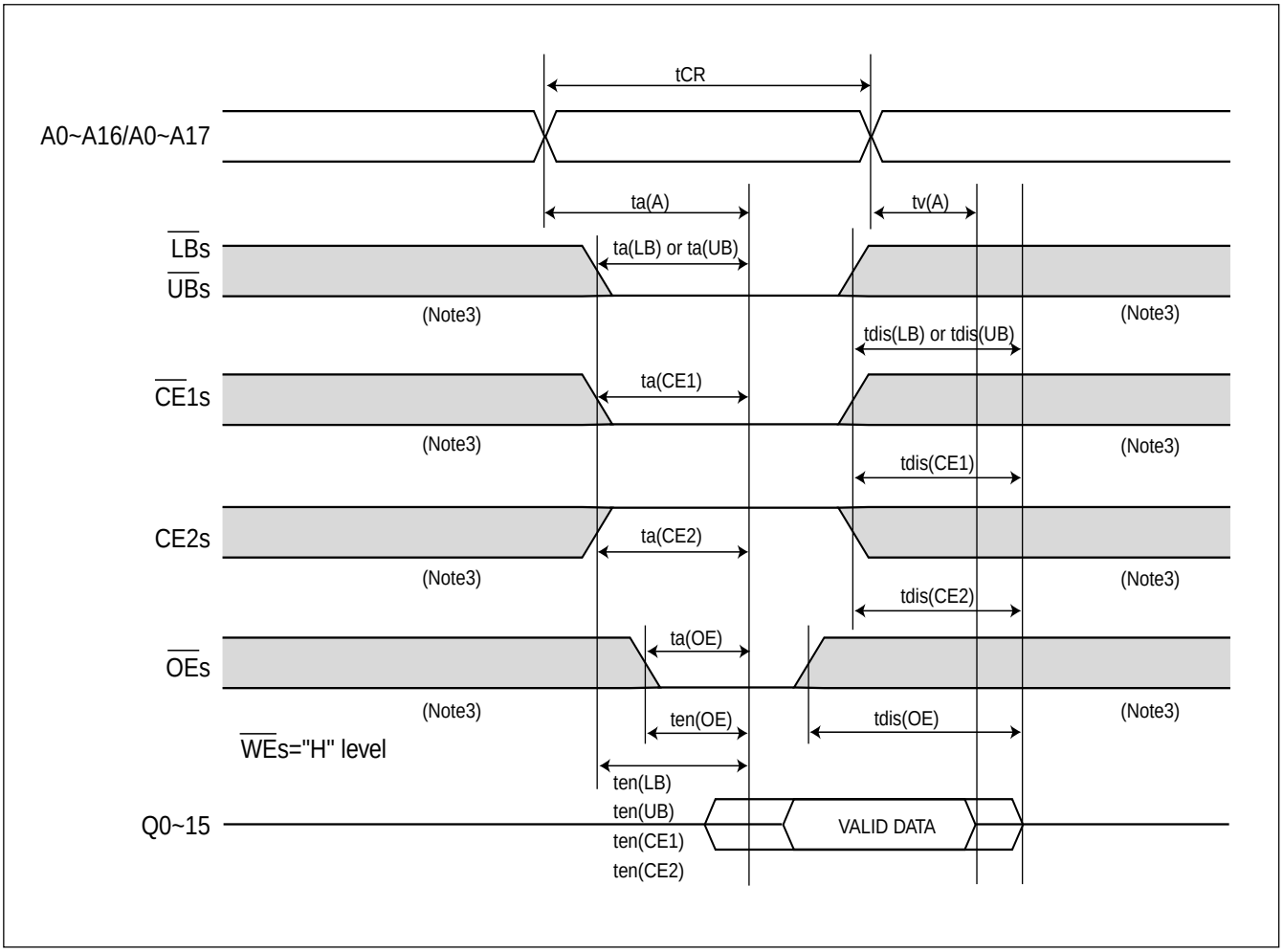
Input Pulse Levels	3.0/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Supply Voltage	2.7V~3.6V

AC ELECTRICAL CHARACTERISTICS

READ CYCLE

Symbol	Parameter	Limits SRAM				Units
		70		85		
		MIN.	MAX.	MIN.	MAX.	
tCR	Read cycle time	70		85		ns
ta(A)	Address access time		70		85	ns
ta(CE1)	Chip select 1 access time		70		85	ns
ta(CE2)	Chip select 2 access time		70		85	ns
ta(LB)	Lower Byte control access time		70		85	ns
ta(UB)	Upper Byte control access time		70		85	ns
ta(OE)	Output enable access time		45		45	ns
tdis(CE1)	Output disable time after $\overline{CE1}$s high		30		30	ns
tdis(CE2)	Output disable time after CE2s low		30		30	ns
tdis(LB)	Output disable time after $\overline{LB}$s high		30		30	ns
tdis(UB)	Output disable time after $\overline{UB}$s high		30		30	ns
tdis(OE)	Output disable time after $\overline{OE}$s high		30		30	ns
ten(CE1)	Output enable time after $\overline{CE1}$s low	10		10		ns
ten(CE2)	Output enable time after CE2s low	10		10		ns
ten(LB)	Output enable time after $\overline{LB}$s low	10		10		ns
ten(UB)	Output enable time after $\overline{UB}$s low	10		10		ns
ten(OE)	Output enable time after $\overline{OE}$s low	5		5		ns
tv(A)	Data valid time after address	10		10		ns

READ CYCLE TIMING DIAGRAMS

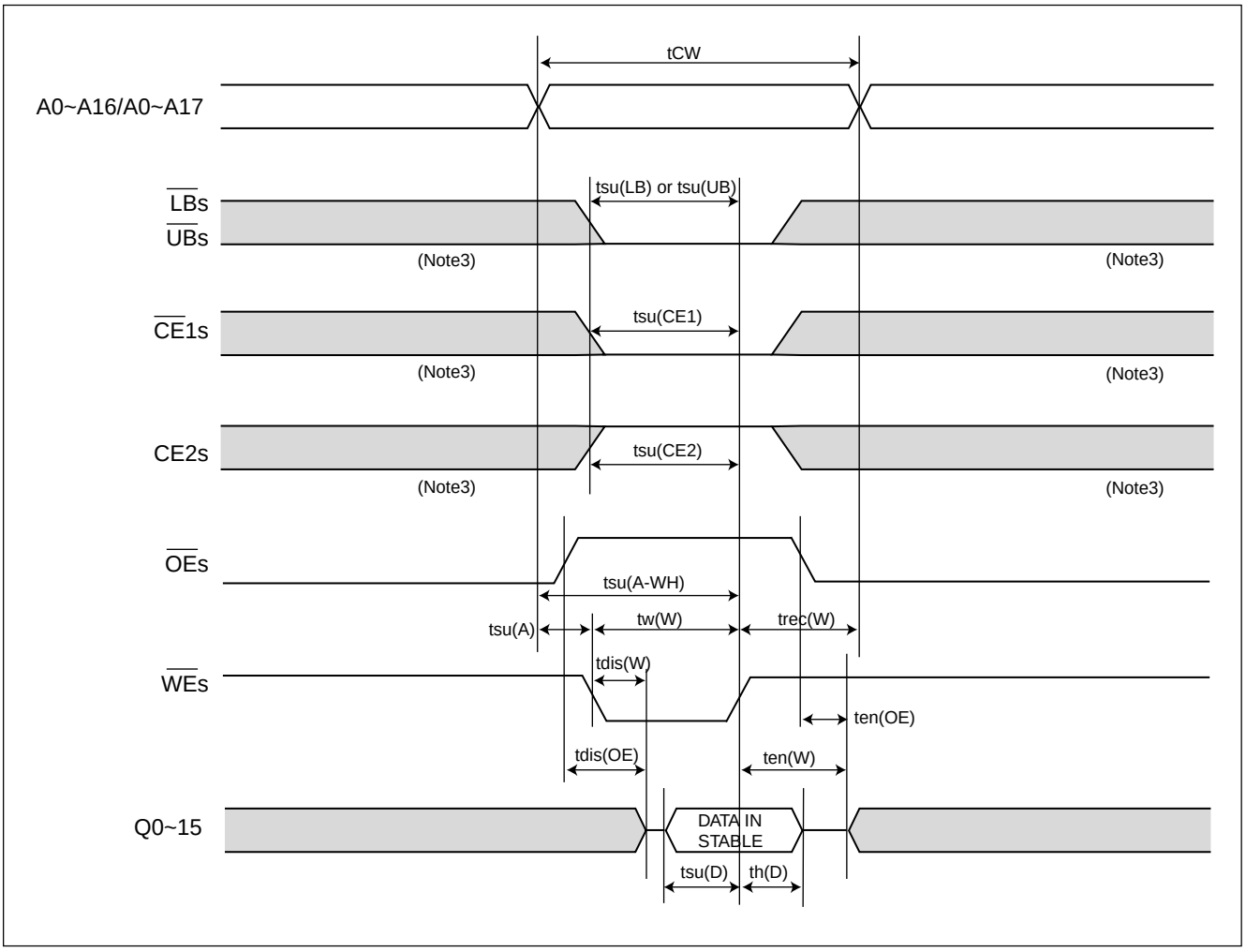


AC ELECTRICAL CHARACTERISTICS

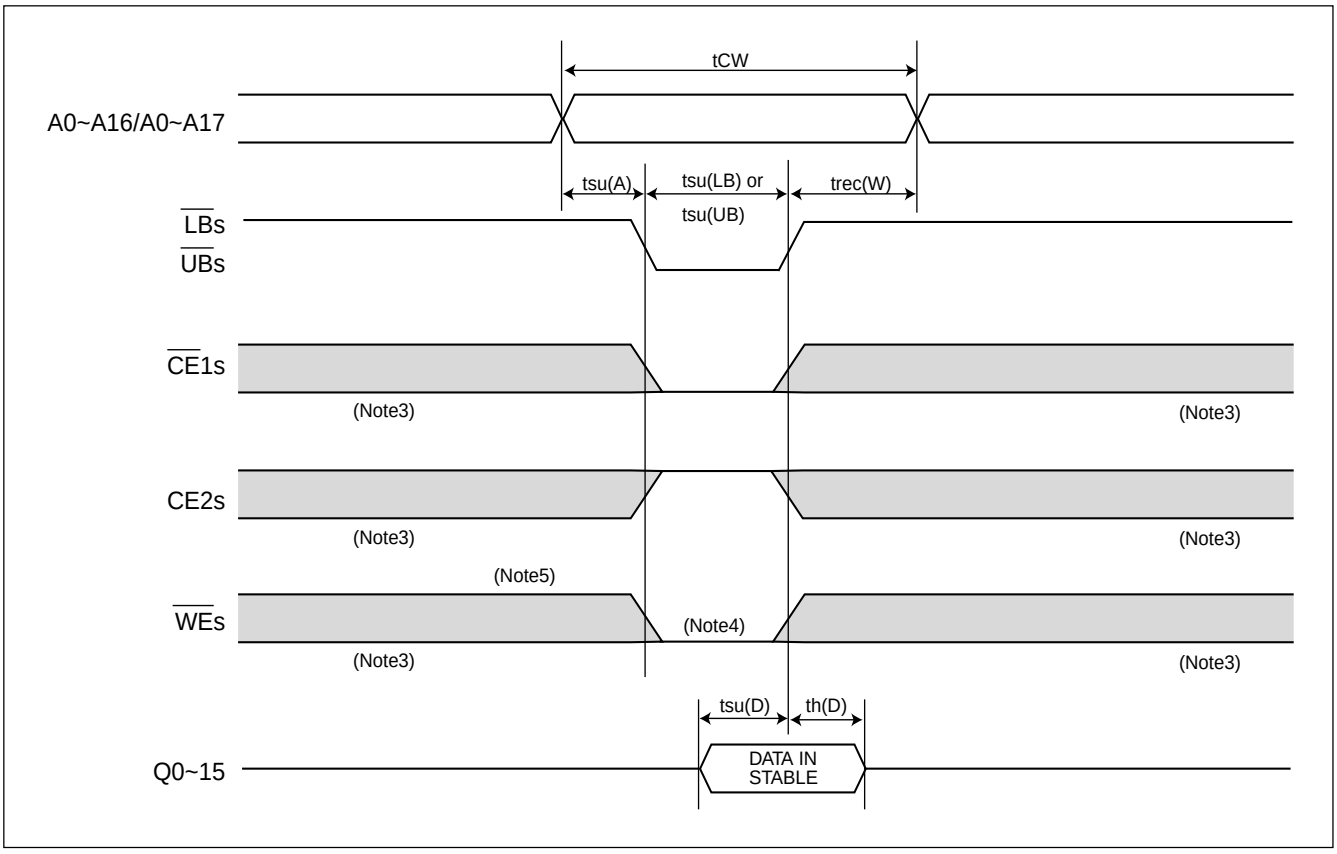
WRITE CYCLE

Symbol	Parameter	Limits SRAM				Units
		70		85		
		MIN.	MAX.	MIN.	MAX.	
tCW	Write cycle time	70		85		ns
tw(W)	Write pulse width	50		50		ns
tsu(A)	Address setup time	0		0		ns
tsu(A-WH)	Address setup time with respect to $\overline{WE}$s	70		70		ns
tsu(LB)	Lower Byte control setup time	70		70		ns
tsu(UB)	Upper Byte control setup time	70		70		ns
tsu(CE1)	Chip select 1 setup time	70		70		ns
tsu(CE2)	Chip select 2 setup time	70		70		ns
tsu(D)	Data setup time	35		35		ns
th(D)	Data hold time	0		0		ns
trec(W)	Write recovery time	0		0		ns
tdis(W)	Output disable time $\overline{WE}$s low		30		30	ns
tdis(OE)	Output disable time $\overline{OE}$s high		30		30	ns
ten(W)	Output enable time $\overline{WE}$s high	5		5		ns
ten(OE)	Output enable time from $\overline{OE}$s low	5		5		ns

WRITE CYCLE ($\overline{WE}$s control mode)

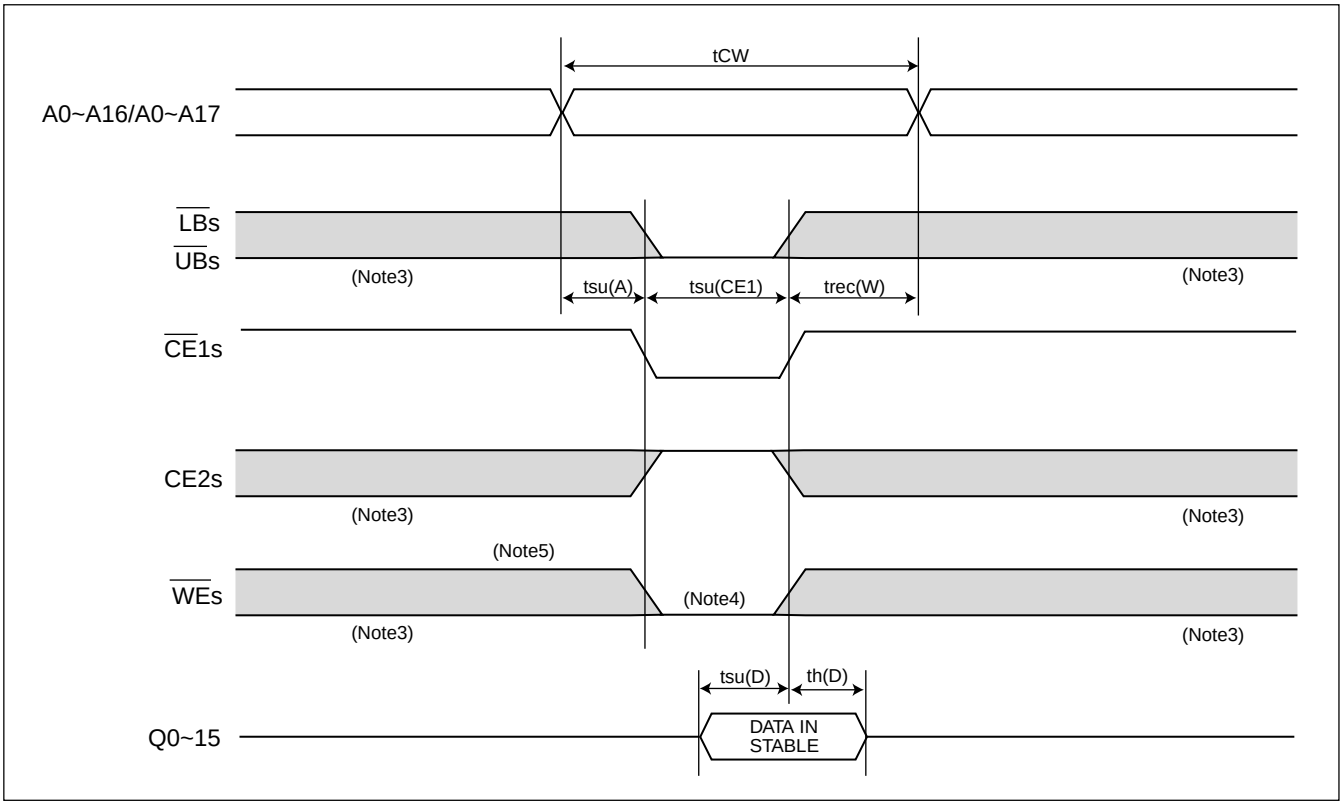


WRITE CYCLE ($\overline{LB}$s, $\overline{UB}$s control mode)

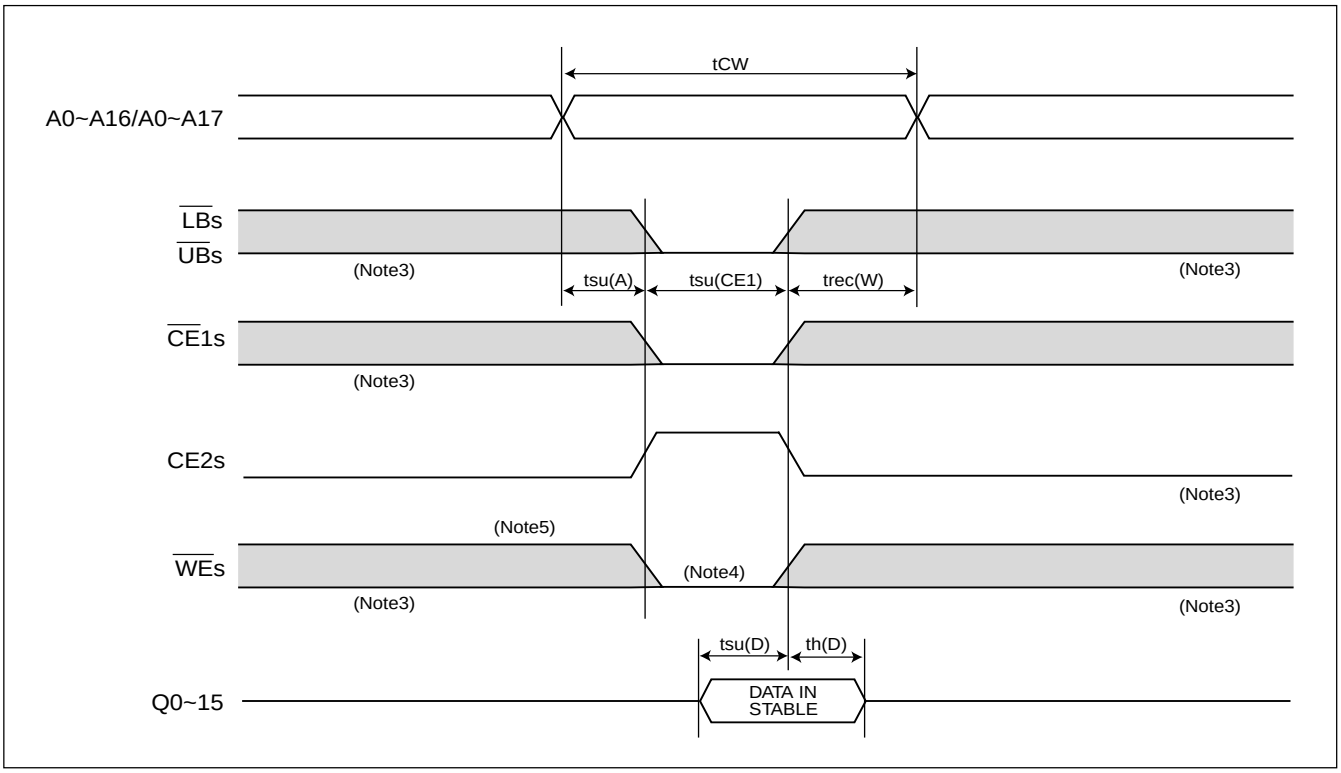


Note 3: Hatching indicates the state is "don't care".
Note 4: A Write occurs during $\overline{CE}$1s low, CE2s high overlaps $\overline{LB}$s and/or $\overline{UB}$s low and $\overline{WE}$s low.
Note 5: When the falling edge of $\overline{WE}$s is simultaneously or prior to the falling edge of $\overline{LB}$s and/or $\overline{UB}$s or the falling edge of $\overline{CE}$1s or rising edge of $\overline{CE}$2s the outputs are maintained in the high impedance state.
Note 6: Don't apply inverted phase signal externally when I/O pin is in output mode.

WRITE CYCLE ($\overline{CE1s}$ control mode)



WRITE CYCLE (CE2s control mode)



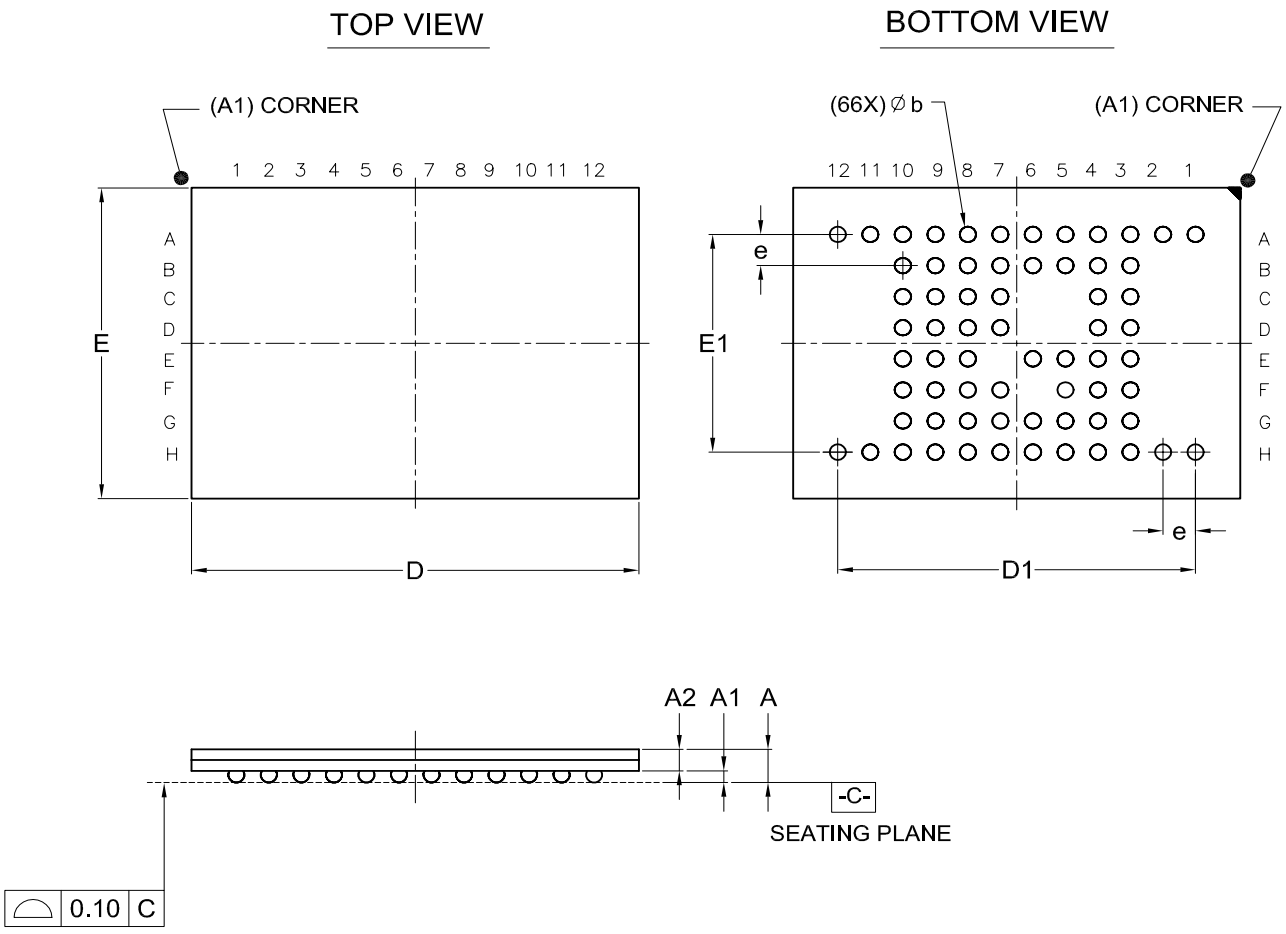
ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	Access Time (ns)	Temperature Range	Type	Package Type	Ball Pitch
MX69F1602C3TXBI-70	70	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1602C3BXBI-70	70	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1602C3TXBI-90	90	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1602C3BXBI-90	90	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1604C3TXBI-70	70	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1604C3BXBI-70	70	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1604C3TXBI-90	90	-40~85℃	66 Ball FBGA	FBGA	0.8mm
MX69F1604C3BXBI-90	90	-40~85℃	66 Ball FBGA	FBGA	0.8mm

PACKAGE INFORMATION

Title: Package Outline for CSP 66BALL(11X8X1.4MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.85	0.35	10.90		7.90		
	Nom.	---	0.30	---	0.40	11.00	8.80	8.00	5.60	0.80
	Max.	1.40	0.35	---	0.45	11.10		8.10		
Inch	Min.	---	0.010	0.033	0.014	0.429		0.311		
	Nom.	---	0.012	—	0.016	0.433	0.346	0.315	0.220	0.031
	Max.	0.055	0.014	—	0.018	0.437		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4221	4	MO-219			10-28-'02

REVISION HISTORY

Revision No.	Description	Page	Date
0.1	1. Add Package Information	P49	NOV/06/2002
0.2	1. Changed Part No. from MX28F1602/1604C3T/B to MX69F1602/1604C3T/B	All	NOV/20/2002
0.3	1. Modified Pin Assignment	P4	NOV/22/2002
0.4	1. Changed package size from 10x8x1.4mm to 11x8x1.4mm	P2,4	MAR/06/2003
0.5	1. Modified absolute maximum ratings	P7	JUL/09/2003

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