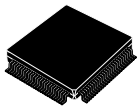
MTC20454

QUAD INTEGRATED ADSL CMOS ANALOG FRONT END CIRCUIT

- Fully integrated quad AFE for ADSL
- Overall 12 bit resolution
- 1.1MHz signal bandwidth
- 8.8 MS/s ADC
- 8.8 MS/s DAC
- THD: -60 dB @ full scale
- 1 V full scale input
- Differential analog I/O
- Accurate continuous-time channel filtering
- 3rd & 4th order tuneable continuous time LP Filters
- 100 pin TQFP package, Industrial Range qualified
- 175 mW power consumption per line



TQFP100 14x14x1.4
ORDERING NUMBER: MTC20454-TQ-I

APPLICATIONS

- ADSL Front-end for high density, low power central office and digital loop carrier equipment

DESCRIPTION

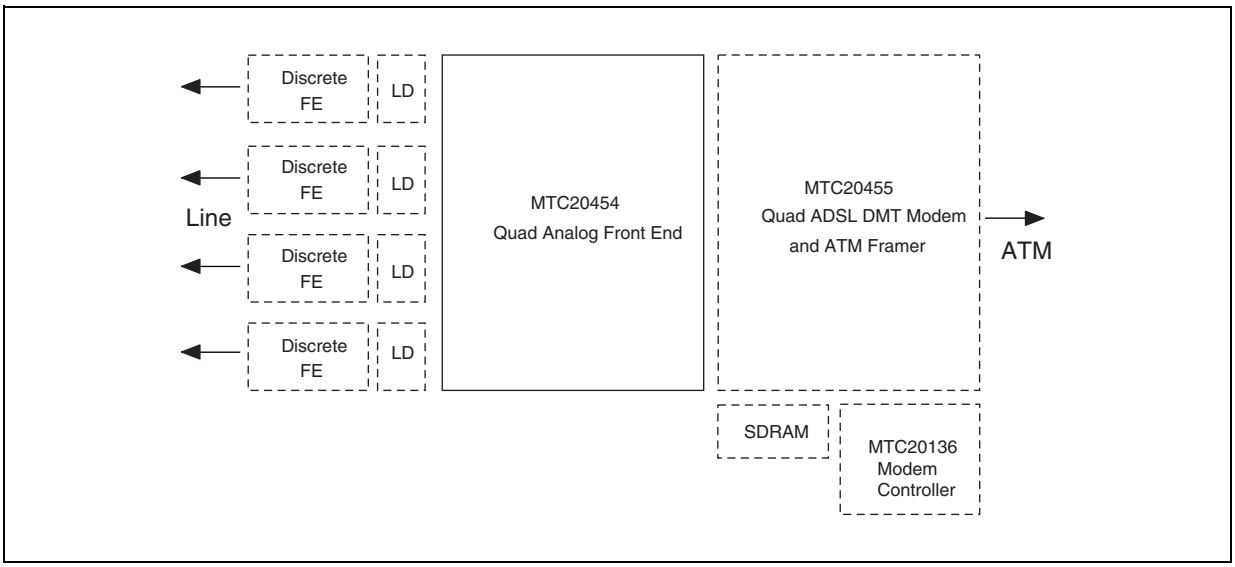
The MTC20454 is the first DynaMiTe ADSL (Asynchronous Digital Subscriber Line) analog front end designed specifically for the central office. It is a fifth generation Analog Front End (AFE) designed for DMT based ADSL modems compliant with ITU G.992.1 and G.992.1 standards. It includes four 12 bit DACs and one 13 bit ADC.

It is intended to be used with the MTC20455 DMT/ ATM processor as part of the MTK20450. The MTC20454 provides programmable low pass filters for each of the two channels and automatic gain control for four individual ADSL modems.

The pipeline ADC architecture provides 13 bit dynamic range and a signal bandwidth of 1.1 MHz. The device consumes only 0.7 Watt in full operation of all four modems and has a power down mode for standby.

It is housed in a compact 100 pin thin plastic quad flat package.

Figure 1. Sample board layout



PIN DESCRIPTION

N°	Pin	Description	Connection	Type
Digital Interface				
1	DVSS	Negative supply for input IOs + core	Dig supply	VSSI
2	TX7	Transmit data bus bit 7 (MSB)	MTC-20455	SCHMITTC
3	TX6	Transmit data bus bit 6	MTC-20455	SCHMITTC
4	TX5	Transmit data bus bit 5	MTC-20455	SCHMITTC
5	TX4	Transmit data bus bit 4	MTC-20455	SCHMITTC
6	TX3	Transmit data bus bit 3	MTC-20455	SCHMITTC
7	TX2	Transmit data bus bit 2	MTC-20455	SCHMITTC
8	TX1	Transmit data bus bit 1	MTC-20455	SCHMITTC
9	TX0	Transmit data bus bit 0 (LSB)	MTC-20455	SCHMITTC
10	CTRLIN	Serial control interface input	MTC-20455	SCHMITTC
11	CLKIN	Master clock (35.328MHz) input	System	SCHMITTC
12	DVDD	Positive supply for input IOs + core	Dig supply	VDDI
13	DVDD	Positive supply for output IOs	Dig supply	VDDE
14	CLKM	Master clock output	System	BD4SCR
15	CLKWD	Word clock output	System	BT4CR
16	RX3	Receive data bus bit 3 (MSB)	MTC-20455	BT4CR
17	RX2	Receive data bus bit 2	MTC-20455	BT4CR
18	RX1	Receive data bus bit 1	MTC-20455	BT4CR
19	RX0	Receive data bus bit 0 (LSB)	MTC-20455	BT4CR
20	DVSS	Negative supply for output IOs	Dig supply	VSSE
98	ONELINE	If high: TX, RX itfce is MTC-20455 compatible	System	SCHMITTC
99	RESETN	General reset (active low)	System	SCHMITTC
100	TEST	Test mode selection (static)	Strap	SCHMITTC
Analog Interface				
21	AVSSADC	ADC analog negative supply	Ana supply	VSSI
25	AVDDADC	ADC analog positive supply	Ana supply	VDDI
28	VREF	ADC virtual ground decoupling	C network	OANA
29	VRAN	ADC negative reference decoupling	C network	OANA
30	VRAP	ADC positive reference decoupling	C network	OANA
32	DACVREF	DAC's voltage reference decoupling	C network	OANA
34	L3GP0	Analog general purpose control pin - Line3	Board	BT4CR
35	AVDDDAC	DAC's analog positive supply	Ana supply	VDDI
37	L3GP1	Analog general purpose control pin - Line3	Board	BT4CR
38	L2GP0	Analog general purpose control pin - Line2	Board	BT4CR
39	L2GP1	Analog general purpose control pin - Line2	Board	BT4CR
40	AVSSDAC	DAC's analog negative supply	Ana supply	VSSI
41	AVSSDS	DS filters analog negative supply	Ana supply	VSSI
42	L3DRVSD	External TX driver shutdown - Line3	TX driver	BT4CR
43	AVDDDS	DS filters analog positive supply	Ana supply	VSSI
44	AVDD TXDRV	Internal TX pre-drivers positive supply	Ana supply	VDDI
45	L3DRV0	External TX driver bias control LSB - Line3	TX driver	BT4CR
46	AVSS TXDRV	Internal pre-drivers negative supply	Ana supply	VSSI
47	L3DRV1	External TX driver bias control MSB - Line3	TX driver	BT4CR
48	L2DRVSD	External TX driver shutdown - Line2	TX driver	BT4CR
49	L2DRV0	External TX driver bias control LSB - Line2	TX driver	BT4CR
50	L2DRV1	External TX driver bias control MSB - Line2	TX driver	BT4CR

PIN DESCRIPTION (continued)

N°	Pin	Description	Connection	Type
51	L3AVSSLNA	LNA analog negative supply - Line3	Ana suppply	VSSI
52	L3RXN	Analog RX signal negative input (diff) - Line3	RX input	OANA
53	L3RXP	Analog RX signal positive input (diff) - Line3	RX input	OANA
54	L3AVDDLNA	LNA analog positive supply - Line3	Ana supply	VDDI
55	L3TXN	Analog TX signal negative output (diff) - Line3	TX output	OANA
56	L3TXP	Analog TX signal positive output (diff) - Line3	TX output	OANA
57	L2AVSSLNA	LNA analog negative supply - Line2	Ana supply	VSSI
58	L2RXN	Analog RX signal negative input (diff) - Line 2	RX input	OANA
59	L2RXP	Analog RX signal positive input (diff) - Line2	RX input	OANA
60	L2AVDDLNA	LNA analog positive supply - Line 2	Ana supply	VDDI
61	L2TXN	Analog TX signal negative output (diff) - Line2	TX output	OANA
62	L2TXP	Analog TX signal positive output (diff) - Line2	TX output	OANA
63	L1AVSSLNA	LNA analog negative supply - Line1	Ana supply	VSSI
64	L1RXN	Analog RX signal negative input (diff) - Line1	RX input	OANA
65	L1RXP	Analog RX signal positive input (diff) - Line1	RX input	OANA
66	L1AVDDLNA	LNA analog positive supply - Line1	Ana supply	VDDI
67	L1TXN	Analog TX signal negative output (diff) - Line1	TX output	OANA
68	L1TXP	Analog TX signal positive output (diff) - Line1	TX output	OANA
69	L0AVSSLNA	LNA analog negative supply - Line0	Ana supply	VSSI
70	L0RXN	Analog RX signal negative input (diff) - Line0	RX input	OANA
71	L0RXP	Analog RX signal positive input (diff) - Line0	RX input	OANA
72	L0AVDDLNA	LNA analog positive supply - Line0	Ana supply	VDDI
73	L0TXN	Analog TX signal negative output (diff) - Line0	TX output	OANA
74	L0TXP	Analog TX signal positive output (diff) - Line0	TX output	OANA
75	VAGND	Analog virtual ground	C network	OANA
76	L1DRVSD	External TX driver shutdown - Line1	TX driver	BT4CR
77	L1DRV1	External TX driver bias control MSB - Line1	TX driver	BT4CR
78	L1DRV0	External TX driver bias control LSB - Line1	TX driver	BT4CR
79	L0DRVSD	External TX driver shutdown - Line0	TX driver	BT4CR
80	AVSS TXDRV	Internal pre-drivers negative supply	Ana supply	VSS
81	L0DRV1	External TX driver bias control MSB - Line0	TX driver	BT4CR
82	AVDD TXDRV	Internal TX pre-drivers positive supply	Ana supply	VDDI
83	AVDDDS	DS filters analog positive supply	Ana supply	VSSI
84	L0DRV0	External TX driver bias control LSB - Line0	TX driver	BT4CR
85	AVSSDS	DS filters analog negative supply	Ana supply	VSSI
86	AVSSDAC	DAC's analog negative supply	Ana supply	VSSI
89	L1GP0	Analog general purpose control pin - Line1	Board	BT4CR
90	L1GP1	Analog general purpose control pin - Line1	Board	BT4CR
91	AVDDDAC	DAC analog positive supply	Ana supply	VDDI
92	L0GP0	Analog general purpose control pin - Line0	Board	BT4CR
93	L0GP1	Analog general purpose control pin - Line0	Board	BT4CR
Analog Test Access Interface				
87	TOP	Pos. diff. output test access	Test	Analog
88	TON	Neg. diff output test access	Test	Analog
94	TIN	Pos. diff input test access	Test	Analog
95	TIP	Neg. diff inp0ut test access	Test	Analog

Figure 2. MTC20454 Grounding and Decoupling Networks

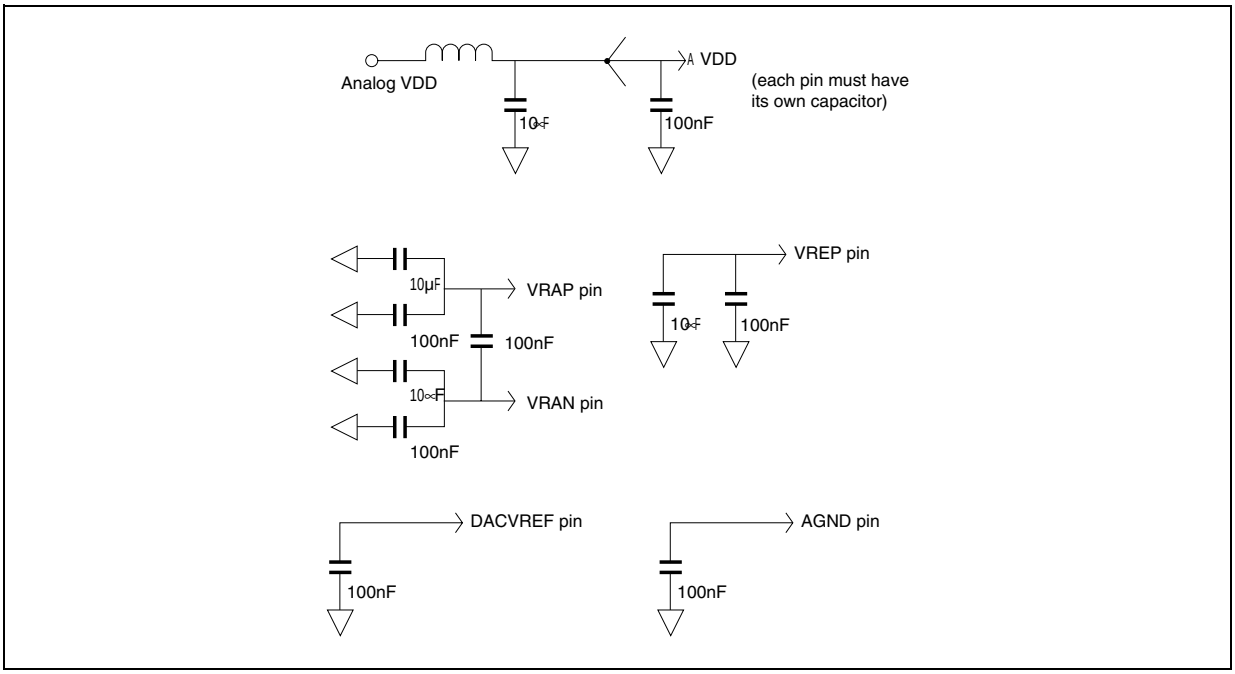
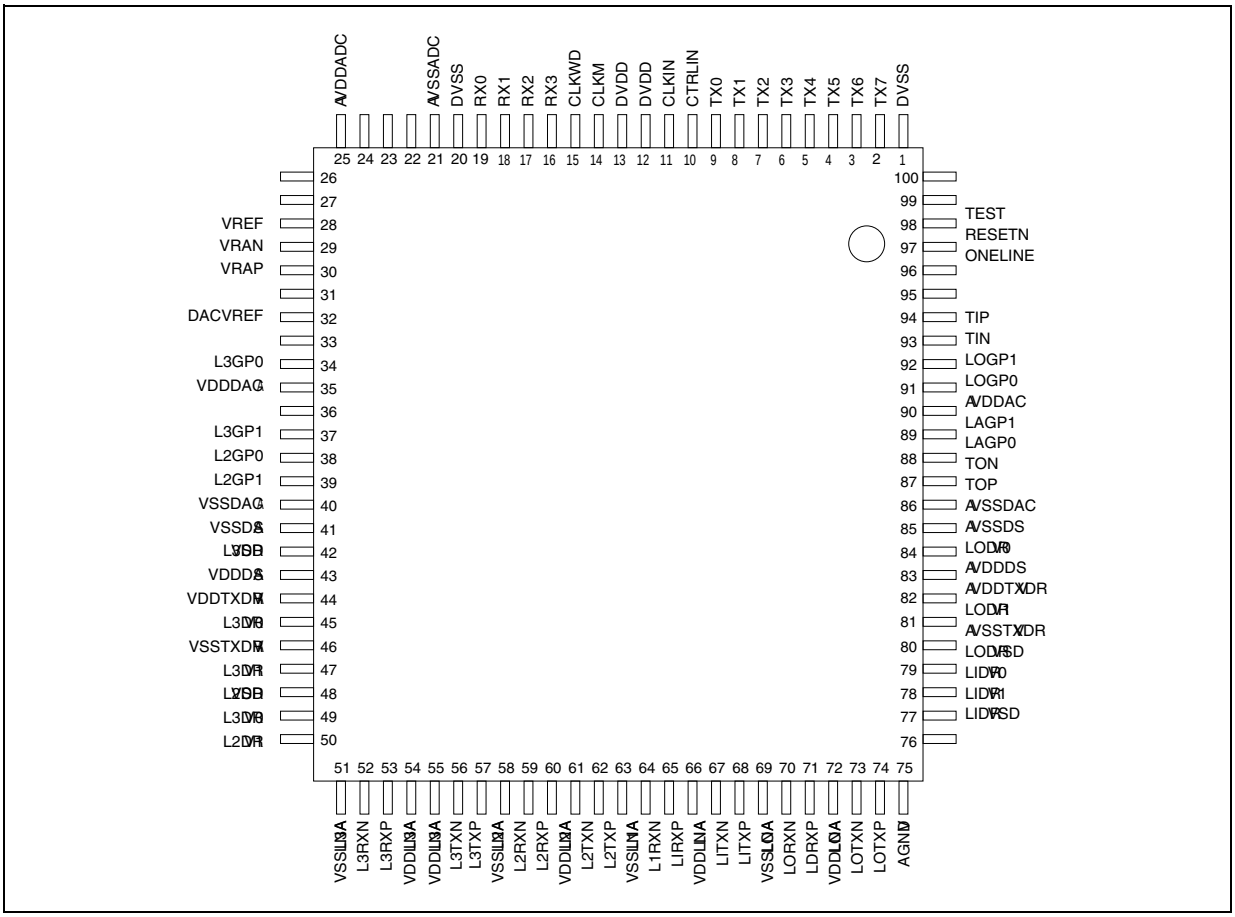


Figure 3. PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Operation of the device beyond these limits may cause permanent damage. It is not implied that more than one of these conditions can be applied simultaneously.

Symbol	Parameter Description	Min	Max	Unit
V_{DD}	Any V_{DD} supply voltage, related to substrate	-0.5	5	Vhh
V_{in}	Voltage at any input pin	-0.5	VDD + 0.5	V
T_{stg}	Storage Temperature	-40	125	°C
T_L	Lead Temperature (10 second soldering)		300	°C
ILU	Latch-up current @ 80°C	100		mA

OPERATING CONDITIONS

Unless specified, the characteristic limits of 'Static characteristics' in this document apply for the following operating conditions:

Symbol	Parameter Description	Min	Max	Unit
AV_{DD}	AVDD supply voltage, related to substrate	3.0	3.6	V
DV_{DD}	DVDD supply voltage, related to substrate	2.7	3.6	V
V_{in}, V_{out}	Voltage at any input and output pin	0	V_{DD}	V
P_d	Power Dissipation	0.4	0.6	W
T_{amb}	Ambient Temperature	-40	85	°C
T_j	Junction temperature	-40	110	°C

ELECTRICAL CHARACTERISTICS

Static Characteristics

a. Digital Inputs

Schmitt-trigger inputs: TXi, CTRLIN, CLKIN, RESETN, TEST

Clock Driver Input

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage				$0.2*DV_{DD}$	V
V_{IH}	High level input voltage		$0.8*DV_{DD}$			V
V_H	Hysteresis		1.0		1.3	V
C_{inp}	Input capacitance				3	pF

b. Digital Outputs

Hard driven outputs: RXi, CLKWD, LiGPi, LiDRVi, LiDRVSD

Clock Driver Output

Symbol	Parameters	Test Cond	Min		Max	Unit
V_{OL}	Low level output voltage	Iout = 4 mA			$.15*DV_{DD}$	V
V_{OH}	High level output voltage	Iout = 4 mA	$.85*DV_{DD}$			V
C_{load}	Load capacitance		1.0		30	pF

Clock Driver Output CLKM

Symbol	Parameters	Test Cond	Min		Max	Unit
V_{OL}	Low level output voltage	Iout = 4 mA			.15*DV_{DD}	V
V_{OH}	High level output voltage	Iout = 4 mA	.85*DV_{DD}			V
C_{load}	Load capacitance				30	pF
Dcycle	Duty cycle		45		55	%

FUNCTIONAL DECRIPTION

The MTC20454 performs the analog portions of four ATU-C modems.

It has filters (with a programmable cut-off frequency) that use automatic continuous time tuning to avoid time varying phase characteristics which can be of dramatic consequence for DMT modems. It requires few external components, uses a 3.3 V supply and is packaged in a 100 pins TQFP in order to reduce PCB area.

The following descriptions apply to each of the four analog front ends in the chip:

The Receiver (RX)

The DMT signal coming from the lines to the MTCMTC20454MTC2045420454 is first filtered by the two following external filters:

- POTS HP filter: Attenuation of speech and POTS signalling.
- Channel filter: Attenuation of echo signal to improve RX dynamic.

The signal is amplified by a low noise gain stage (-15..+31 dB) then lowpass filtered to avoid anti-aliasing and to ease further digital processing by removing unwanted high frequency out-of-band noise. A 12 bits A/D converter samples the data at 8.832 MS/s, transforms the signal into a igital representation and sends it to the DMT signal processor via the multiplexed digital interface.

The Transmitter (TX/TXE)

The 12 bits data at 8.832 Ms coming from the DMT signal processor through the multiplexed digital interface are transformed by a D/A converter into an analog signal. This signal is then filtered to decrease DMT sidelobes levels and meet the ANSI transmitter spectral response but also to reduce he out-of-band noise (which can be echoed to the RX path) to an acceptable level. The pre-driver buffers The signal for the external line driver and case of short loops provide attenuation provision

The Digital Interface

The digital part of the MTC20454 can be divided into two parts:

- The data interface converts the multiplexed data from/to the DMT signal processor into a valid representation for the TX DAC and RX ADC for the requested line.
- The control interface allows the board processor to configure the MTC20454 paths (RX/TX gains, filter band, ...) or settings.

ANALOG TX/RX SIGNALS

The reference impedance for all power calculations is 100 Ohm.

DMT Signal

A DMT signal is basically the sum of N independently QAM modulated signals, each carried over a distinct carrier. The frequency separation of each carrier is 4.3125 KHz with a total number of 256 carriers (ANSI).

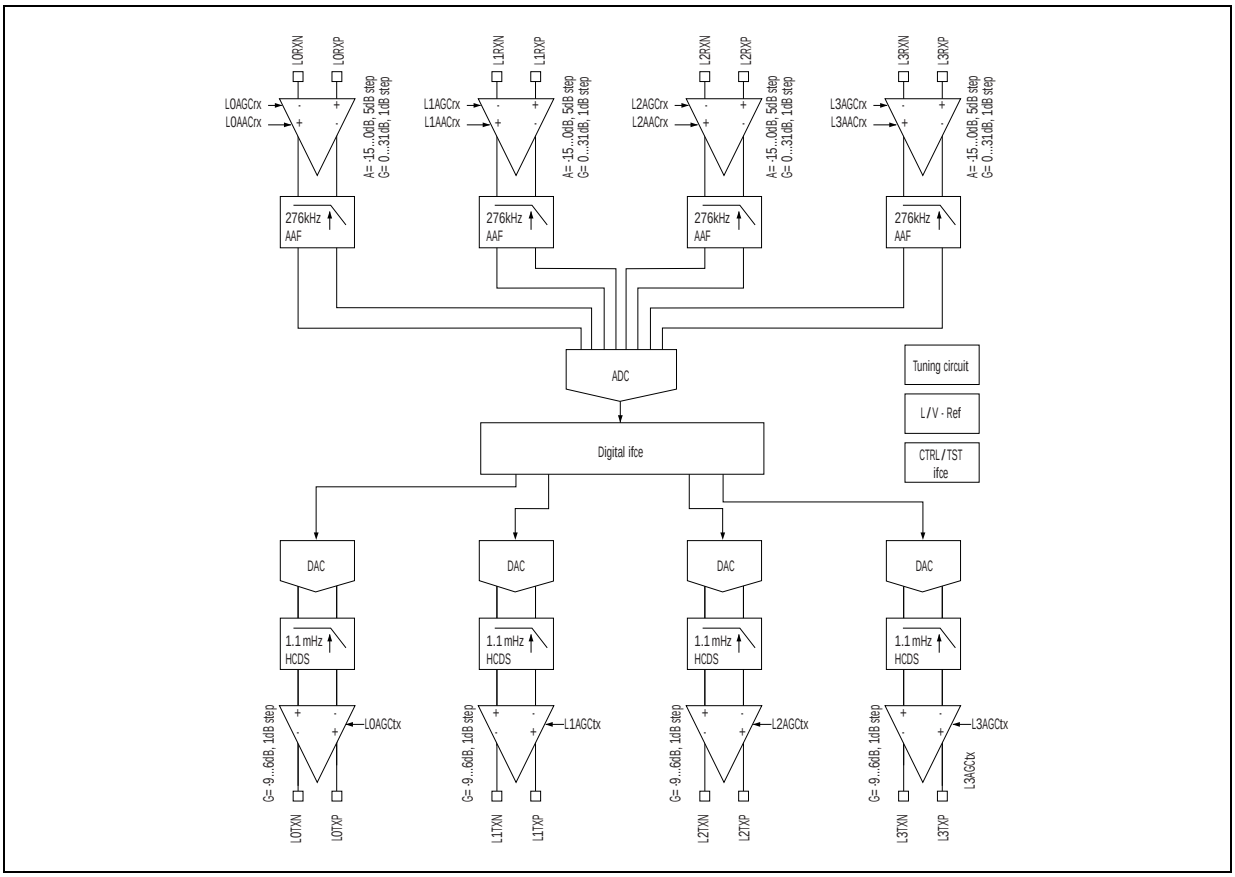
For a large N, the signal can be modelled by a gaussian process with a certain amplitude probability density function. Since the maximum amplitude is expected to arise very rarely, the signal is clipped to trade-off the resulting SNR loss against AD/DA dynamic range.

A clipping factor (Vpeak/Vrms = “crest factor”) of 5 is used resulting in a maximum SNR of 75 dB. ADSL DMT signals are nominally sent at -40 dBm/Hz +/- 3 dB (-3.65 dBm/carrier) with a maximal power of 100 mW for downlink transmitter and 4.5 mW for uplink transmitter. The minimum SNR+D needed for DMT carrier demodulation is about (3*N+20) dB with a minimum of 38 dB where N is the constellation size of a carrier (in bits).

Block Diagram

The transformer has a 1:2 ratio. The termination resistors are 12.5 Ohm in case of 100 Ohm lines. The hybrid bridge resistors should be < 2.5 kOhm for low-noise. An HP filter must be used on the TX path to reduce DMT sidelobes and out-of- band noise influence on the receiver. On the RX path, a LP filter must be used in order to reduce the echo signal level and to avoid saturation of the input stage of the receiver. The POTS filter is used in both directions to reduce cross talk between ADSL signals and POTS speech and signalling.

Figure 4. AFE Block Diagram (for detailed schematics see MTB20450-EBC reference design.)



MTC20454RX PATH

Speech Filter

An external bi-directional LP filter for up and downstream POTS service splits out the speech signal to the analog telephone. The ADSL analog front end integrated circuit does not contain any circuitry for the POTS service but guarantees that the POTS bandwidth is not disturbed by spurious signals from the ADSL spectrum.

Channel Filters

The purpose of these external analog circuits is to provide partial echo cancellation by analog filtering of the receive. This is feasible because the upstream and the downstream data can be modulated on separate carriers (FDM).

Signal Attenuator (ATT) and Low Noise Amplifier

The attenuator needs to be DC decoupled from the external circuitry.

In fact, it is also used to internally fix the LNA input common mode voltage at the nominal value: AVDD/2. This is done by the use of an internal biasing circuit. It is therefore mandatory to de-couple the MTC20454 input from any external DC biasing system. The Low Noise Amplifier (LNA) placed after the ATT will be used in combination with the attenuation block.

The goal is to obtain a range of RX path input level varying from –15 dB to 31 dB, while maintaining the noise contribution negligible.

RX Filters

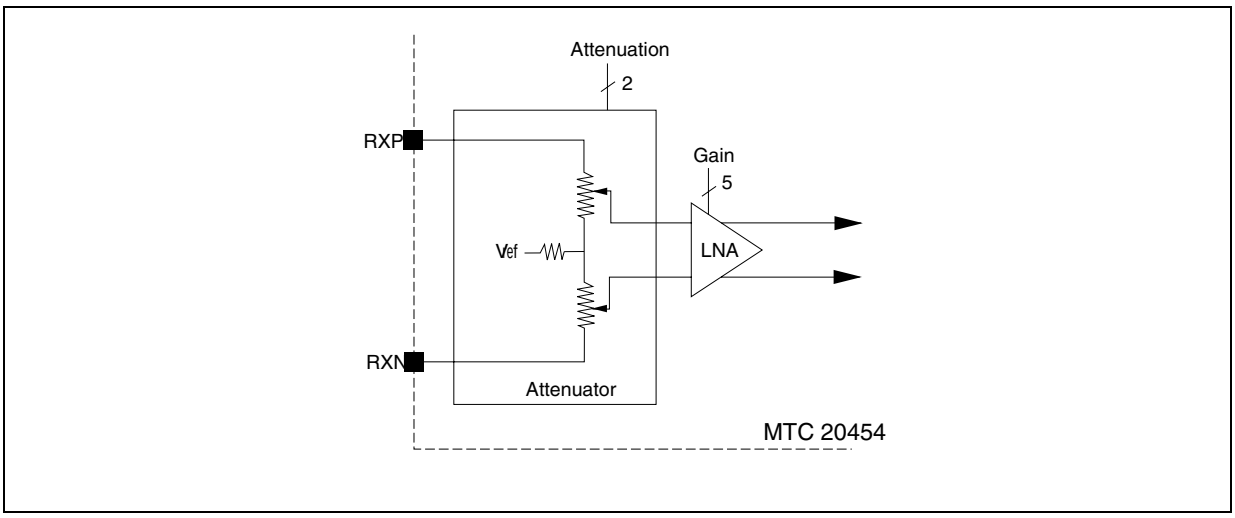
The combination of the external filter (an LC ladder filter typically) with the integrated low pass filter provides:

- echo reduction to improve dynamic Range - DMT sidelobe and out of band (anti-aliasing) attenuation.
- Anti alias filter (60 dB rejection @ image freq.)

Linearity of RX

Linearity of the RX analog path is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.5 Vpd amplitude (total _1 Vpd) at the output of the RX-AGC amplifier (i.e: before the ADC) for the case of minimal AGC setting.

Figure 5. Signal Attenuator (ATT) and Low Noise Amplifier



Power Supply Rejection

The noise on the power supplies for the RX-path must be lower than 50 mVrms in-band white noise for any AVDD.

The pre-driver drives an external line power amplifier which transmits the required power to the line.

TX Filter

The TX filters act not only to suppress the DMT sidebands but also as smoothing filters on the D/A converter's output to suppress the image spectrum. For this reason they are realised in a time continuous approach.

ATU-C-TX Filter

Same filter as ATU-R-RX. Its purpose is now is to remove image frequency of the transmitted signal according the ANSI definition.

Linearity of TX

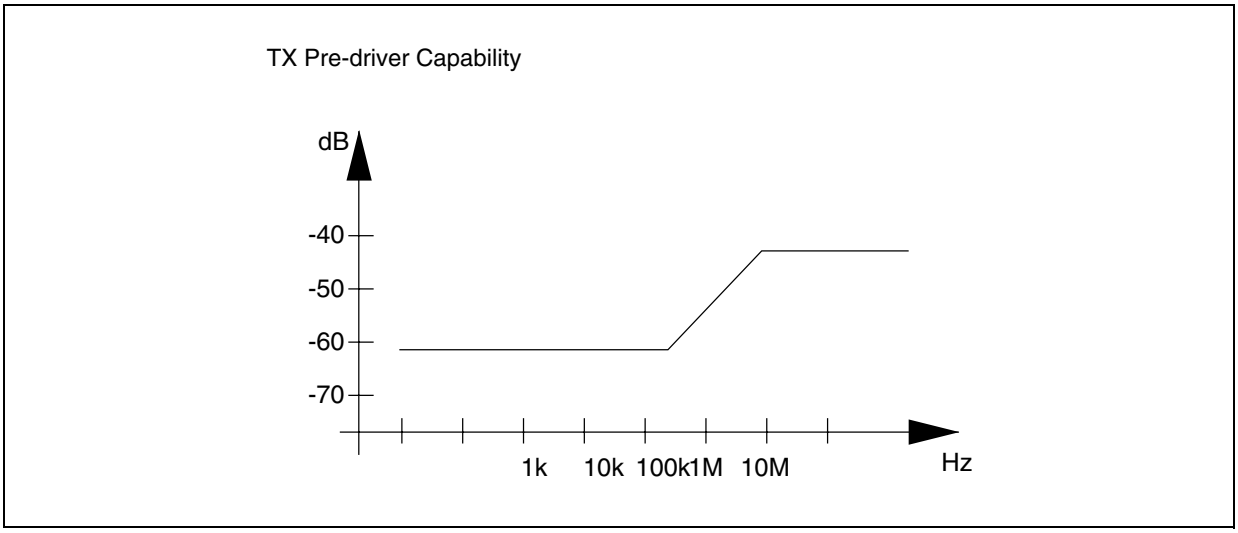
Linearity of the TX is defined by the IM3 product of two sinusoidal signals with frequencies f1 and f2 and each with 0.25 Vpd amplitude (-6 dB FS) at the output of the pre-driver for the case of a total AGC = 0 dB.

Power Supply Rejection

The noise on the power supplies for the TX-path must be lower than the following:

- < 50 mVrms in band white noise for AVDD.
- < 15 mVrms in band white noise for Pre-driver AVDD.

Figure 6. Power Supply Rejection



DIGITAL INTERFACE

Control Interface

The digital code setting for the MTC20454 configuration is sent over a serial line (CTRLIN) using the word clock (CLWD). The data burst is composed of 16 bits from which the first bit is used as start bit ('0'), the three LSBs being used to identify the data contained in the 12 remaining bits. Test related data are latched but they are overruled by the normal settings if the TEST pin is low.

Control Interface Timing

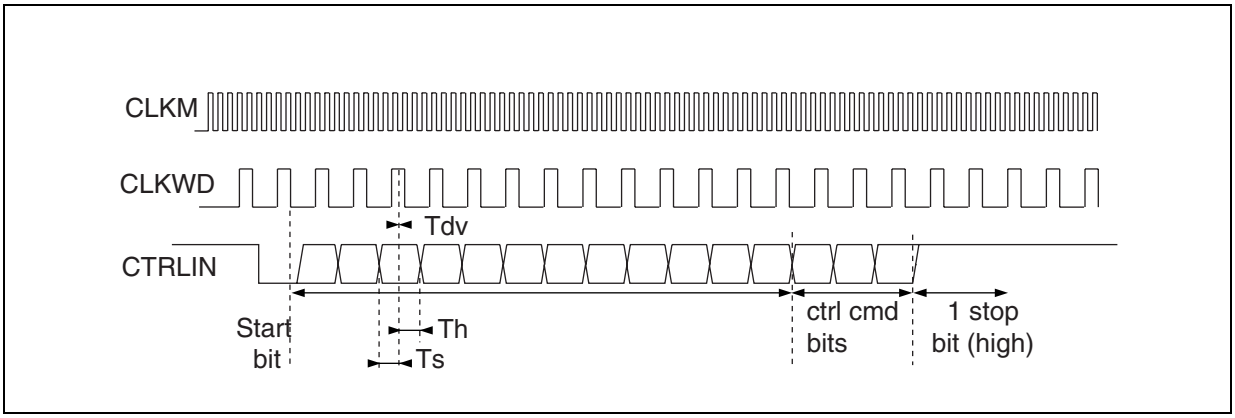
The control interface bits are considered valid on each positive edge of the master clock (CLKM). They will be sampled at this moment. The stop bit will trigger the internal data validation.

The timing requirements are depicted in the following figure and table:

Table 1. Control interface timing requirements

Symbol	Parameter	Min	Typ	Max	Remarks
Ts	Setup time	0.5 ns	-	-	
Th	Hold time	0.2 ns	-	-	
Tdv	Data valid	0.5 ns	-	4 ns	

Figure 7. Control interface chronodiagram



Receive / Transmit Interface

The digital interface is based on a 4 * 8.832 MHz (35.328 MHz) clock. The 8.832MHz 12 bits A/D output signal or the D/A input signal are SIPO multiplexed over 4 parallel 35.328MHz data lines in the following table. If OSR = 2 bit is selected, CLKNIB is used as nibble clock (17.664 MHz, disabled in normal mode), and all the

Table 2. RXi, TXi, CLKWD periods are twice

Packet Number	Bus Line	Word bit
Packet 1	RX0/TX0	Bit 0
	RX1/TX1	Bit 1
	RX2/TX2	Bit 2
	RX3/TX3	Bit 3
Packet 2	RX0/TX0	Bit 4
	RX1/TX1	Bit 5
	RX2/TX2	Bit 6
	RX3/TX3	Bit 7
Packet 3	RX0/TX0	Bit 8
	RX1/TX1	Bit 9
	RX2/TX2	Bit 10
	RX3/TX3	Bit 11
Packet 4	RX0/TX0	Bit 12
	RX1/TX1	Bit 13
	RX2/TX2	Bit 14
	RX3/TX3	Bit 15

TX / TXE Signal Dynamic Range

The dynamic range of the signal for both DACs is 12 bits extracted from the available signed 16 bit representation coming from the digital processor.

The maximal positive number is 2 11 -1, the most negative number is -2 11, the 3 least significant bits are ignored.

Any signal exceeding these limits is clamped to the maximal value.

Table 3. TX bit map

Sign	Sign	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	n.u	n.u	n.u

RX Signal Dynamic Range

The dynamic range of the signal from the ADC is limited to 13 bits. hose bits are converted to a signed representation with a maximal positive number of 2 12 -1 and a most negative number of -2 12.

The 2 LSBs are filled with ‘0’.

Table 4. RX bit map in normal mode

Sign	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0

Receive / Transmit Interface Timing

This interface is a triple (RX,TX, TXE) nibble-serial interface running at 8.8 MHz sampling (normal mode).

The data are represented in 16 bits format, and transferred in groups of 4 bits (nibbles). The LSBs are transferred first. The MTC20454 generates a nibble clock (= master clock in normal mode, CLKNIB in OSR = 2 mode) and word signals shared by the three interfaces.

Data is transmitted on the rising edge of the master clock (CLKM/CLKNIB) and sampled on the low going edge of CLKM/CLKNIB. This holds for the data stream from MTC20454 and rom the digital processor. Data,

CLWD set-up and hold times are 5 ns with reference to the falling edge of CLKM/CLKNIB. RXD is sampled with CLKM rising edge.

Figure 8. TX/RX Digital Interface Timing

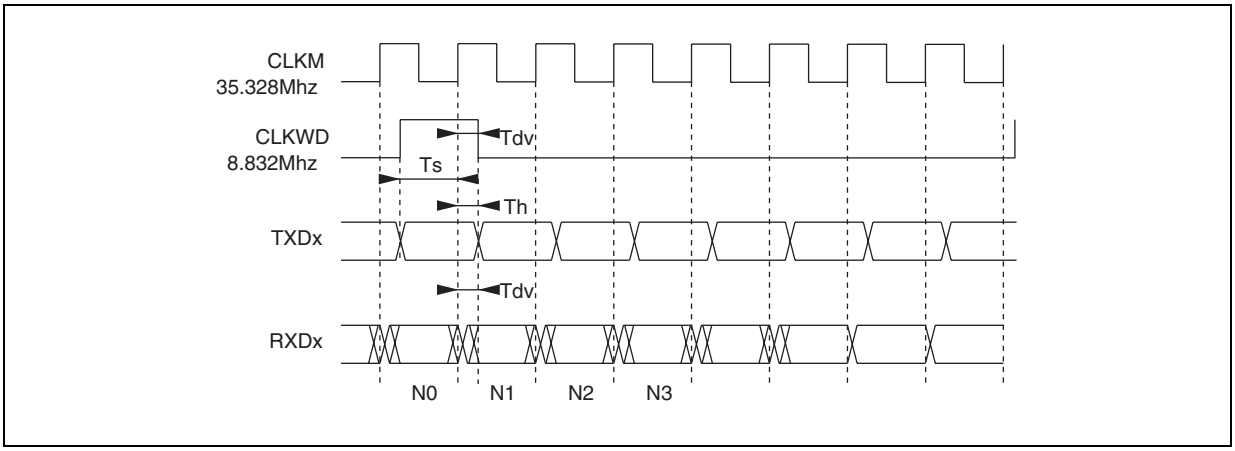


Table 5. TX/RX Digital Interface timing

Symbol	Parameter	Min	Typ	Max
Ts	Setup time	0.5 ns	-	-
Th	Hold time	0.2 ns	-	-
Tdv	Data valid	0.5 ns	-	4 ns

Reset Function

The MTC20454 is placed in reset mode when the RESETN pin is pulled to ground (active low signal). The chip status is depicted in the following table:

Reset
CLKM pin is replicating the CLKIN input clock. System clock available
CLKWD is not generated. The pin stays at high level
Digital blocks are in reset: no activity
Analog blocks are in powerdown
External driver is forced to powerdown

Test

Four different test modes are implemented. The functional test mode allows separate access to different analog parts of the circuit in order to check some characteristics. Various test configurations are available via the CTRLIN interface.

The digital core scan and the I/O nand tree test modes are dedicated for the detection of hardware process flaws in digital elements and IOs.

The last test mode allows to put the outputs in the tristate mode in order to be able to perform the ESD qualification tests.

Test is enabled with a high level n the TEST pin. The actual value of TX1 and TX0 bits on the rising edge of the TEST pin will set the test mode.

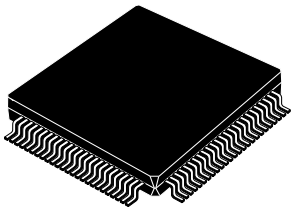
The available test modes and their corresponding signal values are summarized in the following table:

Table 6. Tests mode accessMTC20454

TX1	TX0	Test Mode
0	0	functional test (enable various tests accesses via CTRLIN interface
0	1	digital scan chain test
1	0	I/O nand tree
1	1	Tristate output for ESD

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.020	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc		0.080			0.003	

OUTLINE AND MECHANICAL DATA



TQFP100
(14x14x1.40mm)