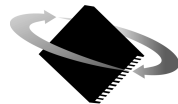


Navigator™ Motion Processor

MC2300 Series Technical Specifications *for Brushless Servo Motion Control*



P M D

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Related Documents

Navigator Motion Processor User's Guide (MC2000UG)

How to set up and use all members of the Navigator Motion Processor family.

Navigator Motion Processor Programmer's Reference (MC2000PR)

Descriptions of all Navigator Motion Processor commands, with coding syntax and examples, listed alphabetically for quick reference.

Navigator Motion Processor Technical Specifications

Four booklets containing physical and electrical characteristics, timing diagrams, pinouts, and pin descriptions of each series:

- MC2100 series, for brushed servo motion control (MC2100TS);

- MC2300 series, for brushless servo motion control (MC2300TS);

- MC2400 series, for microstepping motion control (MC2400TS);

- MC2500 series, for stepping motion control (MC2500TS);

- MC2800 Series, for brushed servo and brushless servo motion control (MC2800TS).

Navigator Motion Processor Developer's Kit Manual (DK2000M)

How to install and configure the DK2000 developer's kit PC board.

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1 The Navigator Family

| | MC2100 Series | MC2300 Series | MC2400 Series | MC2500 Series | MC2800 Series |
|-----------------------------|---|---|---|---|---|
| # of axes | 4, 2, or 1 | 4, 2 or 1 | 4, 2 or 1 | 4, 2, or 1 | 4 or 2 |
| Motor type supported | Brushed servo | Brushless servo | Stepping | Stepping | Brushed servo + brushless servo |
| Output format | Brushed servo (single phase) | Commutated (6-step or sinusoidal) | Microstepping | Pulse and direction | Brushed servo (single phase) + commutated (6-step sinusoidal) |
| Incremental encoder input | ✓ | ✓ | ✓ | ✓ | ✓ |
| Parallel word device input | ✓ | ✓ | ✓ | ✓ | ✓ |
| Parallel communication | ✓ | ✓ | ✓ | ✓ | ✓ |
| Serial communication | ✓ | ✓ | ✓ | ✓ | ✓ |
| Diagnostic port | ✓ | ✓ | ✓ | ✓ | ✓ |
| S-curve profiling | ✓ | ✓ | ✓ | ✓ | ✓ |
| Electronic gearing | ✓ | ✓ | ✓ | ✓ | ✓ |
| On-the-fly changes | ✓ | ✓ | ✓ | ✓ | ✓ |
| Directional limit switches | ✓ | ✓ | ✓ | ✓ | ✓ |
| Programmable bit output | ✓ | ✓ | ✓ | ✓ | ✓ |
| Software-invertable signals | ✓ | ✓ | ✓ | ✓ | ✓ |
| PID servo control | ✓ | ✓ | - | - | ✓ |
| Feedforward (accel & vel) | ✓ | ✓ | - | - | ✓ |
| Derivative sampling time | ✓ | ✓ | - | - | ✓ |
| Data trace/diagnostics | ✓ | ✓ | ✓ | ✓ | ✓ |
| PWM output | ✓ | ✓ | ✓ | - | ✓ |
| Motion error detection | ✓ | ✓ | ✓ (with encoder) | ✓ (with encoder) | ✓ |
| Axis settled indicator | ✓ | ✓ | ✓ (with encoder) | ✓ (with encoder) | ✓ |
| DAC-compatible output | ✓ | ✓ | ✓ | - | ✓ |
| Pulse & direction output | - | - | - | ✓ | - |
| Index & Home signals | ✓ | ✓ | ✓ | ✓ | ✓ |
| Position capture | ✓ | ✓ | ✓ | ✓ | ✓ |
| Analog input | ✓ | ✓ | ✓ | ✓ | ✓ |
| User-defined I/O | ✓ | ✓ | ✓ | ✓ | ✓ |
| External RAM support | ✓ | ✓ | ✓ | ✓ | ✓ |
| Multi-chip synchronization | ✓ (21x3) | ✓ (23x3) | ✓ (24x3) | | ✓ (28x3) |
| Chipset part numbers | MC2140 (4 axes) MC2120 (2 axes) MC2110 (1 axis) | MC2340 (4 axes) MC2320 (2 axes) MC2310 (1 axis) | MC2440 (4 axes) MC2420 (2 axes) MC2410 (1 axis) | MC2540 (4 axes) MC2520 (2 axes) MC2510 (1 axis) | MC2840 (4 axes) MC2820 (2 axes) |
| Developer's Kit p/n's: | DK2100 | DK2300 | DK2400 | DK2500 | DK2800 |

Introduction

This manual describes the operational characteristics of the MC2340, MC2320 and MC2310 Motion Processors from PMD. These devices are members of PMD's second-generation motion processor family, which consists of 14 separate products organized into 5 series.

Each of these devices are complete chip-based motion processors. They provide trajectory generation and related motion control functions. Depending on the type of motor controlled they provide servo loop closure, on-board commutation for brushless motors, and high speed pulse and direction outputs. Together these products provide a software-compatible family of dedicated motion processors that can handle a large variety of system configurations.

Each of these chips utilize a similar architecture, consisting of a high-speed computation unit, along with an ASIC (Application Specific Integrated Circuit). The computation unit contains special on-board hardware that makes it well suited for the task of motion control.

Along with similar hardware architecture these chips also share most software commands, so that software written for one chipset may be re-used with another, even though the type of motor may be different.

Each chipset consists of two PQFP (Plastic Quad Flat Pack) ICs: a 100-pin Input/Output (I/O) chip, and a 132-pin Command Processor (CP) chip.

The four different series in the Navigator family are designed for a particular type of motor or control scheme. Here is a summary description of each series.

Family Summary

MC2100 Series (MC2140, MC2120, MC2110) – This series outputs motor commands in either Sign/Magnitude PWM or DAC-compatible format for use with brushed servo motors, or with brushless servo motors having external commutation.

MC2300 Series (MC2340, MC2320, MC2310) – This series outputs sinusoidally commutated motor signals appropriate for driving brushless motors. Depending on the motor type, the output is a two-phase or three-phase signal in either PWM or DAC-compatible format.

MC2400 Series (MC2440, MC2420, MC2410) – This series provides microstepping signals for stepping motors. Two phased signals per axis are generated in either PWM or DAC-compatible format.

MC2500 Series (MC2540, MC2520, MC2510) – These chipsets provide high-speed pulse and direction signals for stepping motor systems.

MC2800 Series (MC2840, MC2820) – This series outputs sinusoidally or 6-step commutated motor signals appropriate for driving brushless servo motors as well as PWM or DAC-compatible outputs for driving brushed servo motors.

2 Functional Characteristics

2.1 Configurations, parameters, and performance

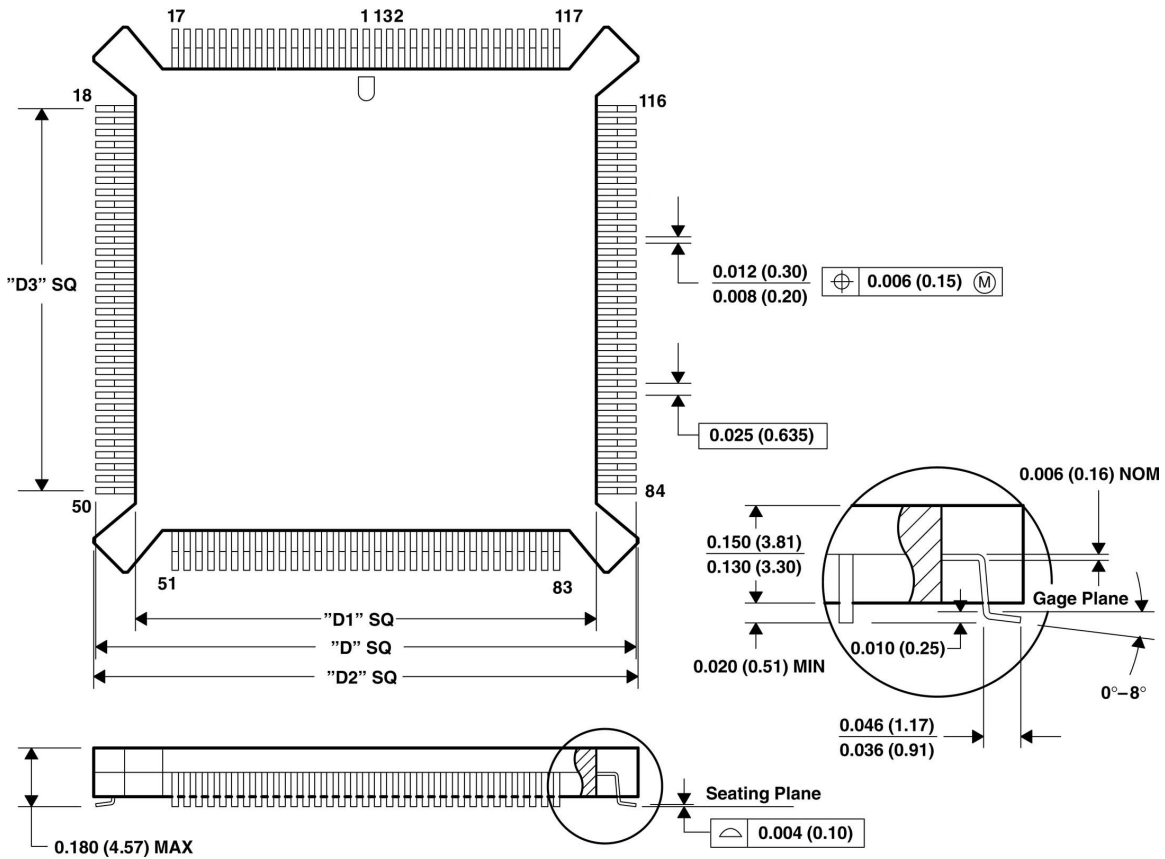
| | |
|---|--|
| Available configurations | 4 axes (MC2340), 2 axes (MC2320), or 1 axis (MC2310) |
| Operating modes | Closed loop (motor command is driven from output of servo filter) Open loop (motor command is driven from user-programmed register) |
| Communication modes | 8/8 parallel (8 bit external parallel bus with 8 bit internal command word size) 8/16 parallel (8 bit external parallel bus with 16 bit internal command word size) 16/16 parallel (16 bit external parallel bus with 16 bit internal command word size) Point to point asynchronous serial Multidrop asynchronous serial |
| Serial port baud rate range | 1,200 baud to 416,667 baud |
| Position range | -2,147,483,648 to +2,147,483,647 counts |
| Velocity range | -32,768 to +32,767 counts/sample with a resolution of 1/65,536 counts/sample |
| Acceleration/deceleration ranges | -32,768 to +32,767 counts/sample ² with a resolution of 1/65,536 counts/sample ² |
| Jerk range | 0 to ½ counts/sample ³ , with a resolution of 1/4,294,967,296 counts/sample ³ |
| Profile modes | S-curve point-to-point (Velocity, acceleration, jerk, and position parameters) Trapezoidal point-to-point (Velocity, acceleration, deceleration, and position parameters) Velocity-contouring (Velocity, acceleration, and deceleration parameters) Electronic Gear (Encoder or trajectory position of one axis used to drive a second axis. Master and slave axes and gear ratio parameters) |
| Electronic gear ratio range | -32,768 to +32,767 with a resolution of 1/65,536 (negative and positive direction) |
| Filter modes | Scalable PID + Velocity feedforward + Acceleration feedforward + Bias. Also includes integration limit, settable derivative sampling time, and output motor command limiting |
| Filter parameter resolution | 16 bits |
| Position error tracking | Motion error window (allows axis to be stopped upon exceeding programmable window) Tracking window (allows flag to be set if axis exceeds a programmable position window) Axis settled (allows flag to be set if axis exceeds a programmable position window for a programmable amount of time after trajectory motion is complete) |
| Motor output modes | PWM (10-bit resolution at 20 kHz) DAC (16 bits) |
| Commutation rate | 20KHz for MC2310 and MC2320, 10KHz for MC2340 |
| Maximum encoder rate | Incremental (up to 5 Mcounts/sec) Parallel-word (up to 160 Mcounts/sec) |
| Parallel encoder word size | 16 bits |
| Parallel encoder read rate | 20 kHz (reads all axes every 50 μsec) |
| Hall sensor inputs | 3 Hall effect inputs per axis (TTL level signals) |
| Servo loop timing range | 153.6 μsec to 32.767 milliseconds |

| | |
|---|--|
| Minimum servo loop time | 153.6 μ sec per enabled axis |
| Multi-chip synchronization | <10 μ sec difference between master and slave servo cycle MC23x3 chipset only |
| Limit switches | 2 per axis: one for each direction of travel |
| Position-capture triggers | 2 per axis: index and home signals |
| Other digital signals (per axis) | 1 AxisIn signal per axis, 1 AxisOut signal per axis |
| Software-invertable signals | Encoder A, Encoder B, Index, Home, AxisIn, AxisOut, PositiveLimit, NegativeLimit, HallA, HallB, HallC (all individually programmable per axis) |
| Analog input | 8 10-bit analog inputs |
| User defined discrete I/O | 256 16-bit wide user defined I/O |
| RAM/external memory support | 65,536 blocks of 32,768 16 bit words per block. Total accessible memory is 2,147,483,648 16 bit words |
| Trace modes | one-time continuous |
| Max. number of trace variables | 4 |
| Number of traceable variables | 27 |
| Number of host instructions | 152 |

2.2 Physical characteristics and mounting dimensions

2.2.1 CP chip

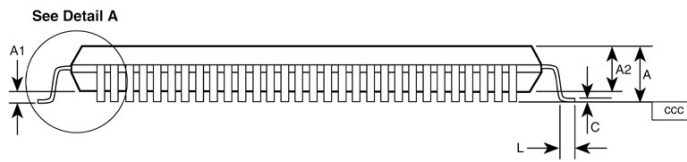
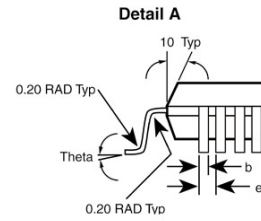
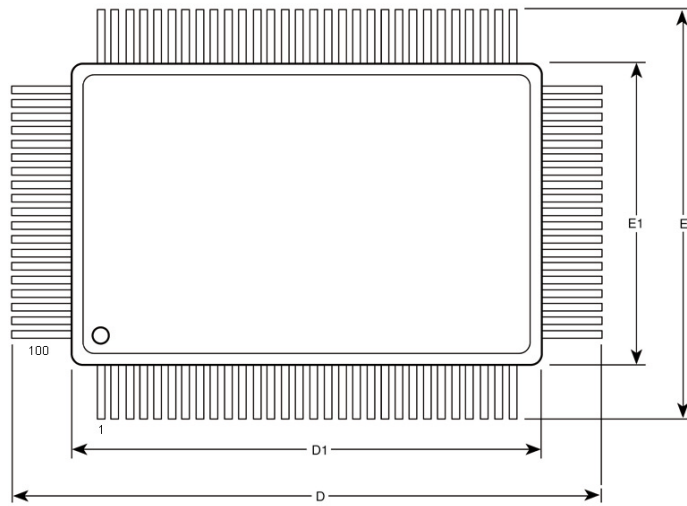
All dimensions are in inches (with millimeters in brackets).



| Dimension | Minimum (inches) | Maximum (inches) |
|-----------|------------------|------------------|
| D | 1.070 | 1.090 |
| D1 | 0.934 | 0.966 |
| D2 | 1.088 | 1.112 |
| D3 | 0.800 nominal | |

2.2.2 I/O chip

All dimensions are in millimeters.



| Dimension | Minimum (mm) | Nominal (mm) | Maximum (mm) |
|-----------|--------------|--------------|--------------|
| A | | | 3.40 |
| A1 | 0.25 | 0.33 | |
| A2 | 2.55 | 2.80 | 3.05 |
| b | 0.22 | | 0.38 |
| c | 0.13 | | 0.23 |
| D | 22.95 | 23.20 | 23.45 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 16.95 | 17.20 | 17.45 |
| E1 | 13.90 | 14.00 | 14.01 |
| e | | 0.65 BSC | |
| L | 0.73 | 0.88 | 1.03 |
| ccc | | | 0.10 |
| theta | 0° | | 7° |

2.3 Environmental and electrical ratings

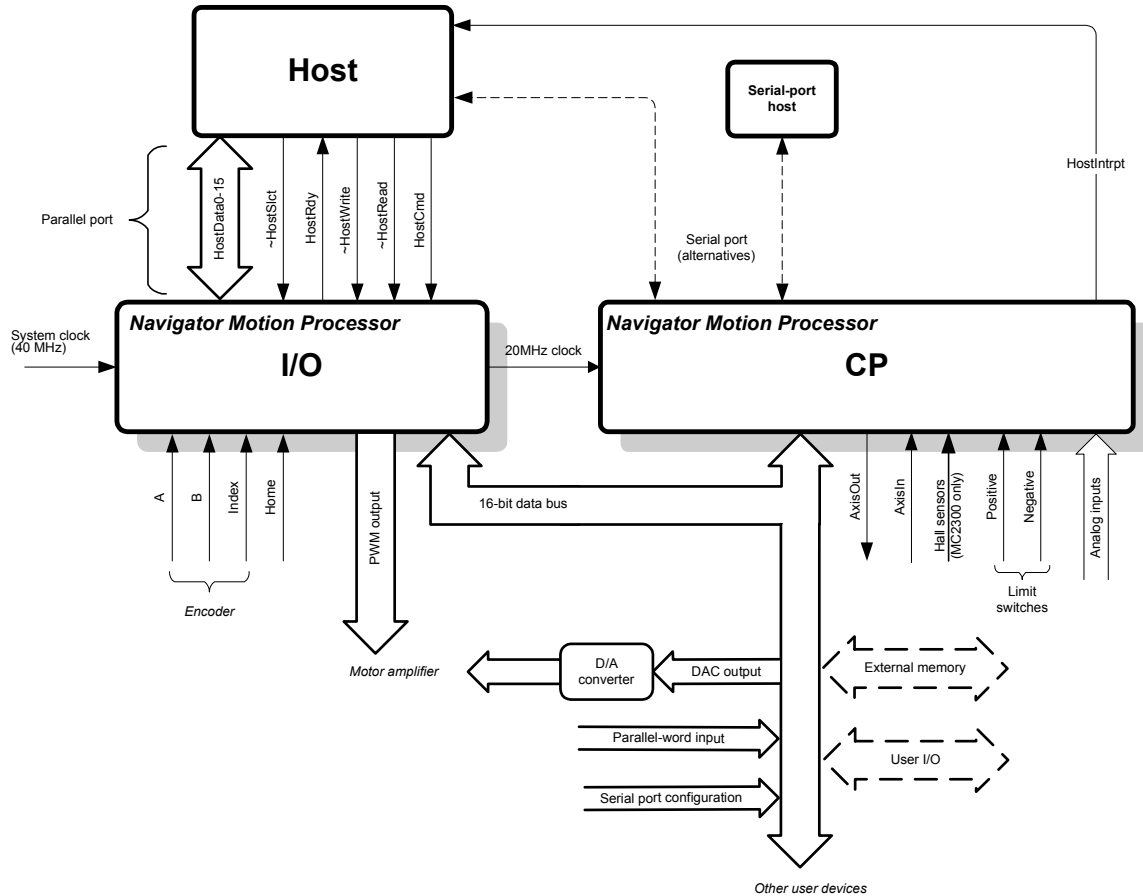
All ratings and ranges are for both the I/O and CP chips.

| | |
|---|------------------------------|
| Storage Temperature (T_s) | -55 °C to 150 °C |
| Operating Temperature (T_a) | 0 °C to 70 °C* |
| Power Dissipation (P_d) | 600 mW (I/O and CP combined) |
| Nominal Clock Frequency (F_{clk}) | 40.0 MHz |
| Supply Voltage limits (V_{cc}) | -0.3V to +7.0V |
| Supply Voltage operating range (V_{cc}) | 4.75V to 5.25V |

* An industrial version with an operating range of -40°C to 85°C is also available. Please contact PMD for more information.

2.4 System configuration

The following figure shows the principal control and data paths in an MC2300 system.



The CP chip contains the profile generator, which calculates velocity, acceleration, and position values for a trajectory; and the digital servo filter, which stabilizes the motor output signal. The filter produces one of two types of output:

- a Pulse-Width Modulated (PWM) signal output which passes via the data bus to the I/O chip, where the output signal generator sends it to the motor amplifiers; or

- a DAC-compatible value routed via the data bus to the appropriate D/A converter.

Axis position information returns to the motion processor through the I/O chip, in the form of encoder feedback, or through the CP chip, in the form of parallel-word feedback.

2.5 Peripheral device address mapping

Device addresses on the CP chip's data bus are memory-mapped to the following locations:

| Address | Device | Description |
|---------|-----------------------|--|
| 0200h | Serial port data | Contains the configuration data (transmission rate, parity, stop bits, etc) for the asynchronous serial port |
| 0800h | Parallel-word encoder | Base address for parallel-word feedback devices |
| 1000h | User-defined | Base address for user-defined I/O devices |
| 2000h | RAM page pointer | Page pointer to external memory |
| 4000h | Motor-output DACs | Base address for motor-output D/A converters |
| 8000h | I/O chip | Base address for I/O chip communications |

3 Electrical Characteristics

3.1 DC characteristics

(V_{cc} and T_a per operating ratings, $F_{clk} = 40.0$ MHz)

| Symbol | Parameter | Minimum | Maximum | Conditions |
|----------|----------------|---------|---------|--------------|
| V_{cc} | Supply Voltage | 4.75 V | 5.25 V | |
| I_{dd} | Supply Current | | 120 mA | open outputs |

Input Voltages

| | | | | |
|---------------|---------------------------------------|--------|------------------|--|
| V_{ih} | Logic 1 input voltage | 2.0 V | $V_{cc} + 0.3$ V | |
| V_{il} | Logic 0 input voltage | -0.3 V | 0.8 V | |
| $V_{ihreset}$ | Logic 1 voltage for reset pin (reset) | 2.2 V | $V_{cc} + 0.3$ V | |

Output Voltages

| | | | | |
|----------|------------------------|-------|--------|--|
| V_{oh} | Logic 1 Output Voltage | 2.4 V | | @CP $I_o = -23$ mA @I/O $I_o = -6$ mA |
| V_{ol} | Logic 0 Output Voltage | | 0.33 V | @CP $I_o = 6$ mA @I/O $I_o = 6$ mA |

Other

| | | | | |
|-----------|----------------------------------|----------------------------|---------------------------|-----------------------------------|
| I_{out} | Tri-State output leakage current | -5 μ A | 5 μ A | @CP $0 < V_{out} < V_{cc}$ |
| I_{in} | Input current | -10 μ A -10 μ A | 10 μ A -10 μ A | @CP @I/O $0 < V_i < V_{cc}$ |
| C_{io} | Input/Output capacitance | 15 pF | 10 pF | @CP typical @I/O |

Analog Input

| | | | | |
|-----------|--|----|-------------|--|
| Z_{ai} | Analog input source impedance | | 9k Ω | |
| E_{dnl} | Differential nonlinearity error. Difference between the step width and the ideal value. | -1 | 1.5 LSB | |
| E_{inl} | Integral nonlinearity error. Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error. | | +/-1.5 LSB | |

3.2 AC characteristics

See timing diagrams, Section 4, for T_n numbers. The symbol “~” indicates active low signal.

| Timing Interval | T_n | Minimum | Maximum |
|--------------------------------|-------|----------|--------------------------|
| Clock Frequency (F_{clk}) | | > 0 MHz | 40 MHz (<i>note 1</i>) |
| Clock Pulse Width | T1 | 10 nsec | |
| Clock Period (<i>note 3</i>) | T2 | 25 nsec | |
| Encoder Pulse Width | T3 | 150 nsec | |
| Dwell Time Per State | T4 | 75 nsec | |

| Timing Interval | T _n | Minimum | Maximum |
|--|----------------|---------------|----------|
| Index Setup and Hold (relative to Quad A and Quad B low) | T5 | 0 nsec | |
| ~HostSlct Hold Time | T6 | 0 nsec | |
| ~HostSlct Setup Time | T7 | 0 nsec | |
| HostCmd Setup Time | T8 | 0 nsec | |
| HostCmd Hold Time | T9 | 0 nsec | |
| Read Data Access Time | T10 | | 25 nsec |
| Read Data Hold Time | T11 | | 10 nsec |
| ~HostRead High to HI-Z Time | T12 | | 20 nsec |
| HostRdy Delay Time | T13 | 100 nsec | 150 nsec |
| ~HostWrite Pulse Width | T14 | 70 nsec | |
| Write Data Delay Time | T15 | | 35 nsec |
| Write Data Hold Time | T16 | 0 nsec | |
| Read Recovery Time (<i>note 2</i>) | T17 | 60 nsec | |
| Write Recovery Time (<i>note 2</i>) | T18 | 60 nsec | |
| Read Pulse Width | T19 | 70 nsec | |
| Address Setup Delay Time | T20 | | 7 nsec |
| Data Access Time | T21 | | 19 nsec |
| Data Hold Time | T22 | | 2 nsec |
| Address Setup Delay Time | T23 | | 7 nsec |
| Address Setup to WriteEnable High | T24 | 72 nsec | |
| RAMSlct Low to WriteEnable High | T25 | | 79 nsec |
| Address Hold Time | T26 | 17 nsec | |
| WriteEnable Pulse Width | T27 | 39 nsec | |
| Data Setup Time | T28 | | 3 nsec |
| Data Setup before Write High Time | T29 | | 42 nsec |
| Address Setup Delay Time | T30 | | 7 nsec |
| Data Access Time | T31 | | 71 nsec |
| Data Hold Time | T32 | | 2 nsec |
| Address Setup Delay Time | T33 | | 7 nsec |
| Address Setup to WriteEnable High | T34 | 122 nsec | |
| PeriphSlct Low to WriteEnable High | T35 | | 129 nsec |
| Address Hold Time | T36 | 17 nsec | |
| WriteEnable Pulse Width | T37 | 89 nsec | |
| Data Setup Time | T38 | | 3 nsec |
| Data Setup before Write High Time | T39 | | 92 nsec |
| Read to Write Delay Time | T40 | 50 nsec | |
| Reset Low Pulse Width | T50 | 5.0 μ sec | |
| RAMSlct Low to Strobe Low | T51 | | 1 nsec |
| Strobe High to RAMSlct High | T52 | | 4 nsec |
| WriteEnable Low to Strobe Low | T53 | | 1 nsec |
| Strobe High to WriteEnable High | T54 | | 3 nsec |
| PeriphSlct Low to Strobe Low | T55 | | 1 nsec |
| Strobe High to PeriphSlct High | T56 | | 4 nsec |
| Device Ready/ Outputs Enabled | T57 | | 1 msec |

Note 1 Performance figures and timing information valid at $F_{clk} = 40.0$ MHz only. For timing information and performance parameters at $F_{clk} < 40.0$ MHz see section 6.1.

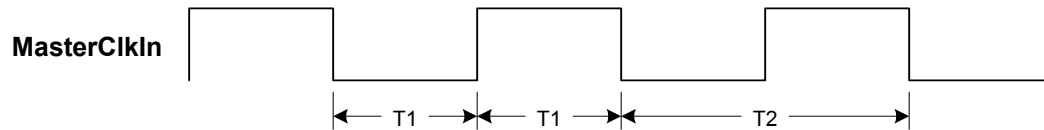
Note 2 For 8/8 and 8/16 interface modes only.

Note 3 The clock low/high split has an allowable range of 45-55%.

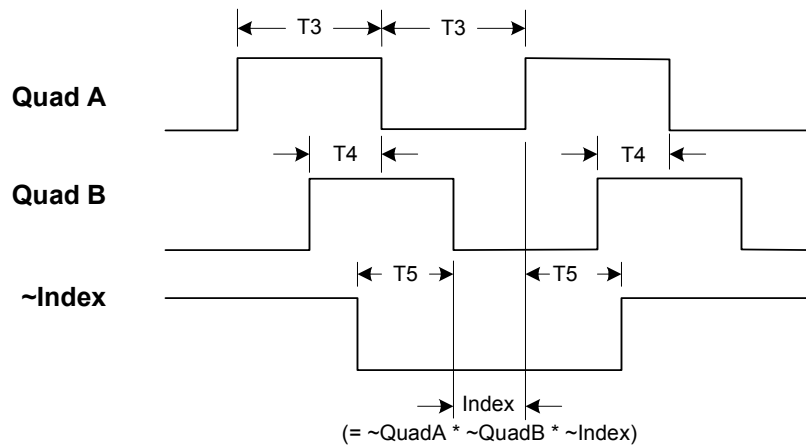
4 I/O Timing Diagrams

For the values of T_n , please refer to the table in Section 3.2.

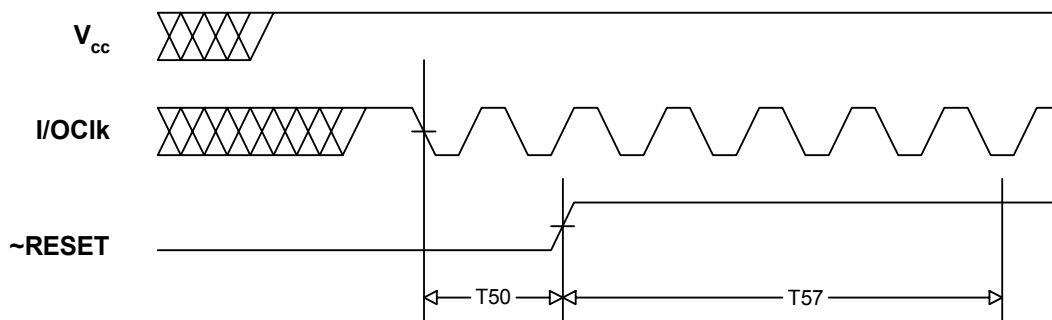
4.1 Clock



4.2 Quadrature encoder input

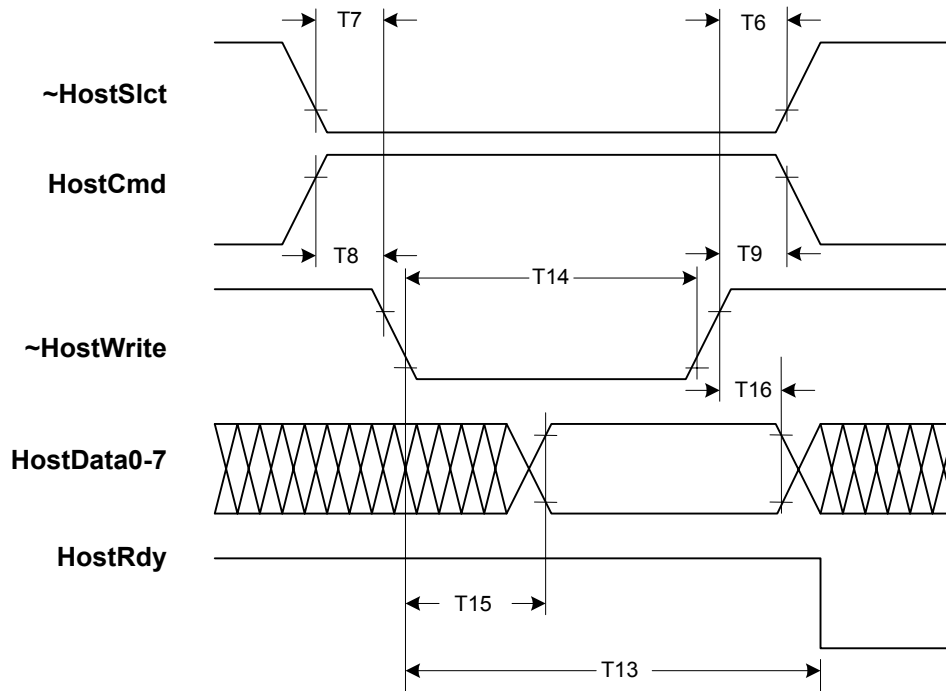


4.3 Reset

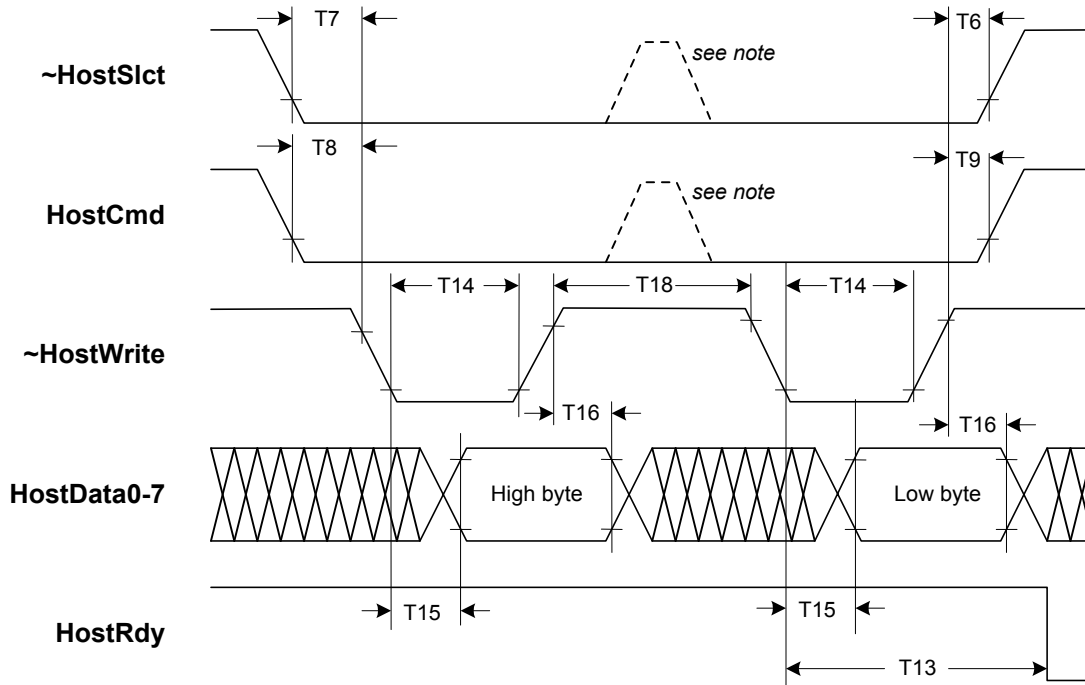


4.4 Host interface, 8/8 mode

4.4.1 Instruction write, 8/8 mode

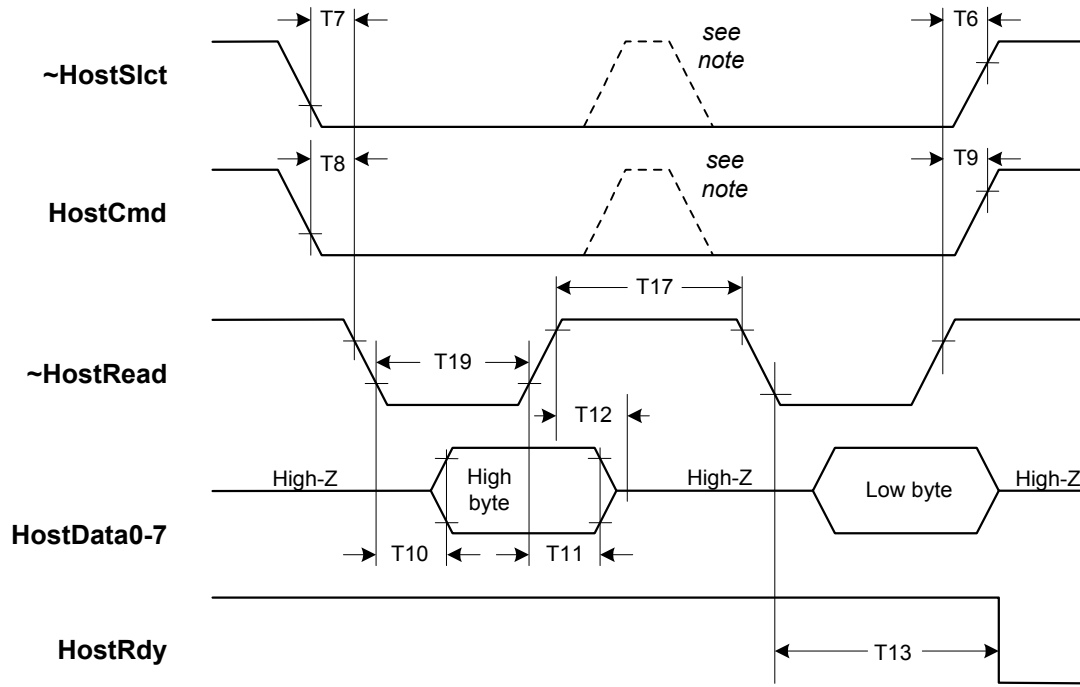


4.4.2 Data write, 8/8 mode



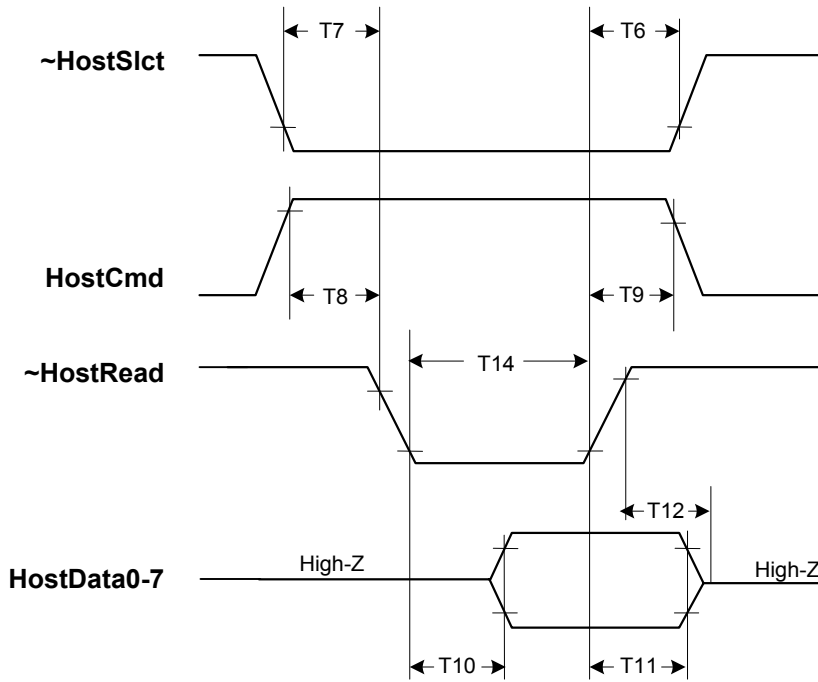
Note: If setup and hold times are met, \sim HostSlct and HostCmd may be de-asserted at this point.

4.4.3 Data read, 8/8 mode



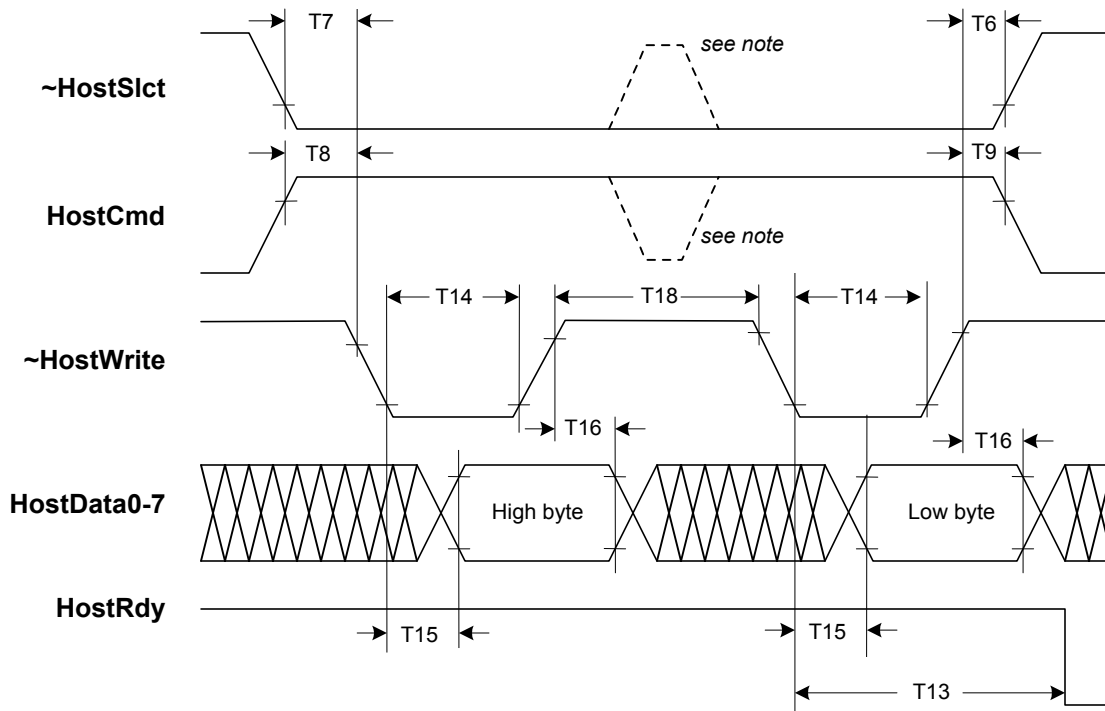
Note: If setup and hold times are met, **~HostSlct** and **HostCmd** may be de-asserted at this point.

4.4.4 Status read, 8/8 mode



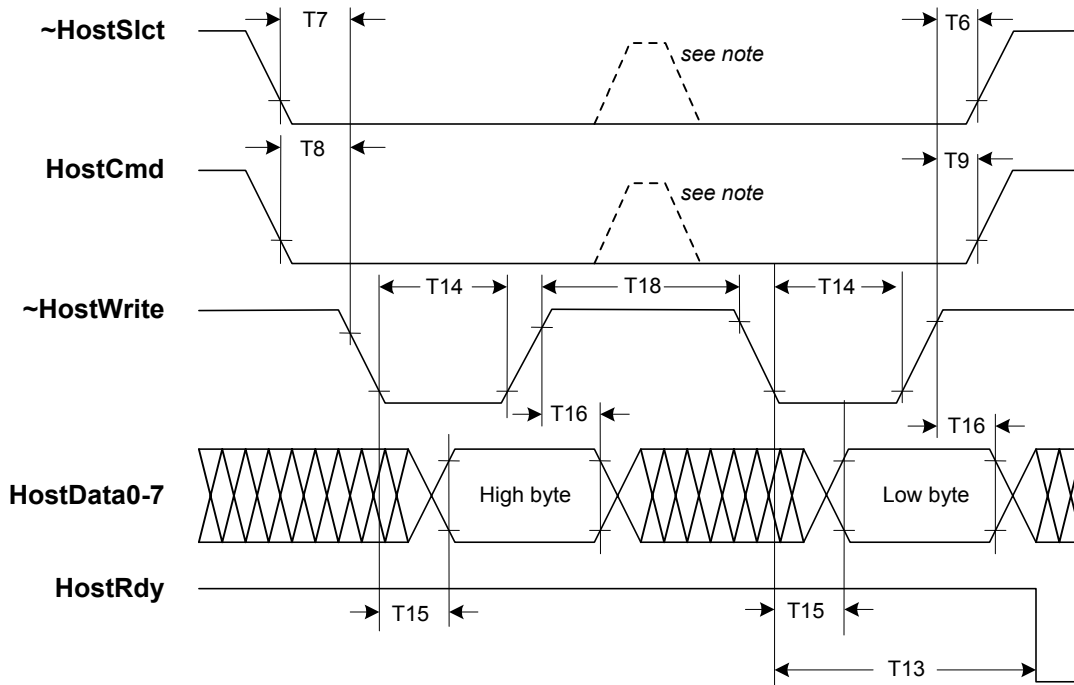
4.5 Host interface, 8/16 mode

4.5.1 Instruction write, 8/16 mode



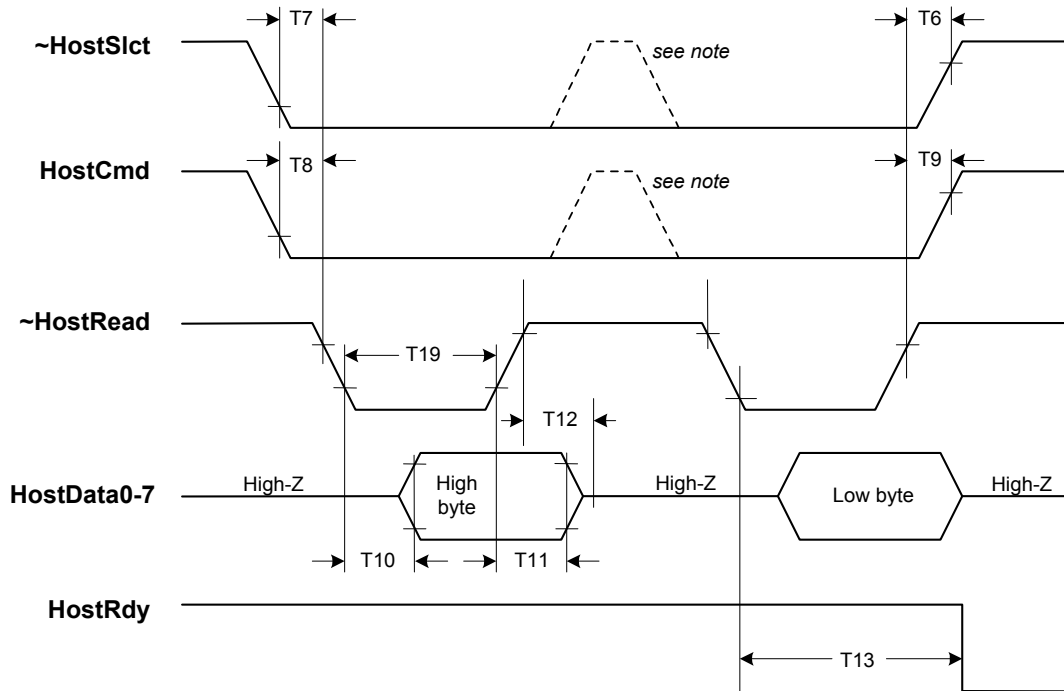
Note: If setup and hold times are met, **~HostSlct** and **HostCmd** may be de-asserted at this point.

4.5.2 Data write, 8/16 mode



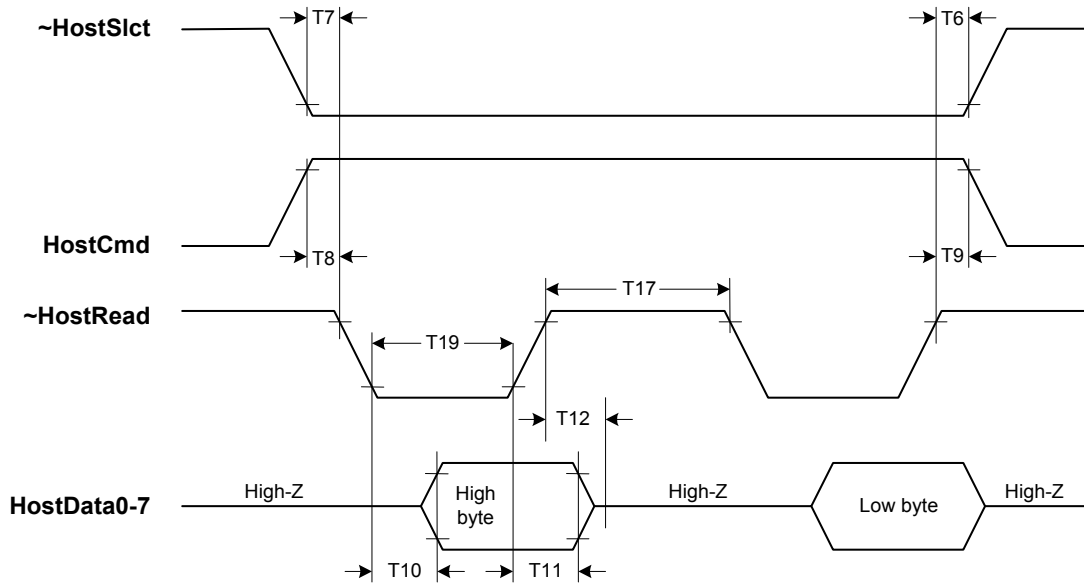
Note: If setup and hold times are met, **~HostSlct** and **HostCmd** may be de-asserted at this point.

4.5.3 Data read, 8/16 mode



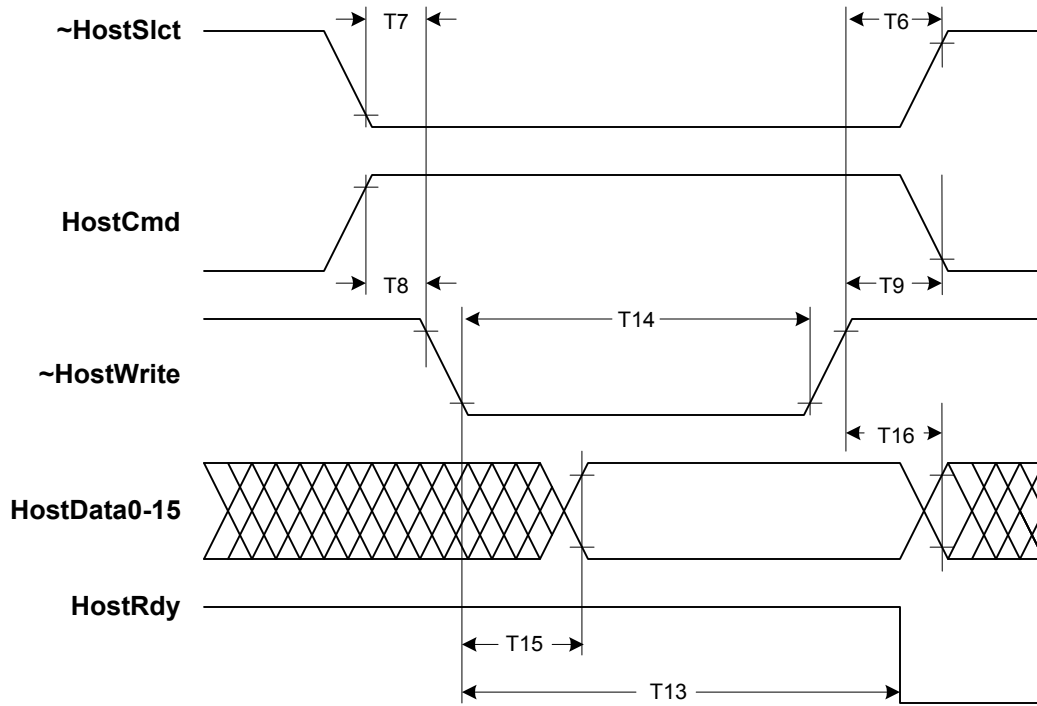
Note: If setup and hold times are met, \sim HostSlct and HostCmd may be de-asserted at this point.

4.5.4 Status read, 8/16 mode

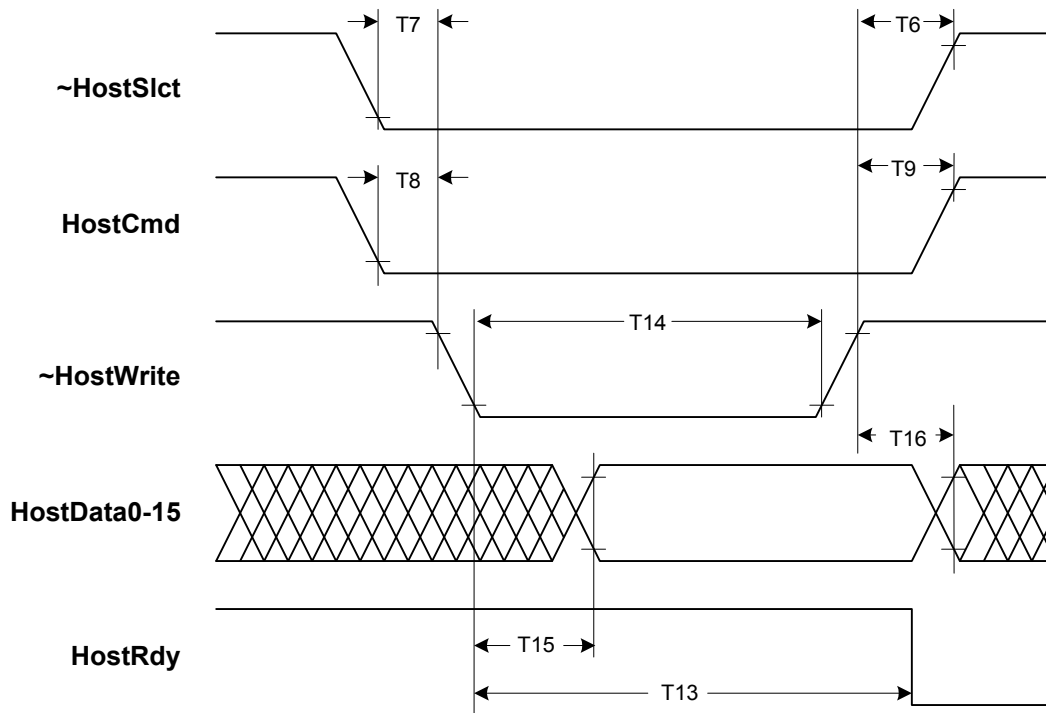


4.6 Host interface, 16/16 mode

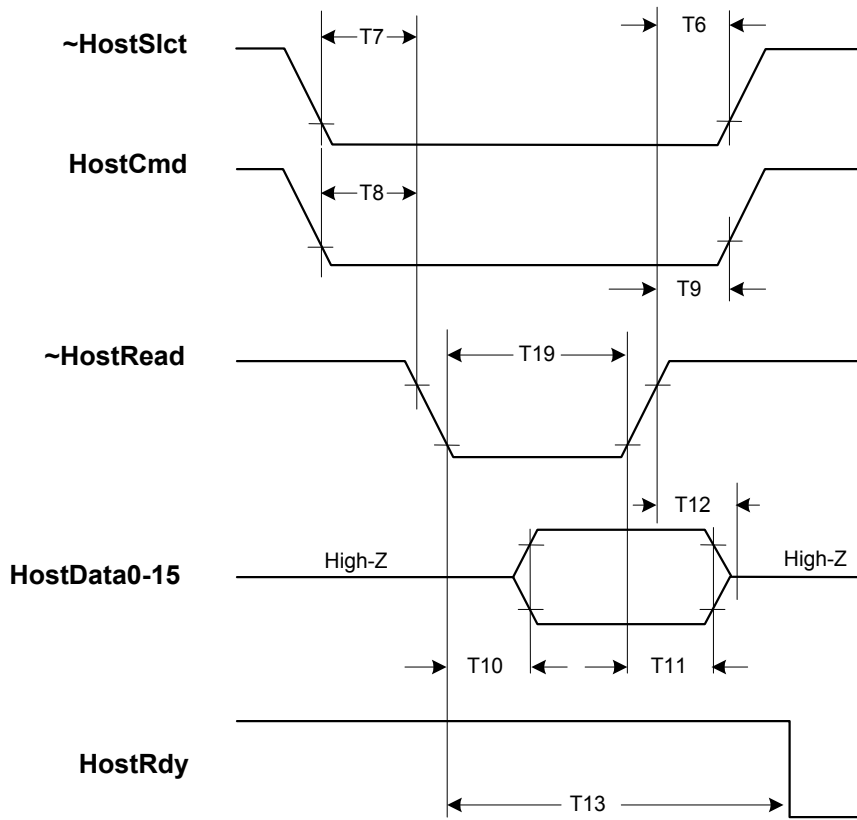
4.6.1 Instruction write, 16/16 mode



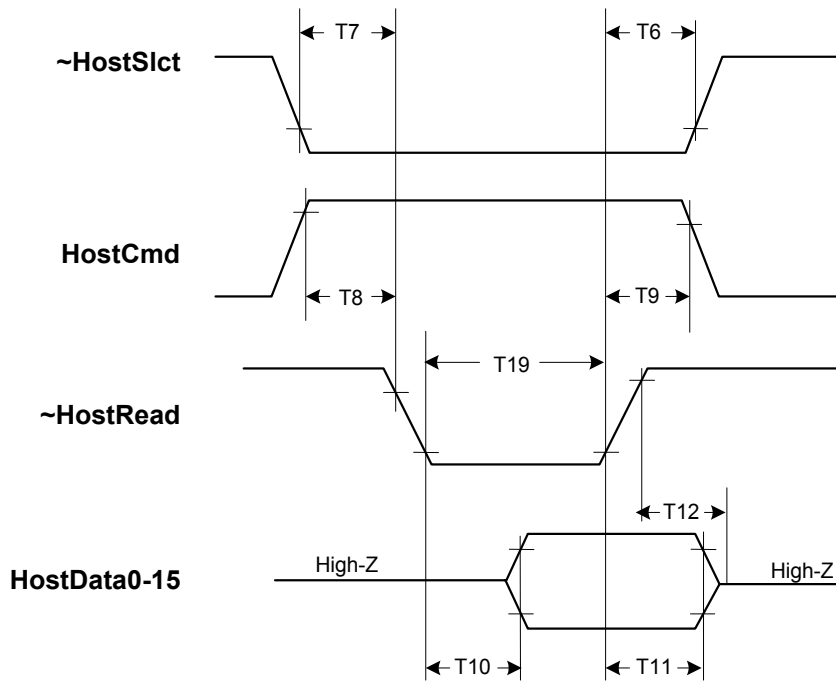
4.6.2 Data write, 16/16 mode



4.6.3 Data read, 16/16 mode



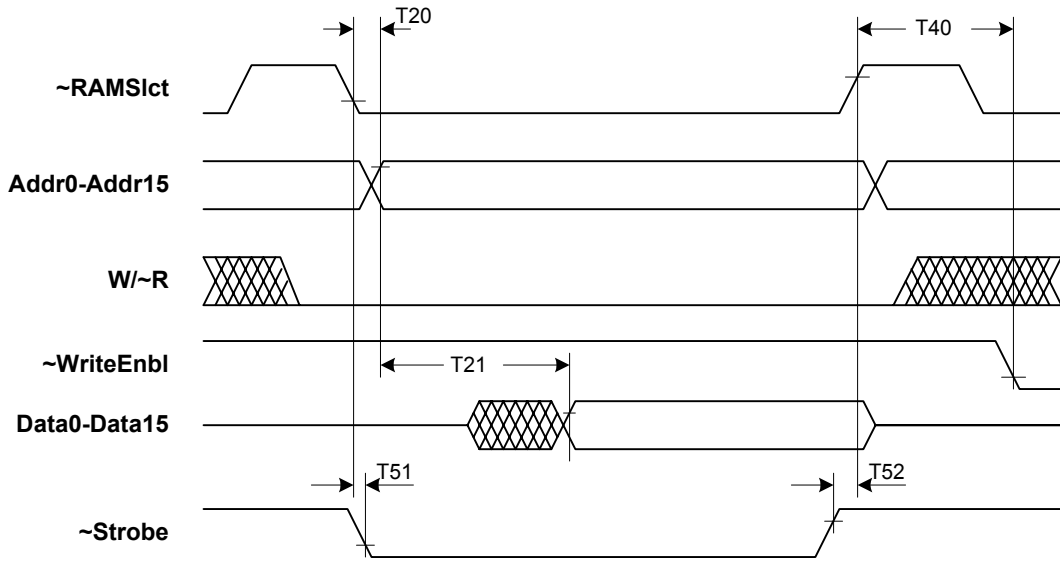
4.6.4 Status read, 16/16 mode



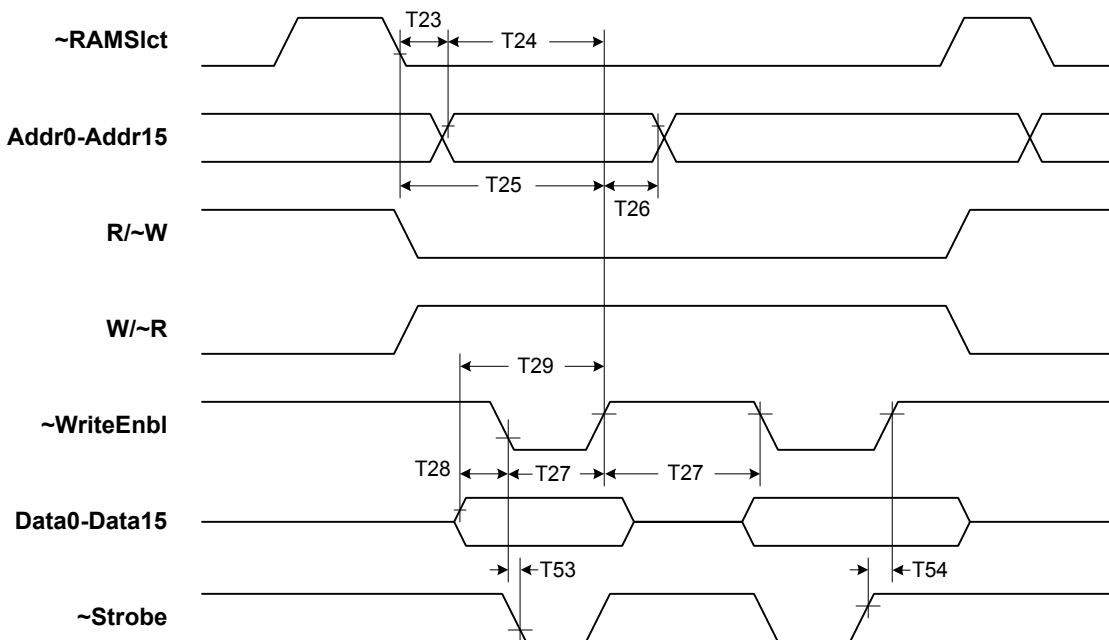
4.7 External memory timing

4.7.1 External memory read

Note: PMD recommends using memory with an access time no greater than 15 nsec.

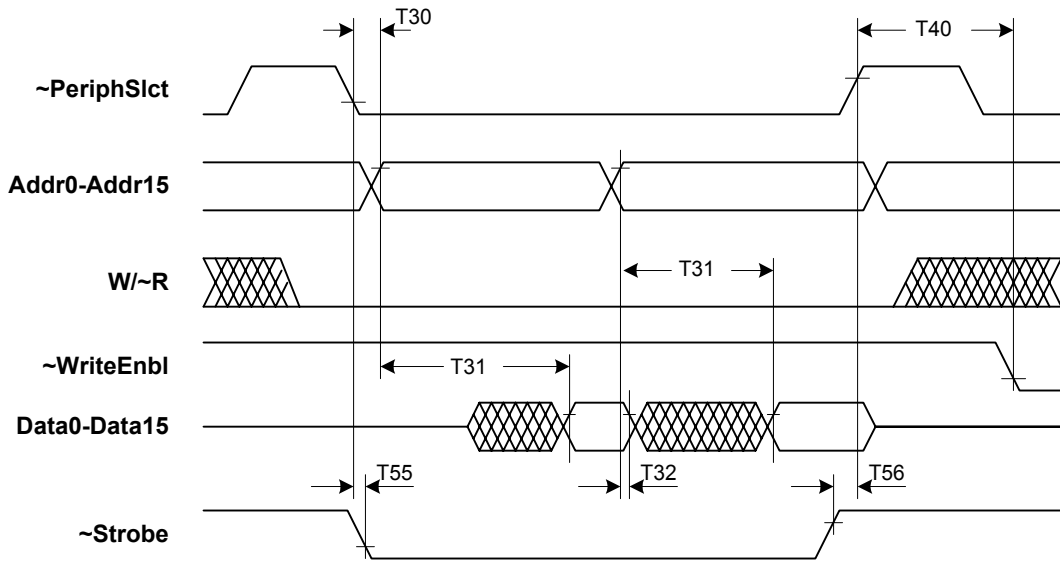


4.7.2 External memory write

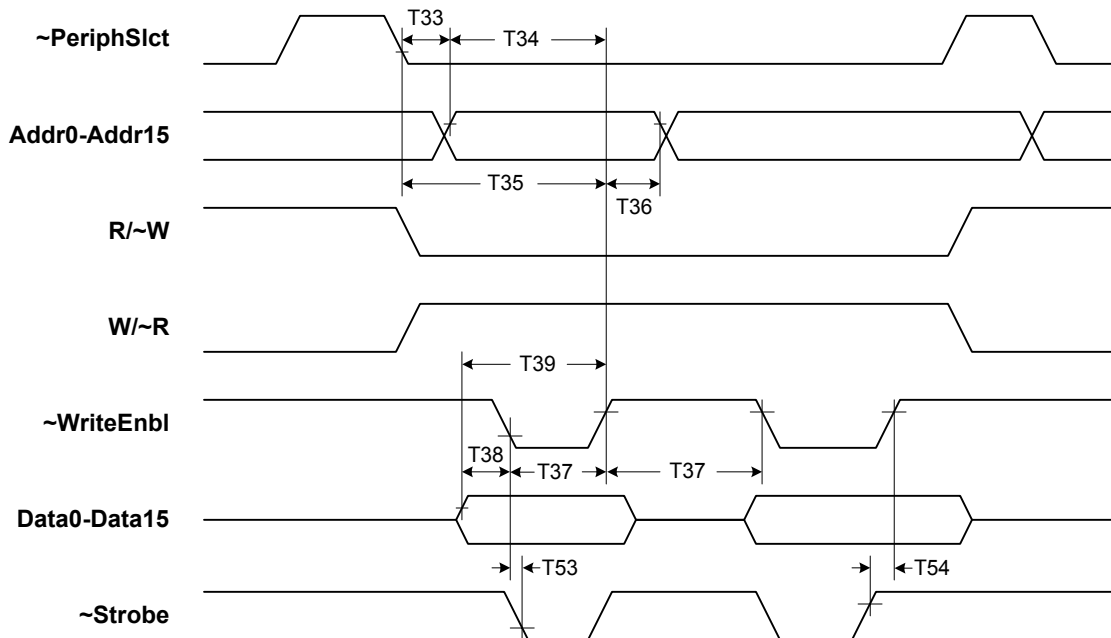


4.8 Peripheral device timing

4.8.1 Peripheral device read

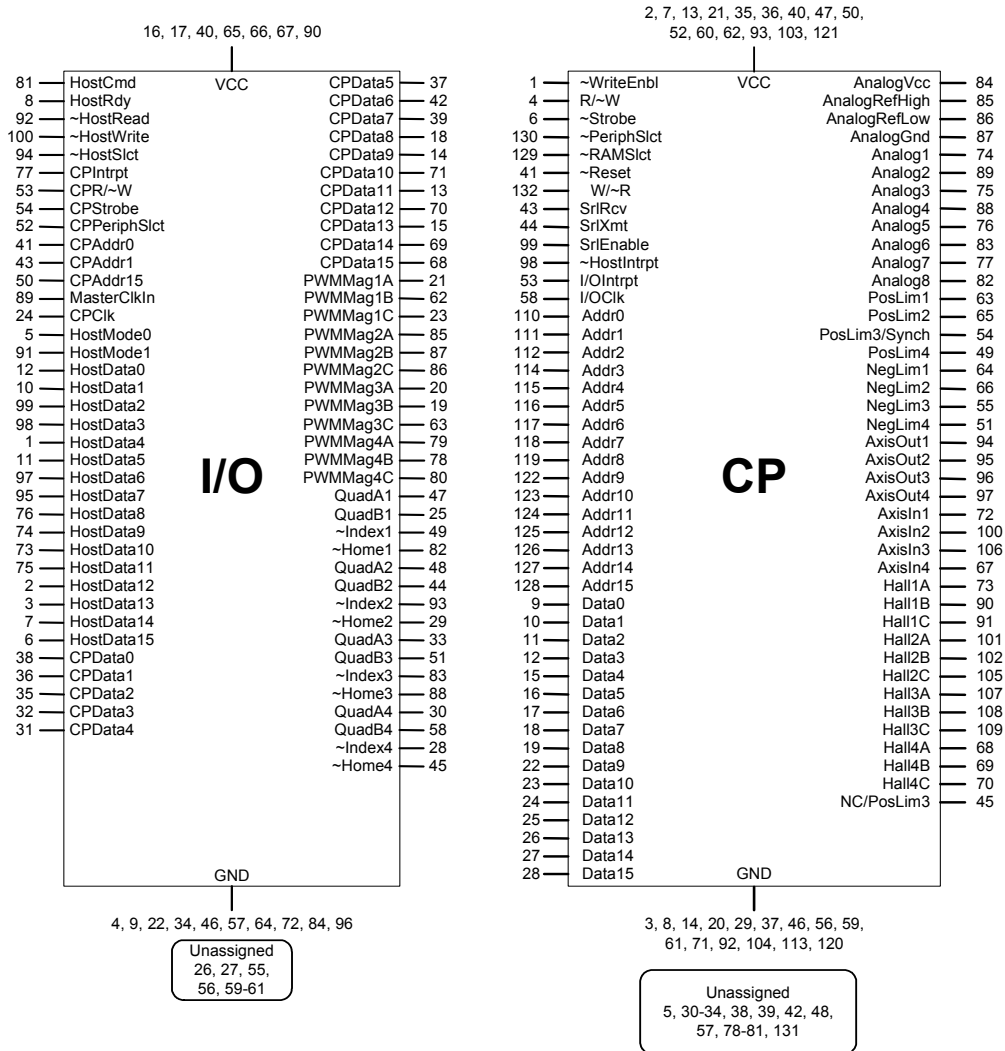


4.8.2 Peripheral device write

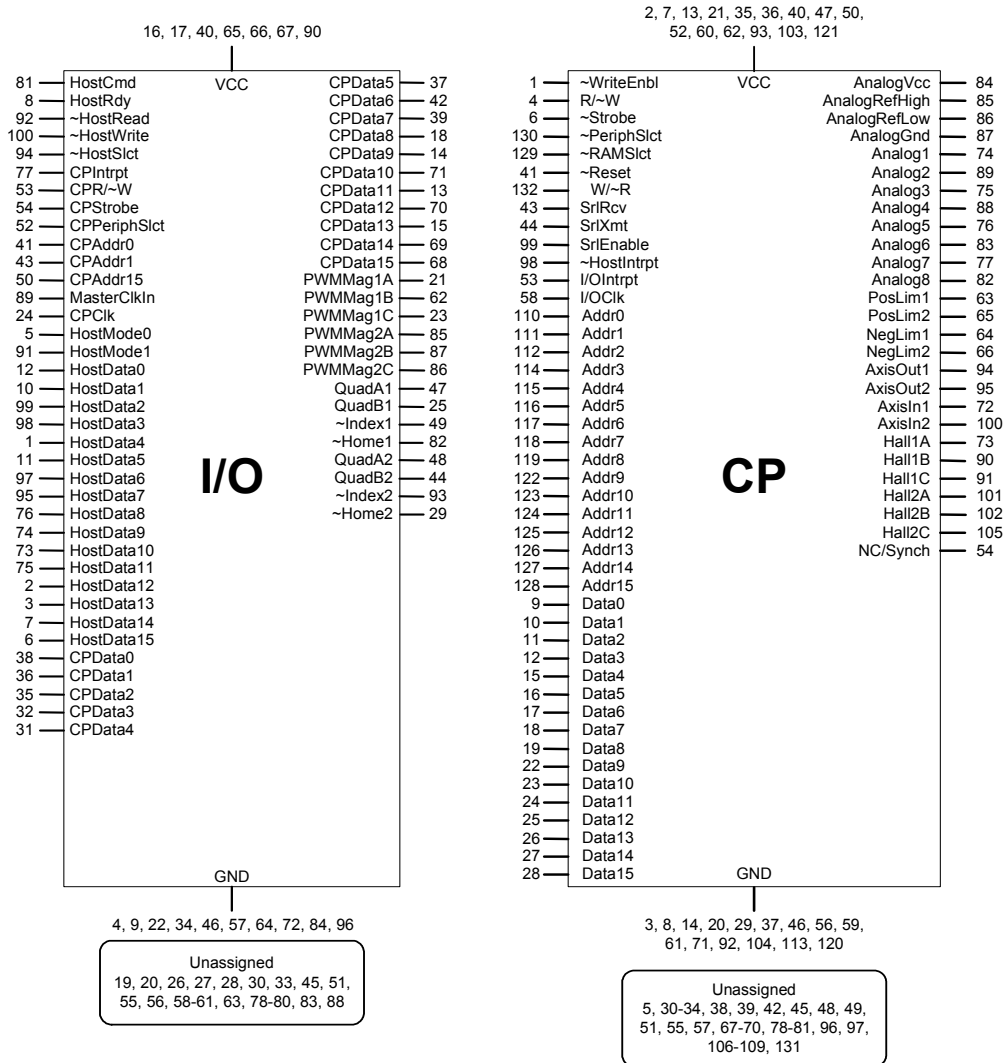


5 Pinouts and Pin Descriptions

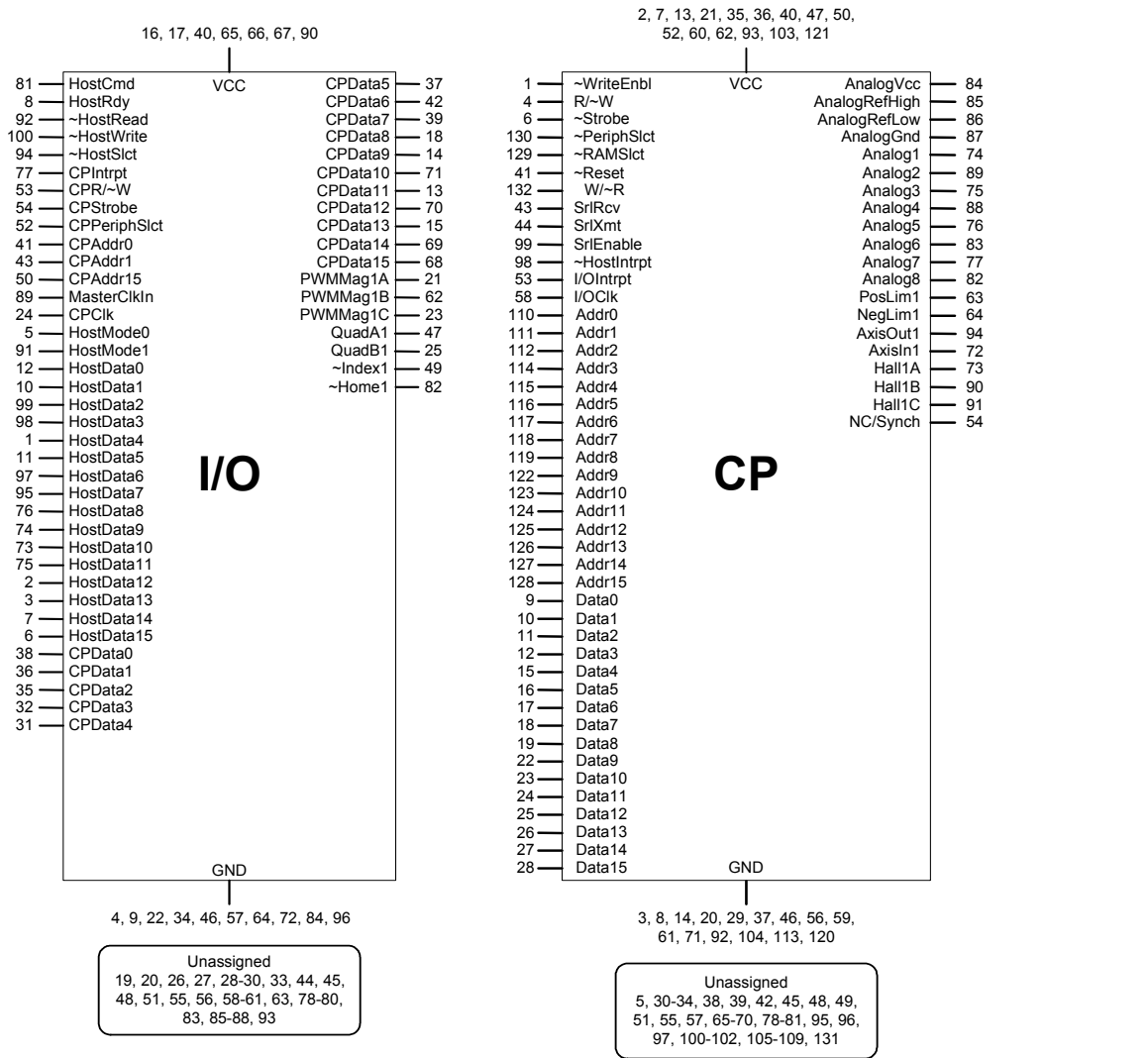
5.1 Pinouts for MC2340



5.2 Pinouts for MC2320



5.3 Pinouts for MC2310



5.4 Pin description tables

5.4.1 I/O chip

| | | I/O Chip | |
|--------------------------------|----------------|-----------|---|
| Pin Name and number | | Direction | Description |
| HostCmd | 81 | Input | This signal is asserted <i>high</i> to write a host instruction to the Motion Processor, or to read the status of the HostRdy and HostIntrpt signals. It is asserted <i>low</i> to read or write a data word. |
| HostRdy | 8 | Output | This signal is used to synchronize communication between the Motion Processor and the host. HostRdy will go <i>low</i> (indicating host port busy) at the end of a read or write operation according to the interface mode in use, as follows: Interface Mode HostRdy goes low 8/8 after the instruction byte is transferred after the second byte of each data word is transferred 8/16 after the second byte of the instruction word after the second byte of each data word is transferred 16/16 after the 16-bit instruction word after each 16-bit data word serial <i>n/a</i> HostRdy will go <i>high</i> , indicating that the host port is ready to transmit, when the last transmission has been processed. All host port communications must be made with HostRdy high (ready). A typical busy-to-ready cycle is 12.5 microseconds. |
| ~HostRead | 92 | Input | When ~HostRead is <i>low</i> , a data word is read from the Motion Processor. |
| ~HostWrite | 100 | Input | When ~HostWrite is <i>low</i> , a data word is written to the Motion Processor. |
| ~HostSlct | 94 | Input | When ~HostSlct is <i>low</i> , the host port is selected for reading or writing operations. |
| CPIntrpt | 77 | Output | I/O chip to CP chip interrupt. This signal sends an interrupt to the CP chip whenever a host–chipset transmission occurs. It should be connected to CP chip pin 53, I/OIntrpt . |
| CPR/~W | 53 | Input | This signal is <i>high</i> when the I/O chip is reading data from the I/O chip, and <i>low</i> when it is writing data. It should be connected to CP chip pin 4, R/W . |
| CPStrobe | 54 | Input | This signal goes <i>low</i> when the data and address become valid during Motion Processor communication with peripheral devices on the data bus, such as external memory or a DAC. It should be connected to CP chip pin 6, Strobe . |
| CPPeriphSlct | 52 | Input | This signal goes <i>low</i> when a peripheral device on the data bus is being addressed. It should be connected to CP chip pin 130, PeriphSlct . |
| CPAddr0 CPAddr1 CPAddr15 | 41 43 50 | Input | These signals are <i>high</i> when the CP chip is communicating with the I/O chip (as distinguished from any other device on the data bus). They should be connected to CP chip pins 110 (Addr0), 111 (Addr1), and 128 (Addr15). |
| MasterClkn | 89 | Input | This is the master clock signal for the Motion Processor. It is driven at a nominal 40 MHz |

I/O Chip

| Pin Name and number | | Direction | Description |
|--|--|------------------------------|---|
| CPClk | 24 | Output | This signal provides the clock pulse for the CP chip. Its frequency is half that of MasterClkIn (pin 89), or 20 MHz nominal. It is connected directly to the CP chip I/Oclk signal (pin 58). |
| HostMode1 HostMode0 | 91 5 | Input | These two signals determine the host communications mode, as follows: HostMode1 HostMode0 0 0 16/16 parallel (16-bit bus, 16-bit instruction) 0 1 8/8 parallel (8-bit bus, 8-bit instruction) 1 0 8/16 parallel (8-bit bus, 16-bit instruction) 1 1 serial |
| HostData0 HostData1 HostData2 HostData3 HostData4 HostData5 HostData6 HostData7 HostData8 HostData9 HostData10 HostData11 HostData12 HostData13 HostData14 HostData15 | 12 10 99 98 1 11 97 95 76 74 73 75 2 3 7 6 | Bi-directional, tri-state | These signals transmit data between the host and the Motion Processor through the parallel port. Transmission is mediated by the control signals ~HostSlct , ~HostWrite , ~HostRead and HostCmd . In 16 bit mode all 16 bits are used (HostData0-15). In 8 bit mode only the low-order 8 bits of data are used (HostData0-7). The HostMode0 and HostMode1 signals select the communication mode this port operates in. |
| CPData0 CPData1 CPData2 CPData3 CPData4 CPData5 CPData6 CPData7 CPData8 CPData9 CPData10 CPData11 CPData12 CPData13 CPData14 CPData15 | 38 36 35 32 31 37 42 39 18 14 71 13 70 15 69 68 | Bi-directional | These signals transmit data between the I/O chip and pins Data0-15 of the CP chip, via the Motion Processor data bus. |
| PWMMag1A PWMMag1B PWMMag1C PWMMag2A PWMMag2B PWMMag2C PWMMag3A PWMMag3B PWMMag3C PWMMag4A PWMMag4B PWMMag4C | 21 62 23 85 87 86 20 19 63 79 78 80 | Output | These pins provide the Pulse Width Modulated signals for each phase to the motor. In PWM 50/50 output mode the sign (direction) is encoded within each signal. Refer to the User's Guide for more information. The PWM resolution is 10 bits at a frequency of 20.0 KHz. For MC2340 all pins are valid. For MC2320 only PWMMag1A-C and PWMMag2A-C are valid. For MC2310 only PWMMag1A-C is valid. Invalid or unused pins may be left unconnected. |

I/O Chip

| Pin Name and number | Direction | Description |
|--|--------------------------------------|--|
| QuadA1 47 QuadB1 25 QuadA2 48 QuadB2 44 QuadA3 33 QuadB3 51 QuadA4 30 QuadB4 58 | Input | <p>These pins provide the A and B quadrature signals for the incremental encoder for each axis. When the axis is moving in the positive (forward) direction, signal A leads signal B by 90°.</p> <p>The theoretical maximum encoder pulse rate is 5.1 MHz. Actual maximum rate will vary, depending on signal noise.</p> <p>NOTE: Many encoders require a pull-up resistor on each signal to establish a proper high signal. Check your encoder's electrical specifications).</p> <p>For MC2340 all 8 pins are valid. For MC2320 only the first four pins (axes 1 and 2) are valid.</p> <hr/> <p>WARNING! If a valid axis pin is not used, its signal must be tied high.</p> <hr/> <p>Invalid axis pins may be left unconnected.</p> |
| ~Index1 49 ~Index2 93 ~Index3 83 ~Index4 28 | Input | <p>These pins provide the Index quadrature signals for the incremental encoders. A valid index pulse is recognized by the chip set when ~Index, A, and B are all <i>low</i>.</p> <p>For MC2340 all 4 pins are valid. For MC2320 only ~Index1 and ~Index2 are valid. For MC2310 only ~Index1 is valid.</p> <hr/> <p>WARNING! If a valid axis pin is not used, its signal must be tied high.</p> <hr/> <p>Invalid axis pins may be left unconnected.</p> |
| ~Home1 82 ~Home2 29 ~Home3 88 ~Home4 45 | Input | <p>These pins provide the Home signals, general-purpose inputs to the position-capture mechanism. A valid Home signal is recognized by the chipset when ~Home_n goes <i>low</i>. These signals are similar to ~Index, but are not gated by the A and B encoder channels.</p> <p>For MC2340 all 4 pins are valid. For MC2320 only ~Home1 and ~Home2 are valid. For MC2310 only ~Home1 is valid.</p> <hr/> <p>WARNING! If a valid axis pin is not used, its signal must be tied high.</p> <hr/> <p>Invalid axis pins may be left unconnected.</p> |
| Vcc | 16, 17, 40, 65, 66, 67, 90 | All of these pins must be connected to the I/O chip's digital supply voltage, which should be in the range 4.75 to 5.25 V. |
| GND | 4, 9, 22, 34, 46, 57, 64, 72, 84, 96 | I/O chip ground. All of these pins must be connected to the digital power supply return. |
| unassigned | 26, 27, 55, 56, 59-61, | These pins may be left unconnected (floating). |

5.4.2 CP chip

CP chip

| Pin Name and number | | Direction | Description |
|---------------------|-----|----------------|---|
| ~WriteEnbl | 1 | output | When <i>low</i> , this signal enables data to be written to the bus. |
| R/~W | 4 | output | This signal is <i>high</i> when the CP chip is performing a read, and <i>low</i> when it is performing a write. It should be connected to I/O chip pin 53, CPR/~W. |
| ~Strobe | 6 | output | This signal is <i>low</i> when the data and address are valid during CP communications. It should be connected to I/O chip pin 54, CPStrobe. |
| ~PeriphSlct | 130 | output | This signal is <i>low</i> when peripheral devices on the data bus are being addressed. It should be connected to I/O chip pin 52, CPPeriphSlct. |
| ~RAMSlct | 129 | output | This signal is <i>low</i> indicates when external memory is being accessed. |
| ~Reset | 41 | input | This is the master reset signal. When brought <i>low</i> , this pin resets the chipset to its initial conditions. |
| W/~R | 132 | output | This signal is the inverse of R/~W; it is <i>high</i> when R/~W is low, and vice versa. For some decode circuits this is more convenient than R/~W. |
| SrlRcv | 43 | input | This pin receives serial data from the asynchronous serial port. NOTE! If this signal is not used, it should be tied high. |
| SrlXmt | 44 | output | This pin transmits serial data to the asynchronous serial port. |
| SrlEnable | 99 | output | This pin sets the serial port enable line. SrlEnable is always <i>high</i> for the point-to-point protocol and is <i>high</i> during transmission for the multi-drop protocol. |
| ~HostIntrpt | 98 | output | When <i>low</i> , this signal causes an interrupt to be sent to the host processor. |
| I/OIntrpt | 53 | input | This signal interrupts the CP chip when a host I/O transfer is complete. It should be connected to I/O chip pin 77, CPIIntrpt. |
| Data0 | 9 | Bi-directional | Multi-purpose data lines. These pins comprise the CP chip's external data bus, used for all communications with the I/O chip and peripheral devices such as external memory or DACs. They may also be used for parallel-word input and for user-defined I/O operations. |
| Data1 | 10 | | |
| Data2 | 11 | | |
| Data3 | 12 | | |
| Data4 | 15 | | |
| Data5 | 16 | | |
| Data6 | 17 | | |
| Data7 | 18 | | |
| Data8 | 19 | | |
| Data9 | 22 | | |
| Data10 | 23 | | |
| Data11 | 24 | | |
| Data12 | 25 | | |
| Data13 | 26 | | |
| Data14 | 27 | | |
| Data15 | 28 | | |

CP chip

| Pin Name and number | Direction | Description |
|--|--|-------------|
| Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7 Addr8 Addr9 Addr10 Addr11 Addr12 Addr13 Addr14 Addr15 | 110 111 112 114 115 116 117 118 119 122 123 124 125 126 127 128 | output |
| Multi-purpose Address lines. These pins comprise the CP chip's external address bus, used to select devices for communication over the data bus. Addr0 , Addr1 , and Addr15 are connected to the corresponding CPAddr pins on the I/O chip, and are used to communicate between the CP and I/O chips. Other address pins may be used for DAC output, parallel word input, or user-defined I/O operations. See the <i>Navigator Motion Processor User's Guide</i> for a complete memory map. | | |
| I/OClk | 58 | input |
| This is the CP chip clock signal. It should be connected to I/O chip pin 24, CPClk . | | |
| AnalogVcc | 84 | input |
| CP chip analog power supply voltage. This pin must be connected to the analog input supply voltage, which must be in the range 4.5-5.5 V If the analog input circuitry is not used, this pin may be left unconnected. | | |
| AnalogRefHigh | 85 | input |
| CP chip analog high voltage reference for A/D input. The allowed range is AnalogRefLow to AnalogVcc . If the analog input circuitry is not used, this pin may be left unconnected. | | |
| AnalogRefLow | 86 | input |
| CP chip analog low voltage reference for A/D input. The allowed range is AnalogGND to AnalogRefHigh . If the analog input circuitry is not used, this pin may be left unconnected. | | |
| AnalogGND | 87 | |
| CP chip analog input ground. This pin must be connected to the analog input power supply return. If the analog input circuitry is not used, this pin may be left unconnected. | | |
| Analog1 Analog2 Analog3 Analog4 Analog5 Analog6 Analog7 Analog8 | 74 89 75 88 76 83 77 82 | input |
| These signals provide general-purpose analog voltage levels which are sampled by an internal A/D converter. The A/D resolution is 10 bits. The allowed range is AnalogRefLow to AnalogRefHigh . | | |
| PosLim1 PosLim2 PosLim4 | 63 65 49 | input |
| These signals provide inputs from the positive-side (forward) travel limit switches. On power-up or Reset these signals default to active <i>low</i> interpretation, but the interpretation can be set explicitly using the SetSignalSense instruction. For MC2340 all 4 pins are valid. For MC2320 only PosLim1 and PosLim2 are valid. For MC2310 only PosLim1 is valid. | | |
| WARNING! If a valid axis pin is not used, its signal must be tied high. PosLim2 is an output during device reset and as such any connection to GND or V_{cc} must be via a series resistor. | | |
| Invalid axis pins may also be left unconnected. | | |

CP chip

| Pin Name and number | | Direction | Description |
|--|--|--------------|---|
| PosLim3/ Synch | 54 | input/output | <p>On the MC2340 chipset, this pin is the positive-side (forward) travel limit switch for axis#3. On the MC2320 and MC2310 chipsets this pin is not used.</p> <p>On the MC23x3 chipset, this pin is the synchronization signal. In the disabled mode, the pin is configured as an input and is not used. In the master mode, the pin outputs a synchronization pulse that can be used by slave nodes or other devices to synchronize with the internal chip cycle of the master node. In the slave mode, the pin is configured as an input and a pulse on the pin synchronizes the internal chip cycle.</p> <hr/> <p>WARNING! If a valid axis limit pin is not used, its signal should be tied high.</p> |
| NC/PosLim3 | 45 | input | <p>On the MC23x0 chipset, this pin is not used.</p> <p>On the MC2343 chipset, this pin is the positive-side (forward) travel limit switch for axis#3. On the MC2323 and MC2313 chipsets this pin is not used.</p> <hr/> <p>WARNING! If a valid axis limit pin is not used, its signal should be tied high.</p> |
| NegLim1 NegLim2 NegLim3 NegLim4 | 64 66 55 51 | input | <p>These signals provide inputs from the negative-side (reverse) travel limit switches. On power-up or Reset these signals default to active <i>low</i> interpretation, but the interpretation can be set explicitly using the SetSignalSense instruction. For MC2340 all 4 pins are valid. For MC2320 only NegLim1 and NegLim2 are valid. For MC2310 only NegLim1 is valid.</p> <hr/> <p>WARNING! If a valid axis pin is not used, its signal must be tied high. NegLim1 is an output during device reset and as such any connection to GND or V_{cc} must be via a series resistor.</p> <hr/> <p>Invalid axis pins may also be left unconnected.</p> |
| AxisOut1 AxisOut2 AxisOut3 AxisOut4 | 94 95 96 97 | output | <p>Each of these pins can be conditioned to track the state of any bit in the Status registers associated with its axis.</p> <p>For MC2340 all 4 pins are valid. For MC2320 only AxisOut1 and AxisOut2 are valid. For MC2310 only AxisOut1 is valid.</p> <p>Invalid or unused pins may be left unconnected.</p> |
| AxisIn1 AxisIn2 AxisIn3 AxisIn4 | 72 100 106 67 | input | <p>These are general-purpose programmable inputs. They may be used as a breakpoint input, to stop a motion axis, or to cause an UPDATE to occur.</p> <p>For MC2340 all 4 pins are valid. For MC2320 only AxisIn1 and AxisIn2 are valid. For MC2310 only AxisIn1 is valid.</p> <p>Invalid or unused pins may be left unconnected.</p> |
| Hall1A Hall1B Hall1C Hall2A Hall2B Hall2C Hall3A Hall3B Hall3C Hall4A Hall4B Hall4C | 73 90 91 101 102 105 107 108 109 68 69 70 | Input | <p>Hall sensor inputs. Each set (A, B, and C) of signals encodes 6 valid states as follows: A on, A and B on, B on, B and C on, C on, C and A on. A sensor is defined as being on when its signal is <i>high</i>.</p> <p>Note: These signals should only be connected to Hall sensors that are mounted at a 120° offset. Schemes which provide Hall signals 60° apart will not work.</p> <p>For MC2340 all 12 pins are valid. For MC2320 only the first six pins (axes 1 and 2) are valid. For MC2310 only the first three pins (axis 1) are valid.</p> <p>Invalid or unused pins may be left unconnected.</p> |

CP chip

| Pin Name and number | Direction | Description |
|---------------------|---|--|
| V _{cc} | 2, 7, 13, 21, 35, 36, 40, 47, 50, 52, 60, 62, 93, 103, 121 | CP digital supply voltage. All of these pins must be connected to the supply voltage. V _{cc} must be in the range 4.75 - 5.25 V. WARNING! Pin 35 must be tied HIGH with a pull-up resistor. A nominal value of 22K Ohms is suggested. |
| GND | 3, 8, 14, 20, 29, 37, 46, 56, 59, 61, 71, 92, 104, 113, 120 | CP ground. All of these pins must be connected to the power supply return. |
| Unassigned (MC2340) | 5, 30-34, 38, 39, 42, 48, 57, 78-81, 131 | These signals may be left unconnected (floating). |

6 Application Notes

6.1 Design Tips

The following are recommendations for the design of circuits that utilize a PMD Motion Processor.

Serial Interface

The serial interface is a convenient interface that can be used before host software has been written to communicate through the parallel interface. It is recommended that even if the serial interface is not utilized as a standard communication interface, that the serial receive and transmit signals are brought to test points so that they may be connected during initial board configuration/debugging. This is especially important during the prototype phase. The serial receive line should include a pull-up resistor to avoid spurious interrupts when it is not connected to a transceiver.

If the serial configuration decode logic is not implemented (see section 6.3) and the serial interface may be used for debugging as mentioned above, the CP data bus should be tied high. This places the serial interface in a default configuration of 9600,n,8,1 after power on or reset.

Controlling PWM output during reset

When the motion processor is in a reset state (when the reset line is held low) or immediately after a power on, the PWM outputs can be in an unknown state, causing undesirable motor movement. It is recommended that the enable line of any motor amplifier be held in a disabled state by the host processor or some logic circuitry until communication to the motion processor is established. This can be in the form of a delay circuit on the amplifier enable line after power up, or the enable line can be ANDed with the CP reset line.

Reducing noise and power consumption

To reduce the emission of electrical noise and reduce power consumption (caused by floating inputs), all unused input signals can be tied through a resistor to Vcc or directly to GND. The following CP pins can be tied if not used: 45, 48, 68-70, 73, 90, 91, 101, 102, 105, 107-109, 78-81.

Parallel word encoder input

When using parallel word input for motor position, it is useful to also decode this information into the User I/O space. This allows the current input value to be read using the chip instruction ReadIO for diagnostic purposes.

Using a non standard system clock frequency

It is often desirable to share a common clock among several components in a design. In the case of the PMD Motion Processors it is possible to use a clock below the standard value of 40MHz. In this case all system frequencies will be reduced as a fraction of the input clock versus the standard 40MHz clock. The list below shows the affected system parameters:-

- Serial baud rate

- PWM carrier frequency
- Timing characteristics as shown in section 3.2
- Cycle time
- Commutation rate

For example, if an input clock of 34MHz is used with a serial baud rate of 9600 the following timing changes will result:-

- Serial baud rate decreases to $9600 \text{ bps} * 34/40 = 8160 \text{ bps}$
- PWM frequency decreases to $20 \text{ KHz} * 34/40 = 17 \text{ KHz}$
- Cycle time per axis increases to $153.6 \mu\text{sec} * 40/34 = 180.71 \mu\text{sec}$
- Commutation rate for MC2310/MC2320 decreases to $20\text{KHz} * 34/40 = 17 \text{ KHz}$
- Commutation rate for MC2340 decreases to $10\text{KHz} * 34/40 = 8.5 \text{ KHz}$

6.2 ISA Bus Interface

A complete, ready-to-use ISA (PC/AT) bus interface circuit has been provided to illustrate Navigator host interfacing, as well as to make it easier for the customer to build a Navigator development system.

The interface between the PMD Navigator chipset and the ISA (PC-AT) bus is shown on the following page.

Comments on Schematic

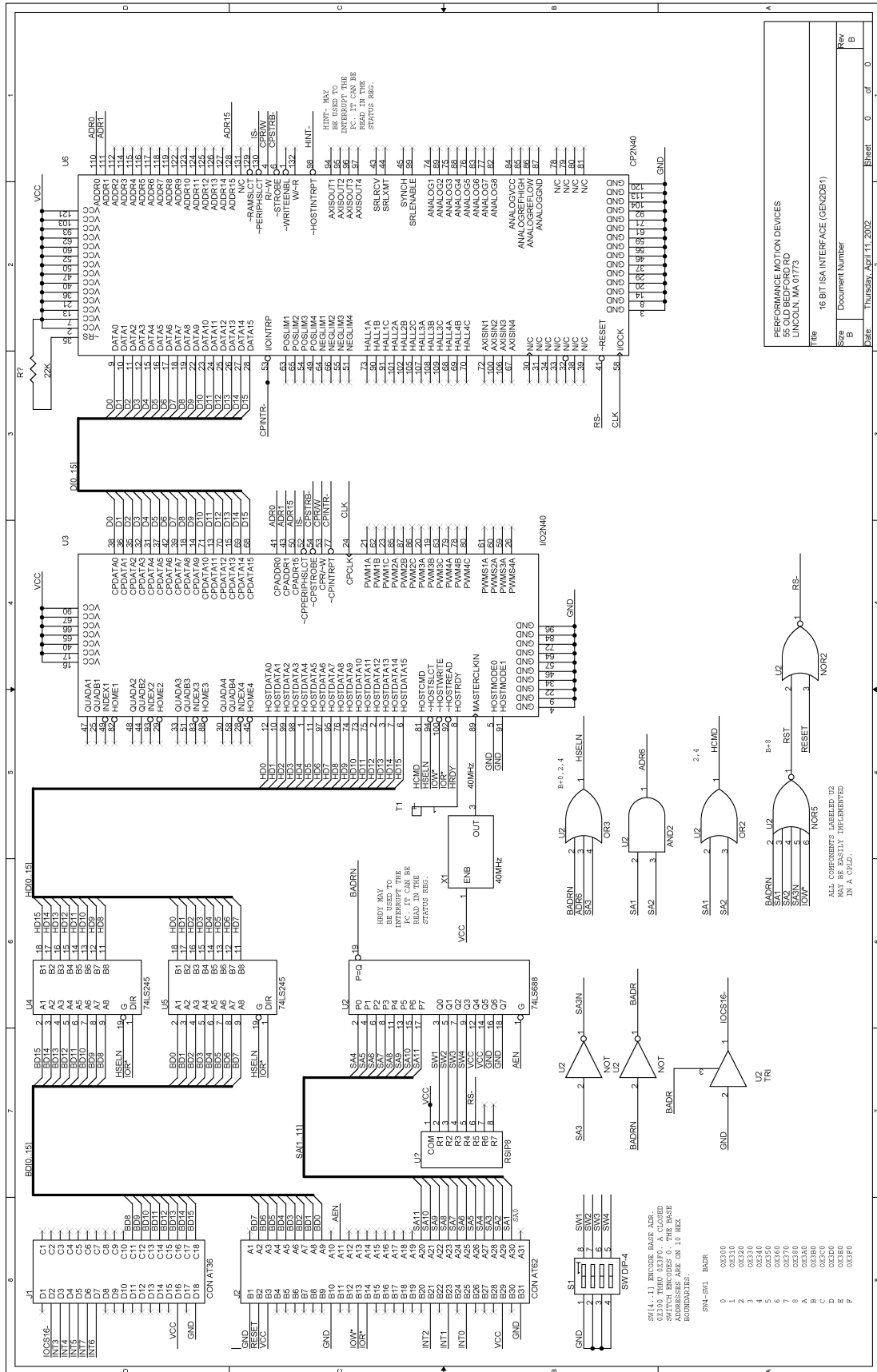
This interface uses a CPLD and two 74LS245s to buffer the data lines. This interface assumes a base address is assigned in the address space of A9-A0, 300-400 hex. These addresses are generally available for prototyping and other system-specific uses without interfering with system assignments. This interface occupies 16 addresses from XX0 to XXF hex though it does not use all the addresses. Four select lines are provided allowing the base address to be set from 300 to 3F0 hex for the select lines SW1-SW4 equal to 0- F respectively. The address assignments used are as follows, where BADR is the base address, 340 hex for example:

| Address | use |
|---------|---------------------------------|
| 340h | read-write data |
| 342h | write command -read status |
| 344h | write command -read status |
| 348h | write reset [Data = don't care] |

The base address (BADR) is decoded in the 74LS688. It is combined with SA1, SA2, and SA3, (BADR+0,2,4) to form HSELN to select the I/O chip and the 245's. (BADR+2,4) asserts HCMD.

Two addresses are used to be compatible with the first generation products, which used BADR+2 to write command and BADR+4 to read status.

B+8 and IOW* generate a reset pulse, -RS, for the CP chip. The reset instruction is OR'd with RESET on the bus to initialize the PMD chipset when the PC is reset.



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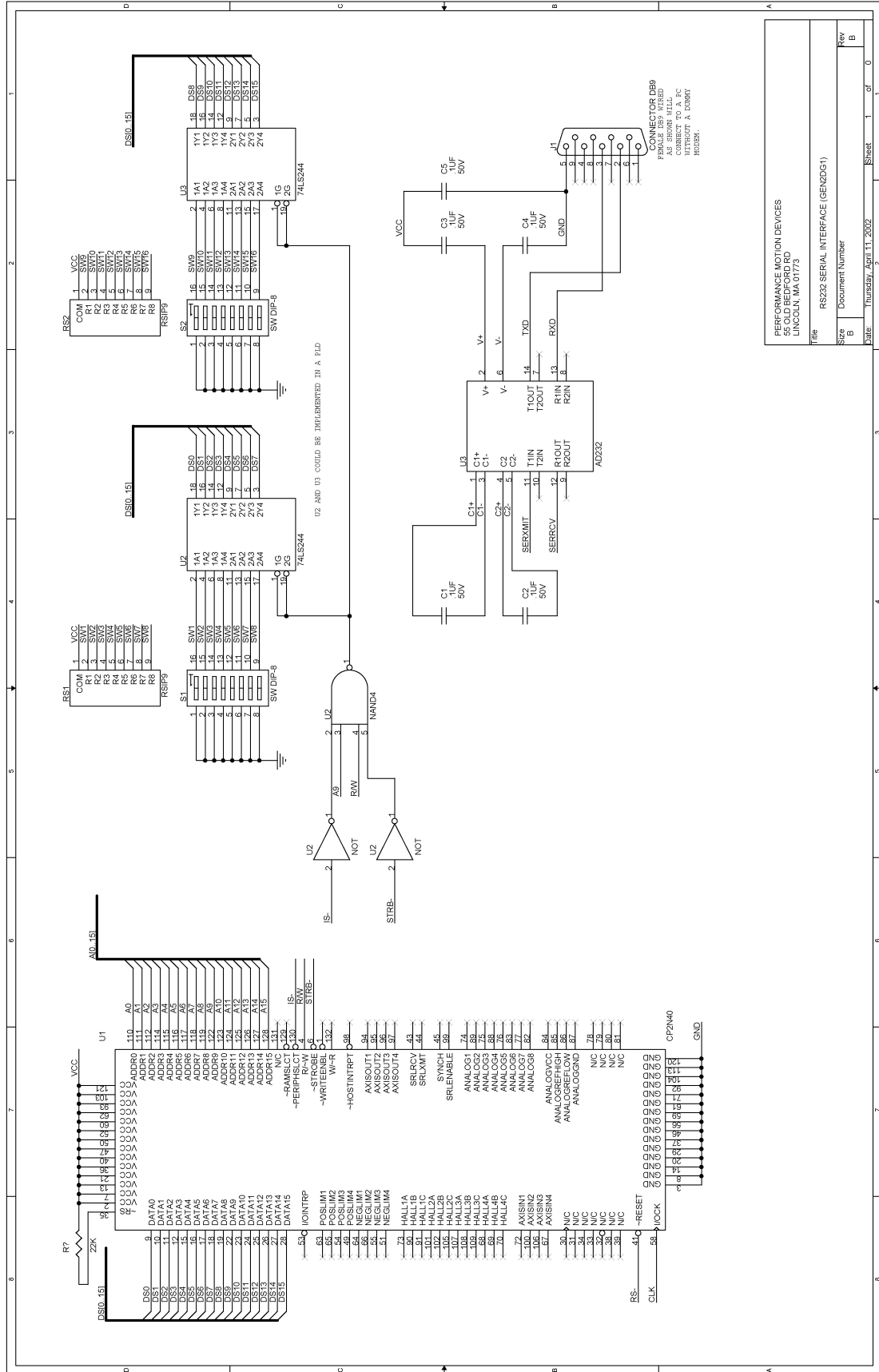
File: 16 BIT ISA INTERFACE (GEN2D81)
Size: 0 of 0
Doc#: Thursday, April 11, 2002 Sheet: 0 of 0

6.3 RS-232 Serial Interface

The interface between the Navigator chipset and an RS-232 serial port is shown in the following figure.

Comments on Schematic

S1 and S2 encode the characteristics of the serial port such as baud rate, number of stop bits, parity, etc. The CP will read these switches during initialization, but these parameters may also be set or changed using the **SetSerialPort** chipset command. The DB9 connector wired as shown can be connected directly to the serial port of a PC without requiring a null modem cable.



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File: RS232 SERIAL INTERFACE (GENZ001)
 Size: Document Number
 Date: Thursday, April 11, 2002 Sheet: 1 of 0

6.4 RS 422/485 Serial Interface

The interface between the Navigator chipset and an RS-422/485 serial port is shown in the following figure.

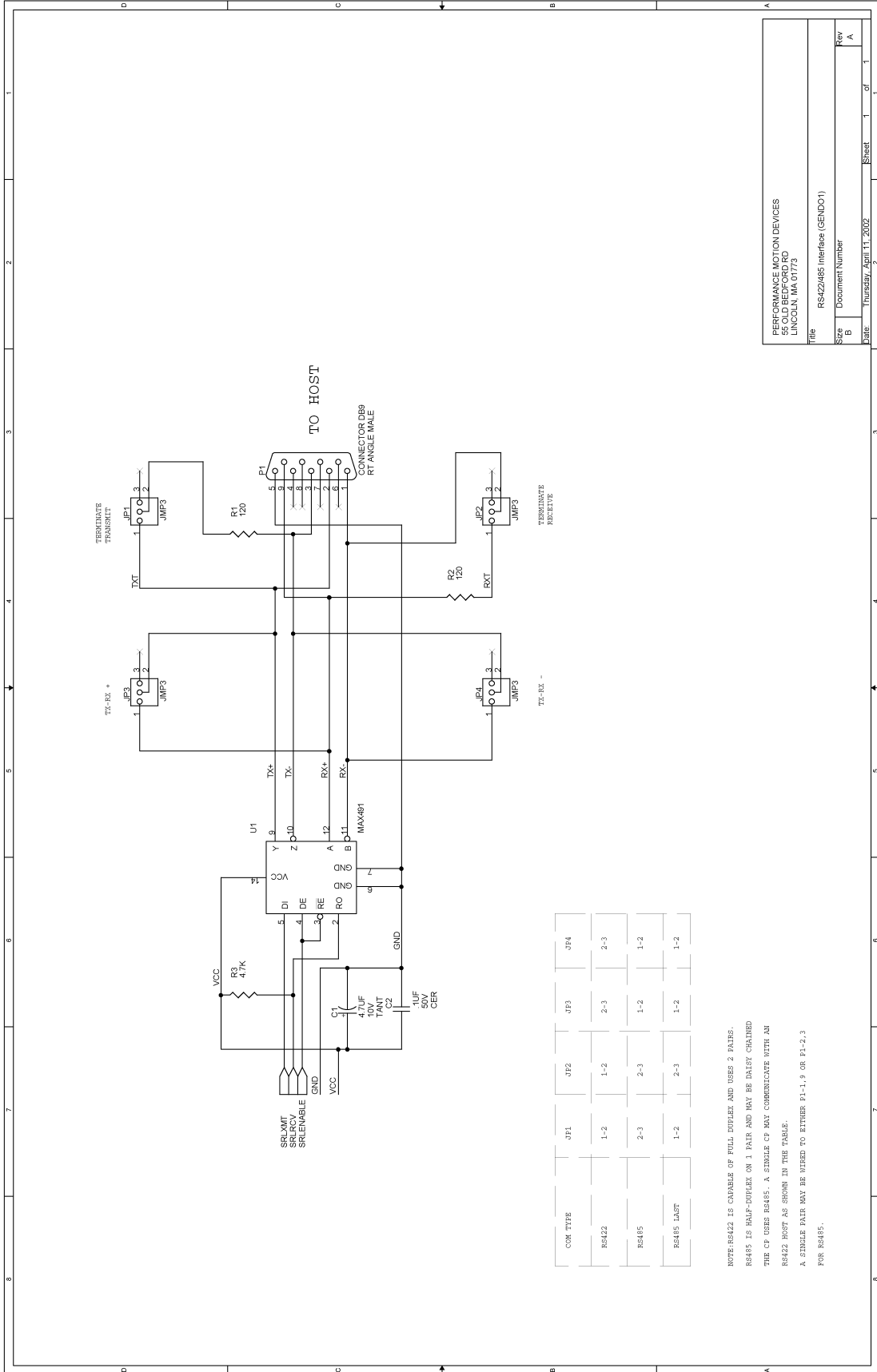
Comments on Schematic

Use the included table to determine the jumper setup that matches the chosen configuration. If using RS485, the last CP must have its jumpers set to RS485 LAST. The DB9 connector wiring is for example only. The DB9 should be wired according to the specification that accompanies the connector to which it is attached.

For correct operation, logic should be provided that contains the start up serial configuration for the chipset. Refer to the RS232 Serial Interface schematic for an example of the required logic.

Note that the RS485 interface cannot be used in point to point mode. It can only be used in a multi-drop configuration where the chip SrlEnable line is used to control transmit/receive operation of the serial transceiver.

Chips in a multi-drop environment should not be operated at different baud rates. This will result in communication problems.



| COM TYPE | JF1 | JF2 | JF3 | JF4 |
|-------------|-----|-----|-----|-----|
| RS422 | 1-2 | 1-2 | 2-3 | 2-3 |
| RS485 | 2-3 | 2-3 | 1-2 | 1-2 |
| RS485 LAOS* | 1-2 | 2-3 | 1-2 | 1-2 |

NOTE: RS422 IS CAPABLE OF FULL DUPLEX AND USES 2 PAIRS.
 RS485 IS HALF-DUPLEX ON 1 PAIR AND MAY BE DAISSY CHAINED.
 THE CP USES RS485. A SINGLE CP MAY COMMUNICATE WITH AN
 RS422 HOST, AS SHOWN IN THE TABLE.
 A SINGLE PAIR MAY BE USED TO EITHER P1-1,9 OR P1-2,3
 FOR RS485.

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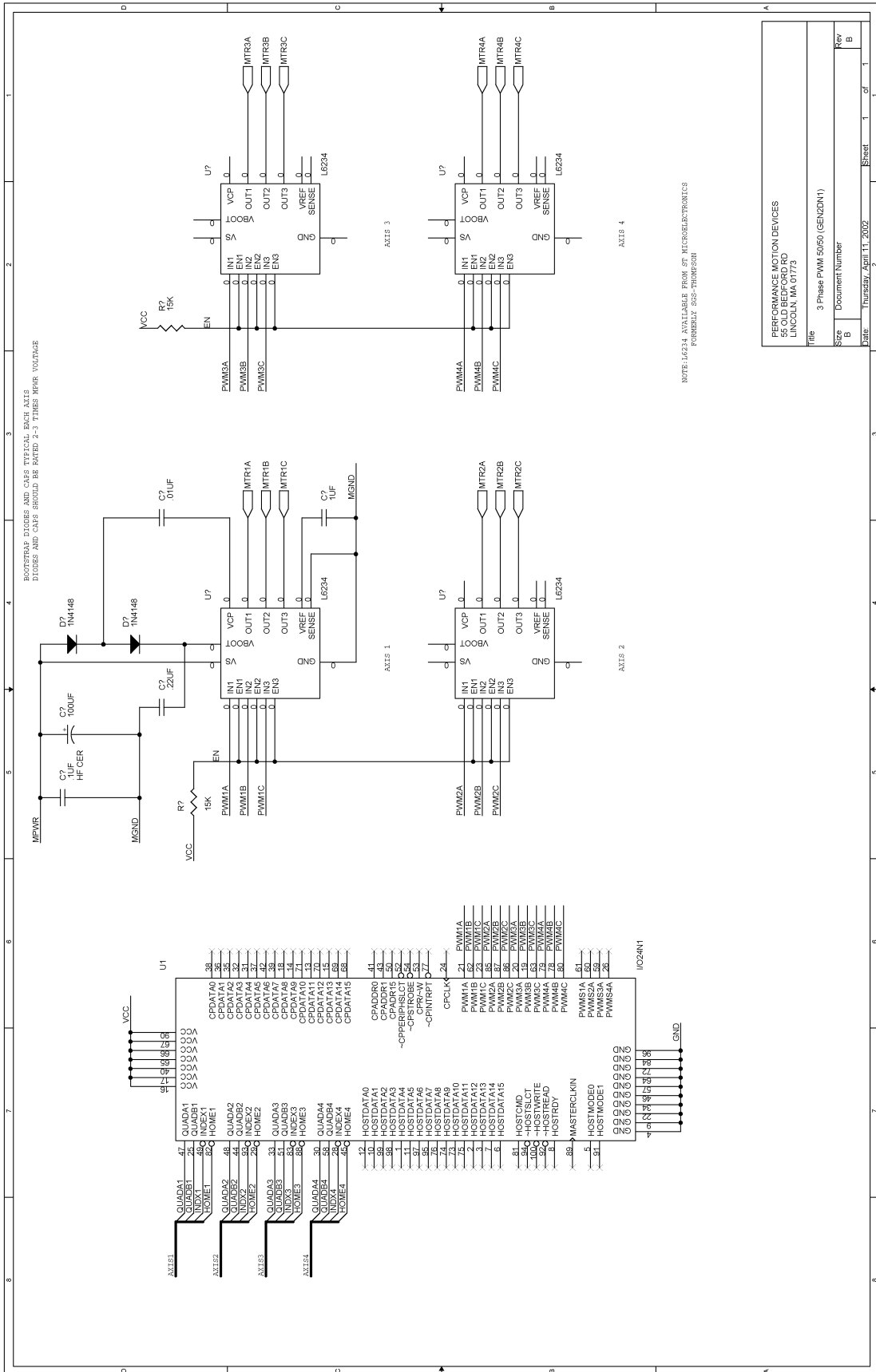
File: RS422/485 Interface (GEND001)
 Size: B Document Number
 Date: Thursday, April 11, 2002 Sheet 1 of 1

6.5 PWM Motor Interface

The following schematic shows a typical interface circuit between the MC2340 and an amplifier used in PWM 50/50 output mode.

Comments on Schematic

The L6234 from ST MicroElectronics is an integrated package that provides 3 half-bridge amplifiers on a single chip. It can drive up to 2 Amps continuous at 52 Volts.



| | |
|-------|----------------------------|
| File | 3 Phase PWM 5050 (GEN00M1) |
| Size | Document Number |
| Rev | B |
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6.6 12-bit Parallel DAC Interface

The interface between the MC2340 chip set and 2 quad 12 bit DAC'S is shown in the following figure.

Comments on Schematic

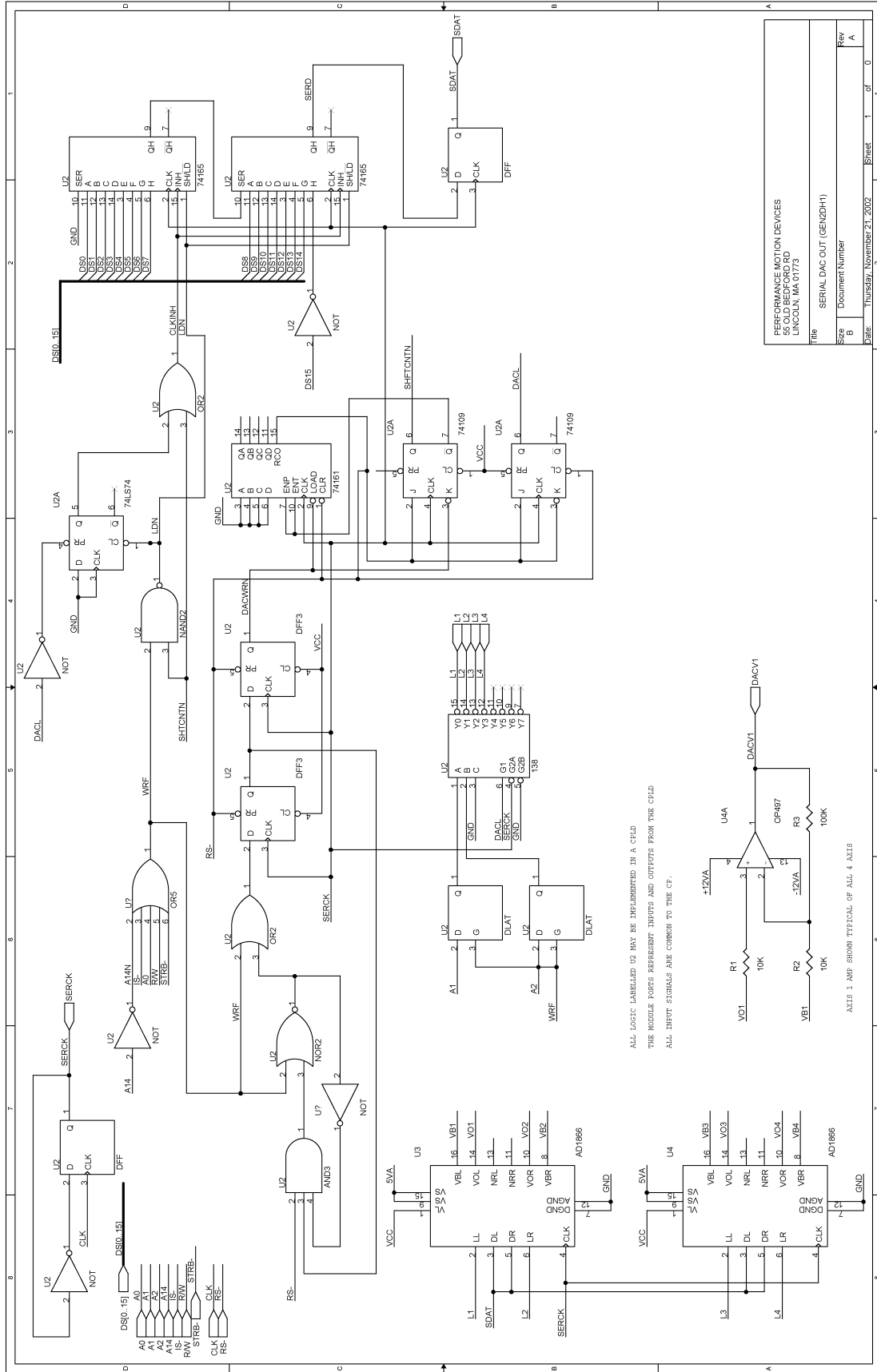
The 12 data bits are written to the DAC addressed by address bits A0 and A1 in Quad DAC 1, when A2 is 0. The 12 data bits are written to the DAC addressed by address bits A0 and A1 in quad DAC 2, when A2 is 1. In this fashion CP addresses 4000,4002,4004,and 4006 are used for axis 1-4, phase A, and 4001,4003, 4005, and 4007, are used for axis 1-4 phase B.

6.7 16-bit Serial DAC Interface

The following schematic shows an interface circuit between the MC2340 and a dual 16-bit serial DAC.

Comments on Schematic

The 16 data bits from the CP chip are latched in the two 74H165 shift registers when the CP writes to address 400x hex, and the address bits A1 and A2 are latched in the 2 DLAT latches and decoded by the 138 CPU cycle. The fed-back and-or gate latches, the decoded WRF, and the next clock will clear the 1st sequencer flop DFF3. This will disable the WRF latch and the second clock will clear the second DFF3 flop, forcing DACWRN low, and setting the first flop since WRF will have gone high. DACWRN low will clear the 74109, SHFTCNTN. The 4 bit counter, 74161, is also parallel loaded to 0, and the counter is enabled by ENP going high. The counter will not start counting nor the shift register start shifting until the clock after the DACWRN flop sets since the load overrides the count enable. When the DACWR flop is set the shift register will start shifting and the counter will count the shifts. After 15 shifts CNT15 from the counter will go high and the next clock will set the DACLAT flop and set the SHFTCNTN flop. This will stop the shift after 16 shifts and assert L1 through L4 depending on the address stored in the latch. The 16th clock also was counted causing the counter to roll over to 0 and CNT15 to go low. The next clock will therefore clear the DACLAT flop causing the DAC latch signal L1 through L4 to terminate and the 16 bits of data to be latched in the addressed DAC. The control logic is now back in its original state waiting for the next write to the DACs by the CP. SERCK is a 10MHz clock, the 20MHz CP clock divided by 2, since the AD1866 DACs will not run at 20MHz.



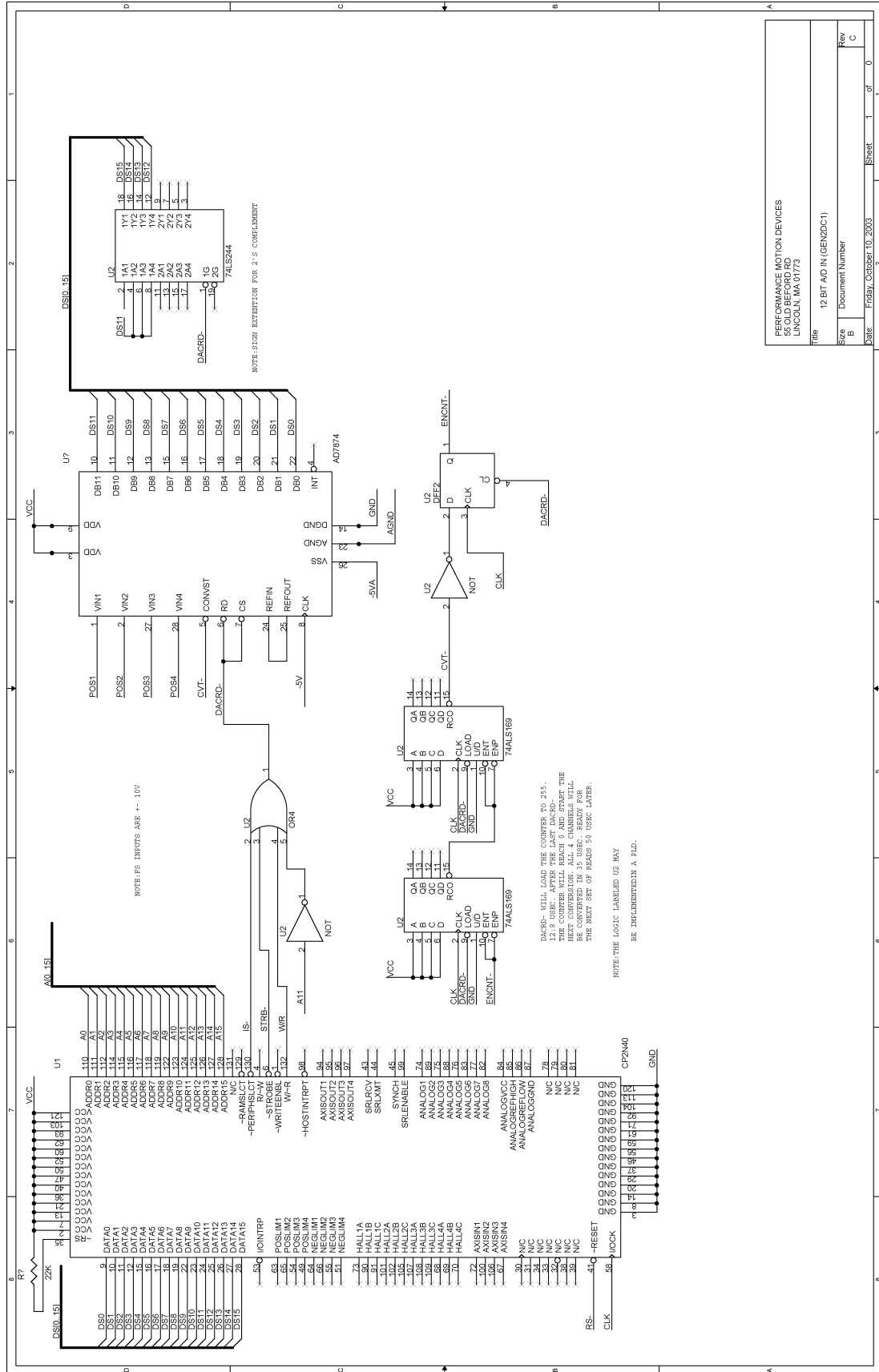
| | | | |
|------|-----------------------------|-----------------|--------|
| FILE | SERIAL DAC OUT (GEN2DH1) | | |
| SIZE | B | Document Number | Rev A |
| DATE | THURSDAY, NOVEMBER 21, 2002 | Sheet | 1 of 0 |

6.8 12-bit A/D Interface

The following schematic shows a typical interface circuit between the Navigator chipset and a quad 12 bit 2's complement A/D converter used as a position input device.

Comments on Schematic

The A/D converter samples all 4 axes and sequentially converts and stores the 2's complement digital words. The data is read out sequentially, axis 1 to 4. DACRD- is used to perform the read and is also used to load the counter to FFh. The counter will be reloaded for each read and will not count significantly between reads. The counter will therefore start counting down after the last read and will generate the cvt- pulse after 12.75 μ sec. The conversions will take approximately 35 μ sec, and the data will be available for the next set of reads after 50 μ sec. The 12 bit words from the A/D are extended to 16 bits with the 74LS244.



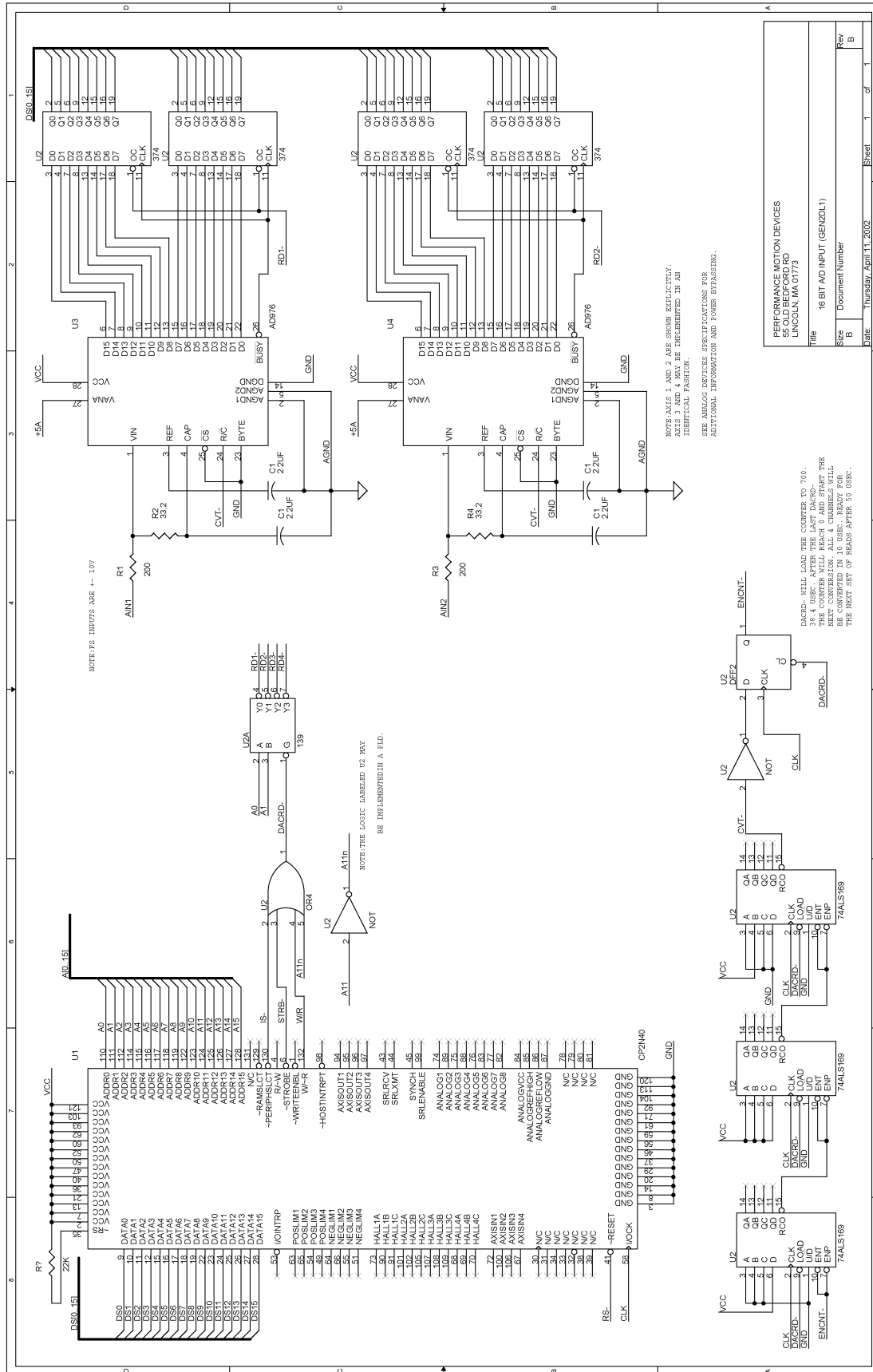
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| PERFORMANCE MOTION DEVICES 55 OLD BEFORD RD LINCOLN, MA 01773 | |
| File | 12 BIT AD IN (GENZDC1) |
| Size | Document Number |
| B | |
| Rev | C |
| Date | Friday, October 10, 2003 |
| Sheet | 1 of 0 |

6.9 16-bit A/D Input

The interface between the Navigator chipset and 16 bit A/D converters as parallel input position devices is shown in the following figure.

Comments on Schematic

The schematic shows a 16 bit A/D used to provide parallel position input to axis 1 and axis 2. The expansion to the remaining two axes is easily implemented. The 374 registers are required on the output of the A/D converters to make the 68-nanosecond access time of the CP. The worst-case timing of the A/D's specify 83 nanoseconds for data on the bus and 83 nanoseconds from data to tri-state on the bus. Each time the data is read the 169 counter is set to 703 decimal. This provides a 35.2-microsecond delay before the next conversion. With a 10-microsecond conversion time the data will be available for the next set of reads after 50 microseconds. The delay is used to provide a position sample close to the actual position.



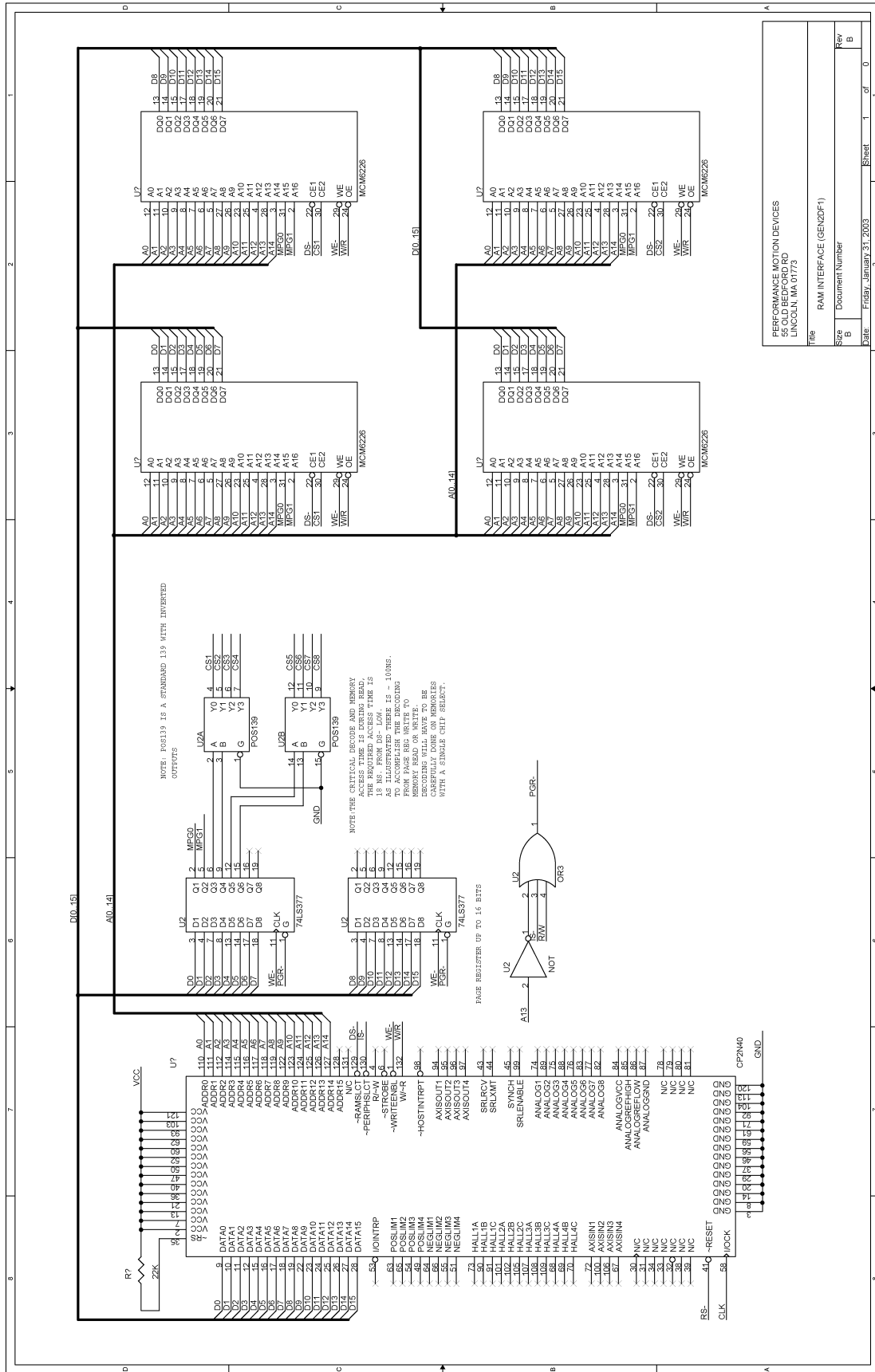
| | |
|-------|----------------------------|
| File | 16 BIT A/D INPUT (GENZDL1) |
| Size | Document Number |
| Date | Thursday, April 11, 2002 |
| Sheet | 1 of 1 |
| Rev | B |

6.10 RAM Interface

The following schematic shows an interface circuit between the Navigator chipset and external ram.

Comments on Schematic

The CP is capable of directly addressing 32K words of 16-bit memory. It will also use a 16 bit paging register to address up to 32K word pages. The schematic shows the paging and addressing for 128KB RAM chips, i.e. 4 pages per RAM chip. The page address decoding is shown for only 6 of the 16 possible paging bits. The decoding time from W/R and DS- to the memory output must not exceed 18 ns. for a read with no wait states. The writes provide 25 extra ns access time for W/R and DS- to reverse the CP data bus.

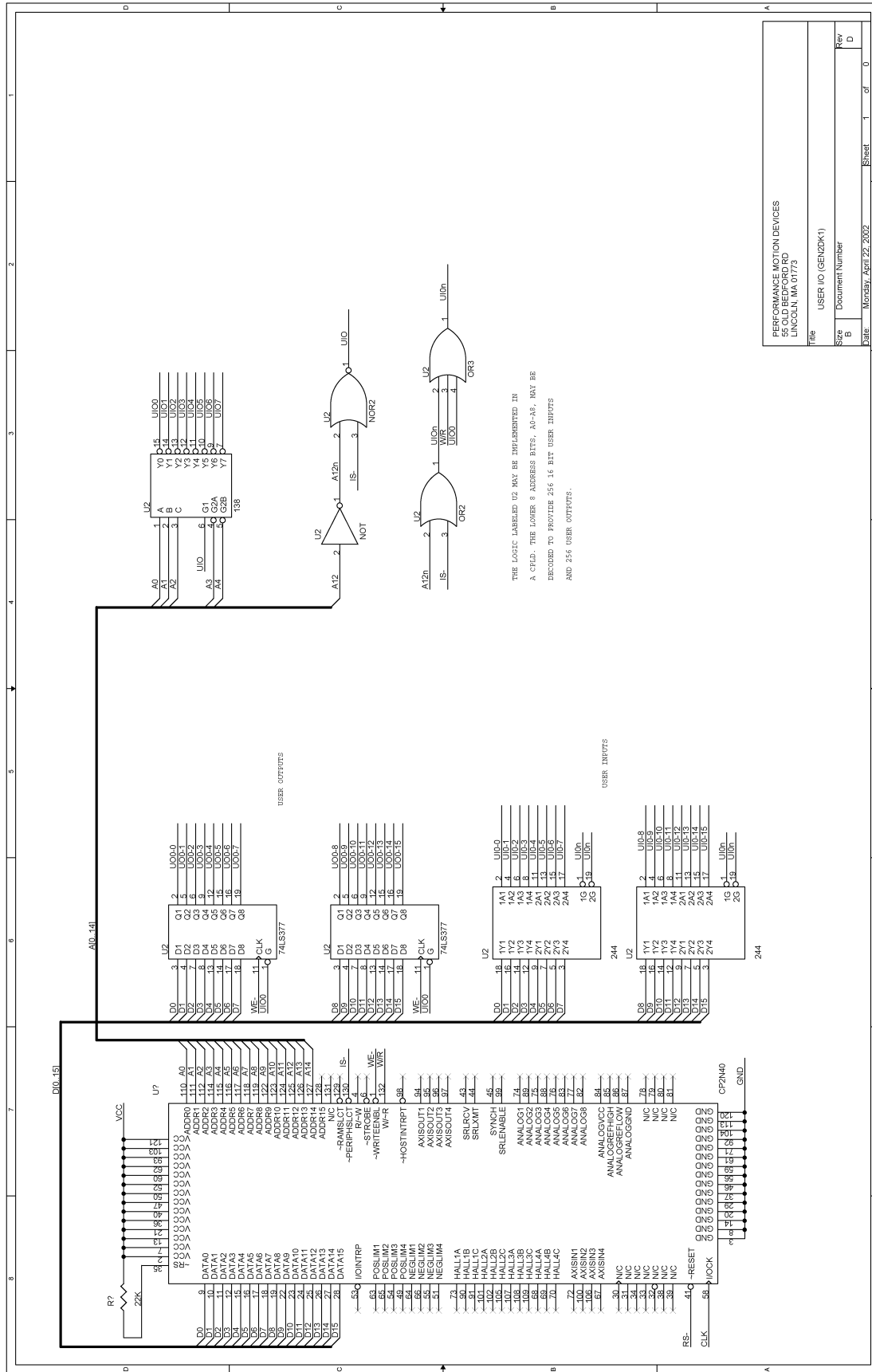


6.11 User-defined I/O

The interface between the Navigator chipset and 16 bits of user output and 16 bits of user input is shown in the following figure.

Comments on Schematic

The schematic implements 1 word of user output registered in the 74LS377's and 1 word of user inputs read via the 244's. The schematic decodes the low 3 bits of the address to 8 possible UIO addresses UIO0 through UIO7. Registers and buffers are shown for only UIO0, but the implementation shown may be easily extended. The lower 8 address bits may be decoded to provide up to 256 user output words and 256 user input words of 16 bits.



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| Title | USER I/O (GEN2DK1) |
| Size | Document Number |
| B | |
| Date | Monday, April 22, 2002 |
| Sheet | 1 of 0 |
| Rev | D |