

ID244E01

4MB Flash Memory Card

(Model No.: ID244E01)

Spec No.: EL093108
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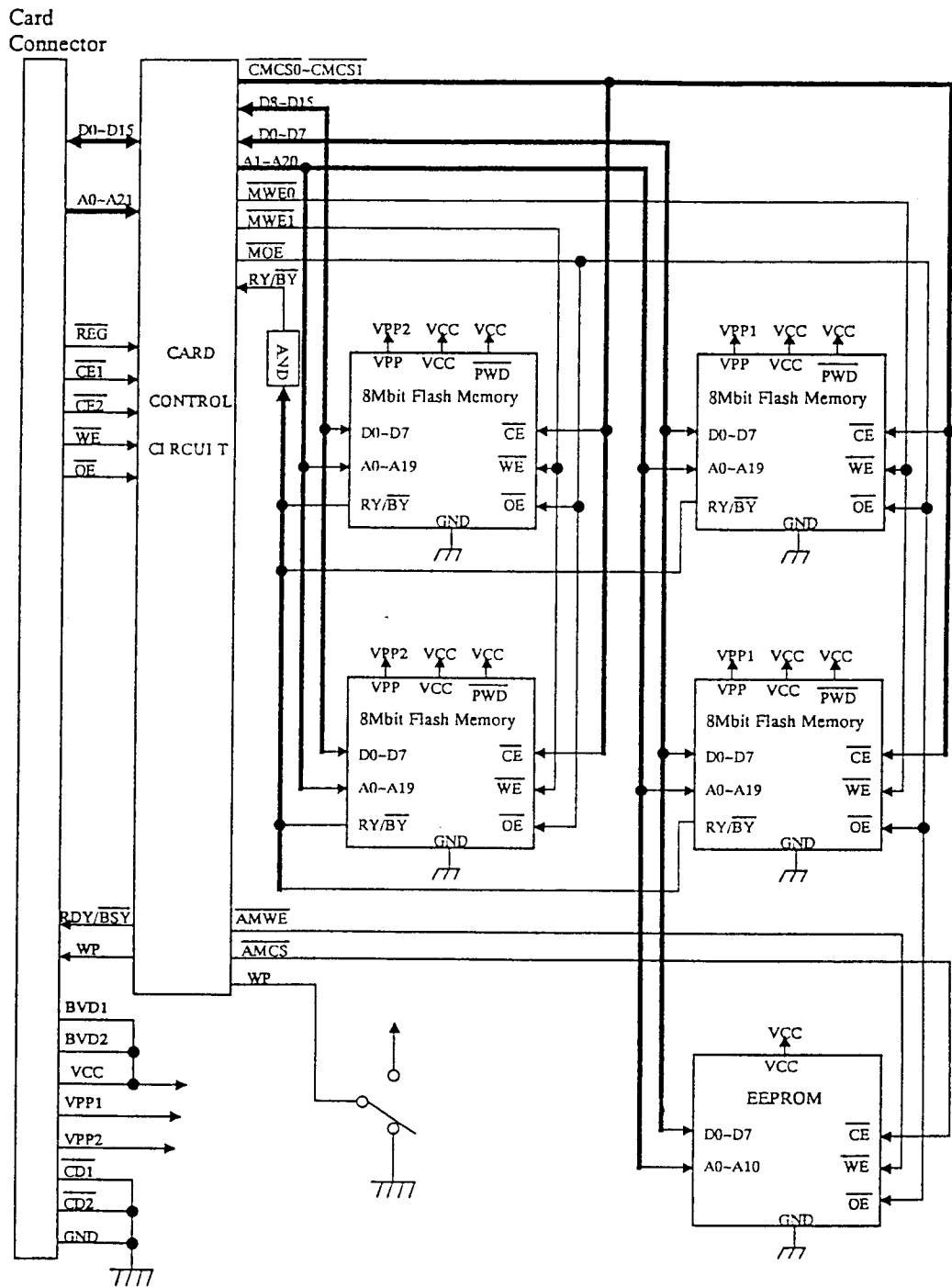
1. General Descriptions

The SHARP ID244E01, which panel design is SHARP standard, is a 4MB Flash Memory PC Card conforms to PCMCIA Release 2.0 and is offered to customers giving aim to confirm an external shape or electrical performances of the card. Before mass production, we will create a new product name dedicated for a customer and also present a specification which implies customer's request including panel design.

2. Features

- | | | |
|------|---|--|
| 2.1 | Type | 4MB Flash Memory Card
(Conforms to PCMCIA Rel. 2.0) |
| 2.2 | Memory Capacity | |
| | Common Memory | 4M words×8 bits or 2M words×16 bits |
| | Attribute Memory | EEPROM Model 2k words×8 bits read/write |
| | Note) We have another type of attribute memory as follows,
No EEPROM Model. (5 words×8 bits read only in card's control circuit)
Sample card name: ID244E02. Customers can choose one model from two. | |
| 2.3 | Supply Voltage | |
| | Read Cycle | Vcc=5±0.5V, Vpp1, Vpp2=0~1.5V |
| | Read/Program/Erase Cycle | Vcc=5±0.5V, Vpp1, Vpp2=5.0V±0.5V/12.0V±0.6V |
| 2.4 | Erase Unit | Block(64k bytes/byte access, 128k bytes/word access) |
| 2.5 | Program/Erase Cycles | 100,000 cycles |
| 2.6 | Interface | Parallel I/O Interface |
| 2.7 | Function Table | See Function Table in page. 6 |
| 2.8 | External Dimensions | 54×85.6×3.3 mm |
| 2.9 | Pin Connections | See Pin Connections in page. 4 |
| 2.10 | Type of Connector | Conforms to PCMCIA Rel. 2.0 Card Use Connector
(Card connector: JC20-J68S-NB3 JAE or
FCN-568J068-G/0 Fujitsu) |
| 2.11 | Average Weight | 30g |
| 2.12 | Operating Temp Range | 0 to 60°C |
| 2.13 | Storage Temp Range | -20 to 65°C |
| 2.14 | External Appearance | External appearance shall be free of any dirt,
cratches and abnormalities that could adversely
affect sales. |
| 2.15 | Manufacturer's Code | The manufacturer's code shall be printed on the
memory card directly or on the seal which is then
attached to the memory card. |
| 2.16 | Brand Name | The user's brand name will be used. |
| 2.17 | Not designed or rated radiation hardened. | |

3. Block Diagram



4. Pin Connections

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	18	V _{pp1}	35	GND	52	V _{pp2}
2	D3	19	A16	36	CD1	53	A22 (NC)
3	D4	20	A15	37	D11	54	A23 (NC)
4	D5	21	A12	38	D12	55	A24 (NC)
5	D6	22	A7	39	D13	56	A25 (NC)
6	D7	23	A6	40	D14	57	NC
7	CE1	24	A5	41	D15	58	NC
8	A10	25	A4	42	CE2	59	NC
9	OE	26	A3	43	NC	60	NC
10	A11	27	A2	44	NC	61	REG
11	A9	28	A1	45	NC	62	BVD2
12	A8	29	A0	46	A17	63	BVD1
13	A13	30	D0	47	A18	64	D8
14	A14	31	D1	48	A19	65	D9
15	WE / PGM	32	D2	49	A20	66	D10
16	RDY/ BSY	33	WP	50	A21	67	CD2
17	Vcc	34	GND	51	Vcc	68	GND

Pin Descriptions:

D0~D7	Data Bus (Input/Output)
D8~D15	Data Bus (Input/Output)
A0~A21	Address Bus (Input)
CE1, CE2	Card Enable (Input)
OE	Output Enable (Input)
WE/PGM	Write Enable/Program (Input)
CD1, CD2	Card Detect (Output)(Card Inserted Detection Signal)
WP	Write Protect (Output)(in write protect mode, the WP output signal is "HIGH")
Vpp1	Program/Erase Power Supply(Even Byte)
Vpp2	Program/Erase Power Supply(Odd Byte)
REG	Register Select (Input)
BVD1, BVD2	Battery Voltage Detect(Always "HIGH")
RDY/BSY	Ready/Busy (Output)

Notes: Pin 53: Address bit 22, Pin 54 Address bit 23, Pin 55: Address bit 24 and Pin 56: Address bit 25 are no connection.

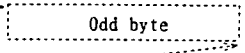
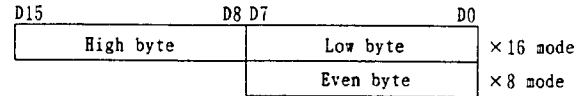
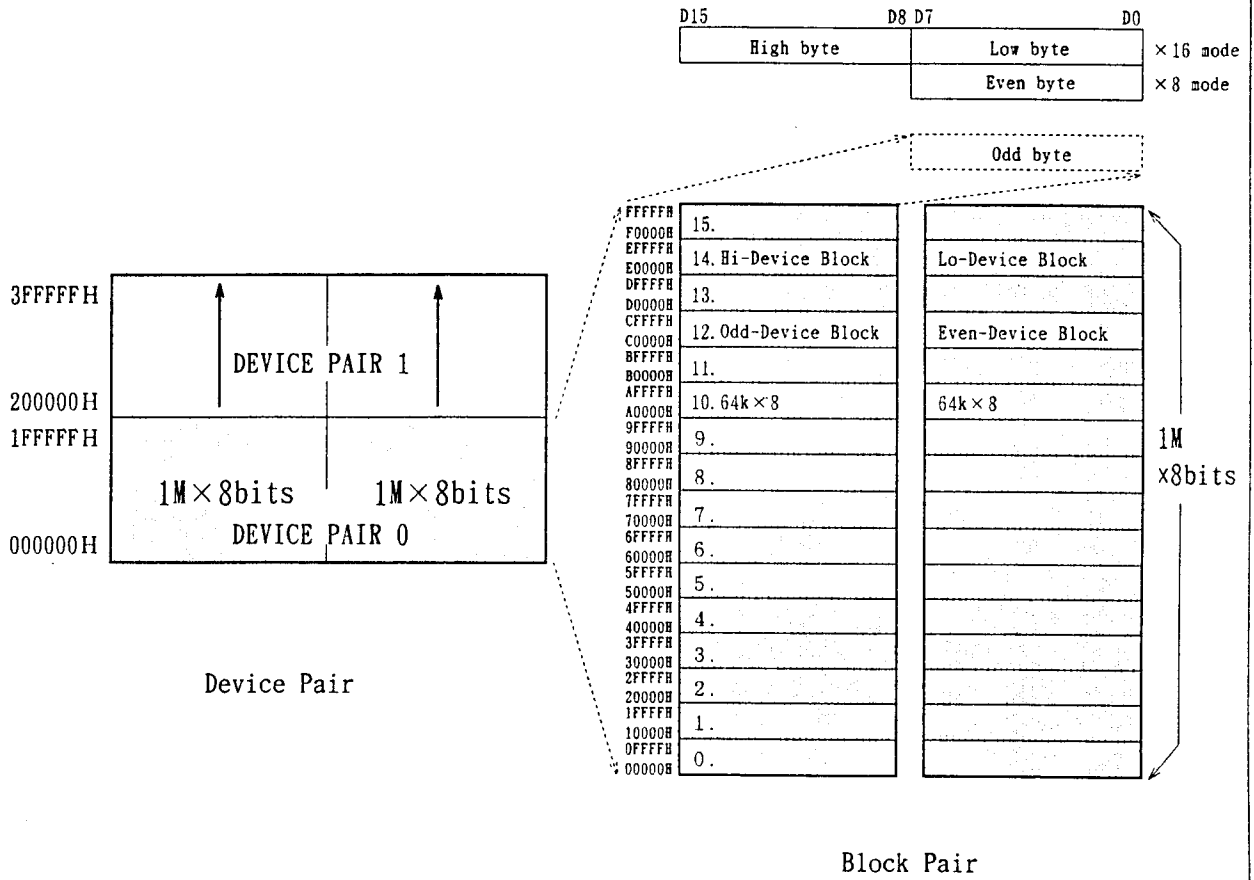
5. Function

5.1 Memory Block

5.1.1 Memory Configuration 8Mbits Flash Memory x 4 Devices.

5.1.2 Memory Erase Unit Block Erase

Block : Byte Mode 64k bytes
Word Mode 128k bytes



5.2 Function Table

$\overline{CE1}$	$\overline{CE2}$	A0	\overline{WE}	\overline{OE}	\overline{REG}	Vpp1	Vpp2	Vcc	Operation	D0-D7	D8-D15	Status
H	H	×	×	×	H	VppL	VppL	Vcc		Hi-Z	Hi-Z	Standby
L	H	L	H	L	H	VppL	VppL	Vcc	Read(x8)	Do(Even)	Hi-Z	Byte
L	H	H	H	L	H	VppL	VppL	Vcc	Read(x8)	Do(Odd)	Hi-Z	Byte
L	L	×	H	L	H	VppL	VppL	Vcc	Read(x16)	Do(Even)	Do(Odd)	Word
H	L	×	H	L	H	VppL	VppL	Vcc	Read(x8)	Hi-Z	Do(Odd)	Byte
L	×	×	×	H	H	VppL	VppL	Vcc	Output Disable	Hi-Z	Hi-Z	Byte
H	L	×	×	H	H	VppL	VppL	Vcc	Output Disable	Hi-Z	Hi-Z	Byte
L	H	L	L	H	H	VppH	VppX	Vcc	Program(x8)	Di(Even)	Don't care	Byte
L	H	H	L	H	H	VppX	VppH	Vcc	Program(x8)	Di(Odd)	Don't care	Byte
L	L	×	L	H	H	VppH	VppH	Vcc	Program(x16)	Di(Even)	Di(Odd)	Word
H	L	×	L	H	H	VppX	VppH	Vcc	Program(x8)	Don't care	Di(Odd)	Byte
L	H	L	H	L	H	VppH	VppX	Vcc	Verify(x8)	Do(Even)	Hi-Z	Byte
L	H	H	H	L	H	VppX	VppH	Vcc	Verify(x8)	Do(Odd)	Hi-Z	Byte
L	L	×	H	L	H	VppH	VppH	Vcc	Verify(x16)	Do(Even)	Do(Odd)	Word
H	L	×	H	L	H	VppX	VppH	Vcc	Verify(x8)	Hi-Z	Do(Odd)	Byte
L	H	H	L	L	H	VppH	VppX	Vcc	*1 Prohibited	——	——	——
L	H	L	L	L	H	VppX	VppH	Vcc	*1 Prohibited	——	——	——
L	L	×	L	L	H	VppH	VppH	Vcc	*1 Prohibited	——	——	——
H	L	×	L	L	H	VppX	VppH	Vcc	*1 Prohibited	——	——	——

*1. Do not use this mode as it will result in write errors.

H : High L : Low × : Don't care
 Di : Input Data Do : Output Data Hi-Z : High Impedance
 Vcc : 4.5 ~ 5.5 V VppL : 0.0 ~ 1.5 V VppH : 4.5~5.5V/11.4~12.6V
 VppX : VppL or VppH

Caution: When the write protect switch is in protect-mode, the WP signal is "HIGH" and write operation are not allowed.

5.3 Software Command(8/16 Bits Operation ():16 Bits Operation)

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle			
		Operation	Address	Data	Operation	Address	Data Input	Data Output
Read Array /Reset	1	Write	R A	FFH/ (FFFFH)	—	—	—	—
Read Intelligent Identifier	3	Write	D A	90H/ (9090H)	Read	I A	—	I I D
Read Status Register	2	Write	D A	70H/ (7070H)	Read	D A	—	S R D
Clear Status Register	1	Write	D A	50H/ (5050H)	—	—	—	—
Erase Setup /Erase Confirm	2	Write	B A	20H/ (2020H)	Write	B A	D0H/ (D0D0H)	—
Erase Suspend/ Erase Resume	2	Write	B A	B0H/ (B0B0H)	Write	B A	D0H/ (D0D0H)	—
Byte Write Setup/Write	2	Write	W A	40H/ (4040H)	Write	W A	W D	—
Alternate Byte Write Setup/Write	2	Write	W A	10H/ (1010H)	Write	W A	W D	—

- Note) 1. This Table shows the basic form of Erase, Verify and Program Verify.
Refer Programming Flowchart, Erase Algorithm in detail.
2. Bus operations are defined in function table in page.
3. I A : Device Identifier Address I I D : Device Identifier Data

	D A	I A			I I D	
		8Bits (Even Device)	8Bits (Odd Device)	16Bits	Byte (8Bits)	Word (16Bits)
Manufacturer Code	000000H~1FFFFFFH	000000H	000001H	000000H	89H	8989H
Device Code	000000H~1FFFFFFH	000002H	000003H	000001H	A6H	A6A6H

R A : Read Address W A : Write Address W D : Write Data
D A : Device Address (Any Address in device is acceptable.)
B A : Erase Block Address (Erase Size is 64k Bytes.)
S R D : Status Register Data

4. Either 40H(4040H) or 10H(1010H) are recognized by the WSM as the Byte Write Setup Command.

- a) Read Array/Reset Command:(FFH/FFFFH)
By writing this command, device/devices pair become read mode. The device remains enable for reads until the Command User Interface contents are altered.
- b) Intelligent Identifier Command:(90H/9090H):
After writing this command into the Command User Interface, a read cycle retrieves the manufacturer Code and device Code. To terminate the Operation, it is necessary to write another valid command into the register.
- c) Read Status Register Command:(70H/7070H):
By Writing this command, the Status Register may be read at any time to determine when a byte or block erase operation is complete, and whether that operation completed successfully. Refer to Status Register definition in page. 9 .After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface.
- d) Clear Status Register Command:(50H/5050H)
Status bits which show error, the Erase Status(SR. 5), Byte Write Status(SR. 4) bits and the Vpp Status bit(SR. 3) can be reset by the Clear Status Machine Register Command.
- e) Erase Setup/Erase Command:(20H/2020H)/(D0H/D0D0H):
Erase is executed one block(64kB for 1 device, 128kB for 2 devices) at a time.
This command is functional when Vpp=VppH and an Erase Setup Command is first written to the Command User Interface, followed by the Erase Confirm Command. After that, the device automatically outputs Status Register data when read. The CPU can detect the completion of the erase event by analyzing the output of the RDY/BSY pin, or the WSM Status bit of the Status Register. When erase is completed, the Erase Status bit should be checked.
If erase error is detected, the Status Register should be cleared.
- f) Erase Suspend/Erase Resume Command:(B0H/B0B0H)/(D0H/D0D0H)
The Erase Suspend command allows block erase interruption in order to read data from another block of memory. The device continues to output Status Register data when read, after the Erase Suspend Command is written. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended. RDY/BSY pin will also transition to V_{OH}. At this point, a Read Array Command can be written to the Command User Interface to read data from blocks other than that which is suspended. Vpp must remain at VppH while device is in Erase Suspend. Erase Resume Command , at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and RDY/BSY pin will return to V_{OL}. After the Erase Resume is written, the device automatically output Status Register data when read.
- g) Byte Write Setup/Write Command:(40H/4040H) or (10H/1010H)
This command is functional when Vpp=VppH and an Byte Write Setup Command is first written to the Command User Interface, followed by a second write specifying the address and data to be written. The WSM then take over, controlling the byte write and write verify algorithms internally. After the two command byte sequence is written to it, the device automatically outputs Status Register data when read. The CPU can detect the completion of the byte write event by analyzing the output of the RDY/BSY pin , or the WSM Status bits of the Status Register.

5.4 Status Register

The memory devices in this card have Status Register which shows state of the device.

Byte Access x8 Bits

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0
WSMS	ESS	ES	BWS	VPPS	RFU	RFU	RFU

Register	Contents
SR. 7=Write State Machine Status 1=Ready 0=Busy	When set "1"s, read, erase, data write is acceptable.
SR. 6=Eraser Suspend Status 1=Eraser Suspend 0=Eraser In Progress/Completed	Check whether Eraser Suspend Command is executed or not.
SR. 5=Eraser Status 1=Error In Block Eraser 0=Successful Block Eraser	Set "1"s when fail to Eraser. Reset by the Clear Status Register Command.
SR. 4=Byte Write Status 1=Error In Byte Write 0=Successful Byte Write	Set "1"s when fail to Byte write. Reset by the Clear Status Register Command.
SR. 3=Vpp Status 1=Vpp Low Detect;Operation Abort 0=Vpp OK	Set "1"s when Vpp, which is needed in Byte Write or Eraser operation, is below VppH. Reset by the Clear Status Register Command.
SR. 2~SR. 0=Reserved for Future Use	

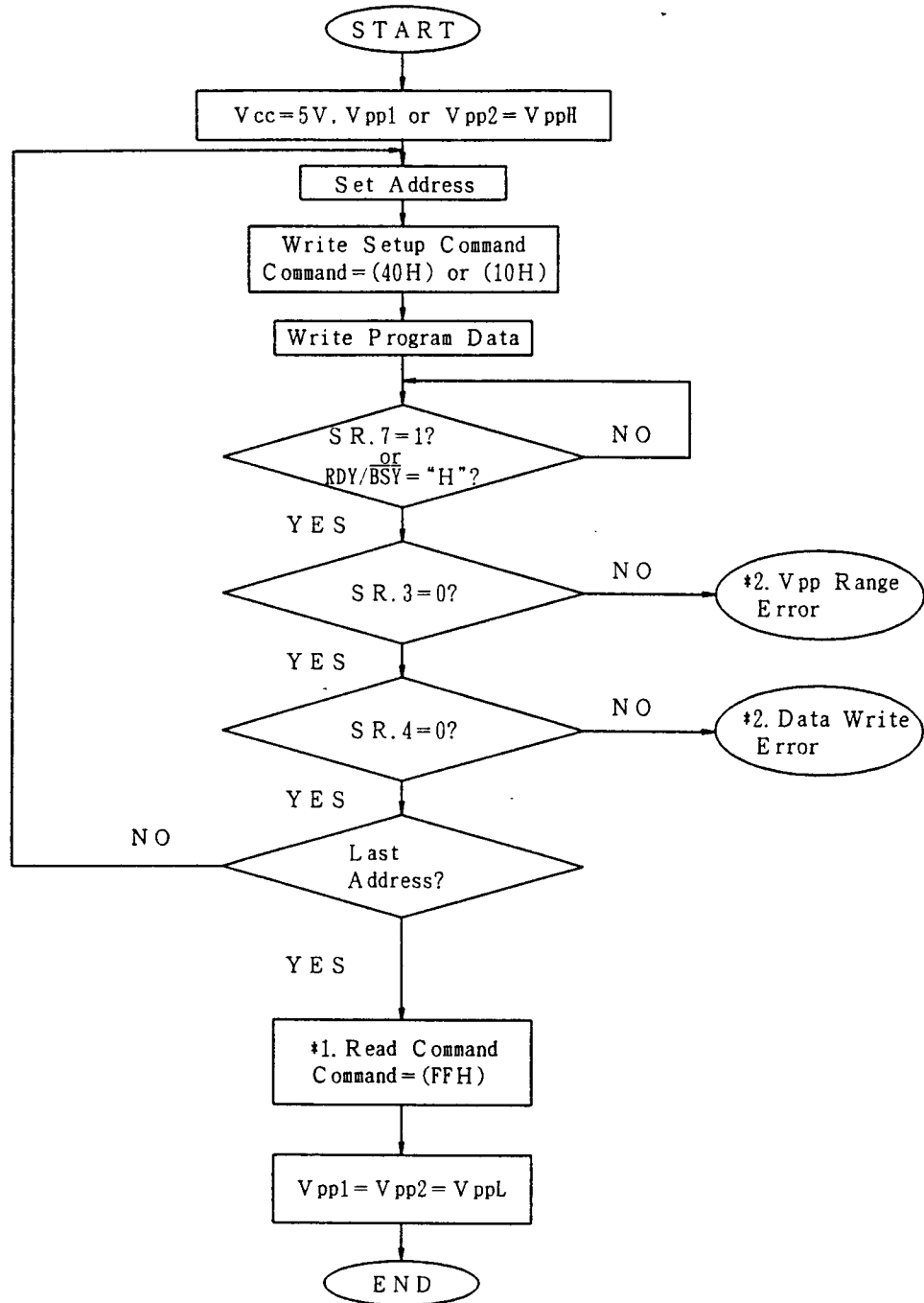
Word Access x16 bits

bit15						bit8 bit7						bit0			
SR. 15	SR. 14	SR. 13	SR. 12	SR. 11	SR. 10	SR. 9	SR. 8	SR. 7	SR. 6	SR. 5	SR. 4	SR. 3	SR. 2	SR. 1	SR. 0

Odd Byte device

Even Byte device

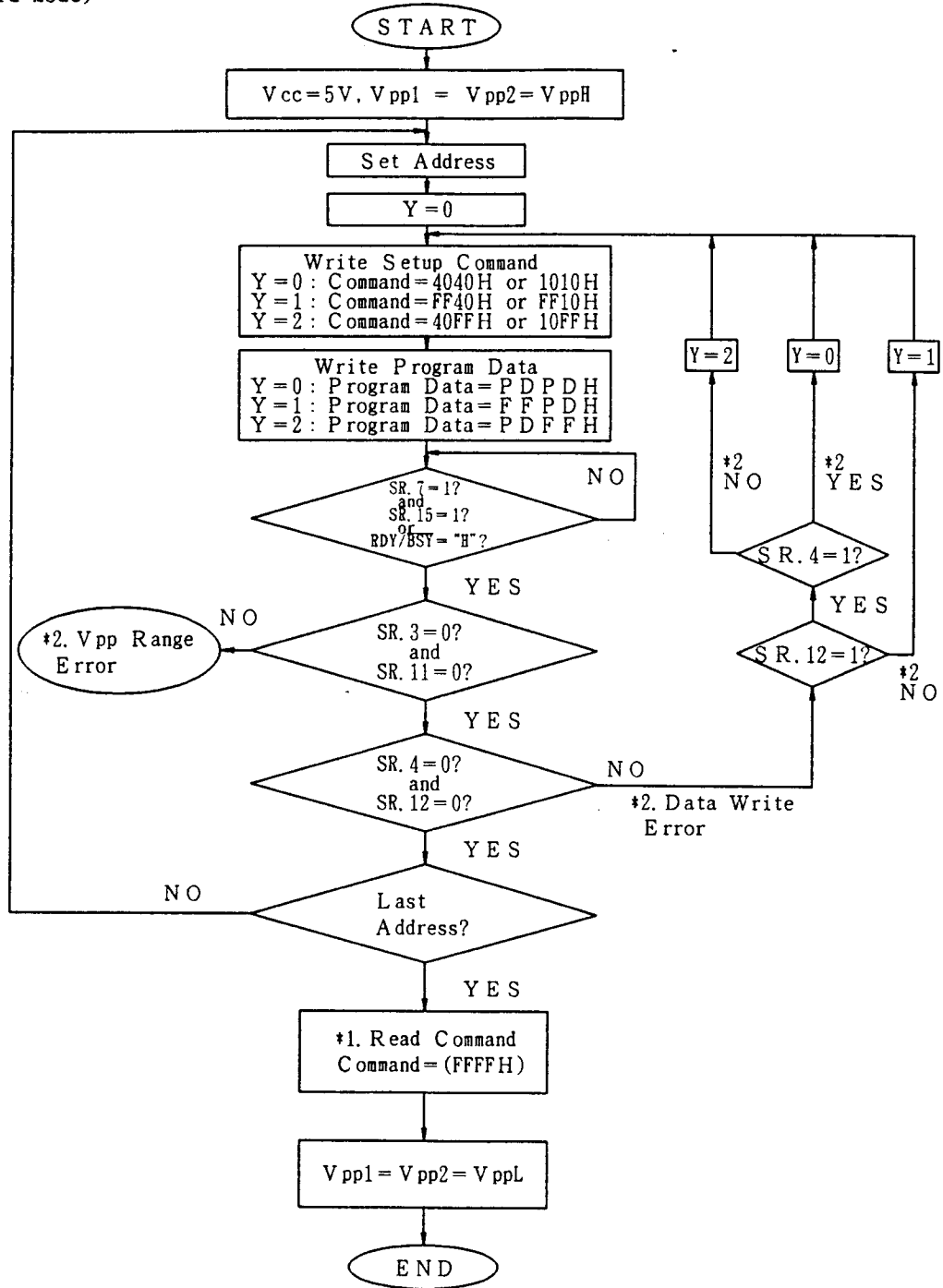
5.5 Programming Flowchart (Byte Mode)



Note) *1. Write FFH after the last block write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

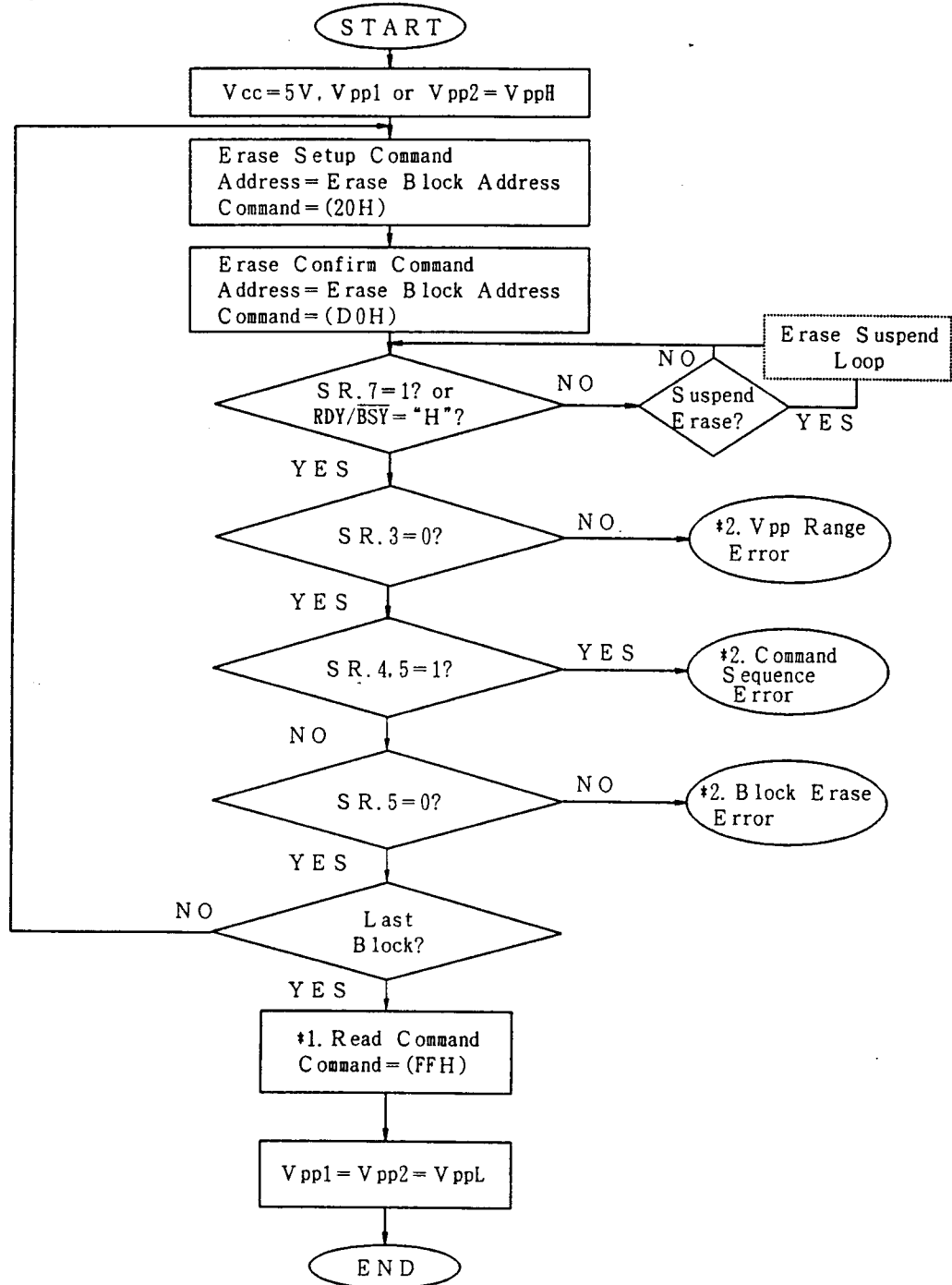
Programming Flowchart
(Word Mode)



Note) *1. Write FFFFH after the last block write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

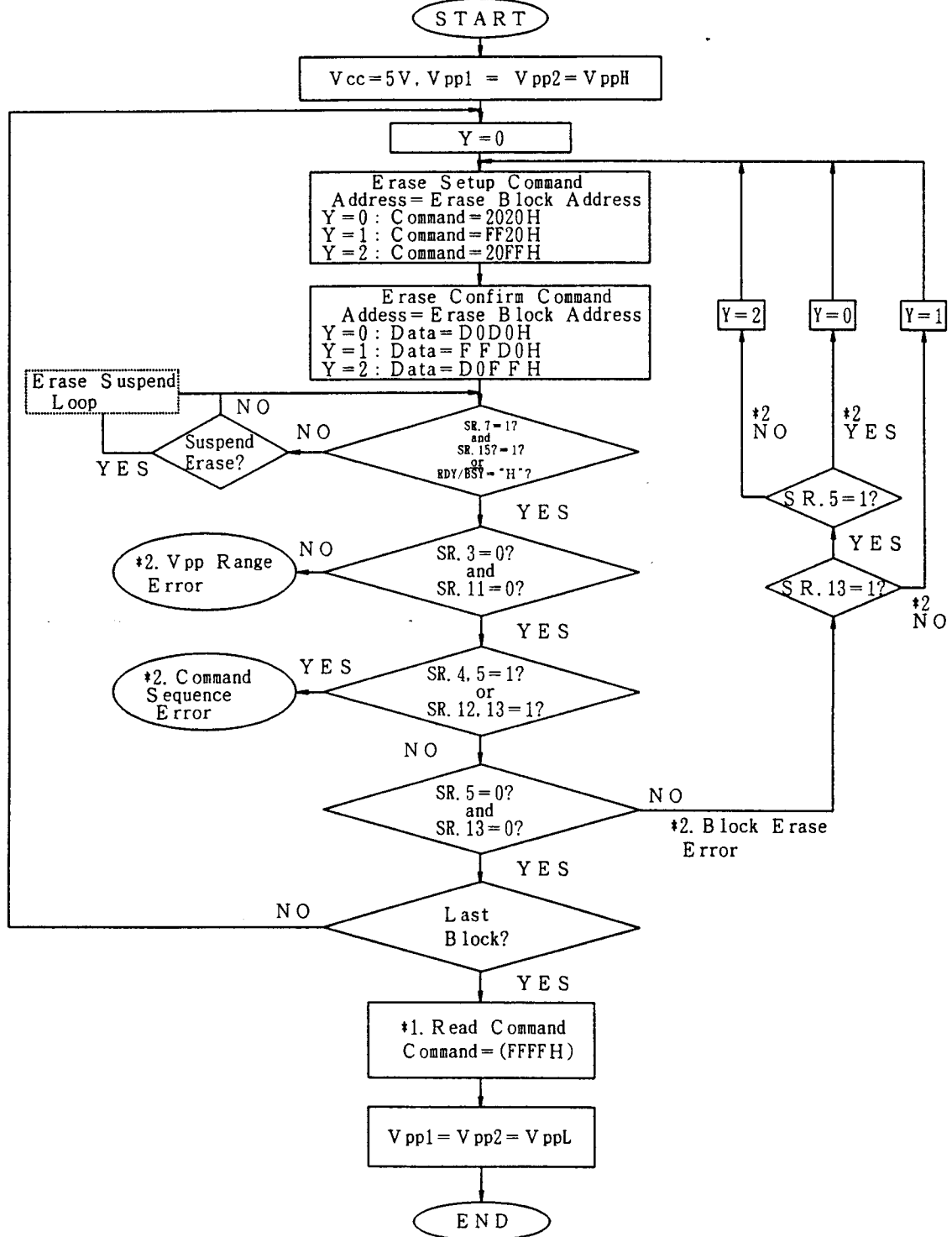
5.6 Erase Algorithm (Byte Mode)



Note) *1. Write FFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

Erase Algorithm (Word Mode)



Note) *1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

6. Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-0.3 to $V_{CC}+0.3$ (Max:7.0)	V
Output Voltage	V_{OUT}	-0.3 to $V_{CC}+0.3$ (Max:7.0)	V
Operating Temperature	T_{OPR}	0 to +60	°C
Storage Temperature	T_{STG}	-20 to +65	°C

7. Recommended Operating Conditions

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
Operating Temperature	T_{OPR}	0	+60	°C
Supply Voltage	V_{CC}	4.5	5.5	V
Input Voltage High	V_{IH}	3.5	$V_{CC}+0.3$	V
Input Voltage Low	V_{IL}	-0.3	1.5	V

8. Capacitance

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	—	17	—	pF	$V_{CC}=5V\pm 10\%$
Input/Output Capacitance	C_{IO}	—	17	—	pF	$f=1MHz, T_a=25^\circ C$

9. Read Operation

9.1 DC Characteristics

(V_{CC}=4.5~5.5V, Ta=0~60°C)

	PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
1	Operating Voltage	High Temperature	V _{CC}	4.50	—	5.50	V	
		Low Temperature						
*1 2	Current Consumption	Static Operatin Current	I _{SB}	—	—	2.0	mA	X16, Address :PingPong
		Dynamic Operating Current	I _{CC}	—	—	80		
3	Input Voltage	Input Voltage Level High	V _{IH}	3.5	—	V _{CC} +0.3	V	V _{CC} =4.5~5.5V
		Input Voltage Level Low	V _{IL}	-0.3	—	1.5		
4	Input Current	A0~A20, D0~D15	I _{LI}	-10	—	70	μA	V _I =V _{CC} , 0V
		CE1, CE2, OE, WE, REG		-70	—	10		
5	Output Voltage	High	V _{OH}	V _{CC} -0.5	—	—	V	I _{OH} =-2mA(*2) I _{OH} =-4μA(*3)
		Low	V _{OL}	—	—	0.4		I _{OL} =4mA

PingPong:Scan the target address, with accessing the target and another address alternately.

*1 (1) Static Operating Current:With the memory card's voltage at 5.5V and the CE1, CE2 OE, WE and REG signals "HIGH" (V_{IH}=V_{CC}-0.2V), A0 signal "LOW" (V_{IL}≤0.2V) the current consumption is measured with the output open.

(2) Dynamic Operating Current : With the memory card's V_{CC} at 5.5V and V_{pp1}=V_{pp2} at 12.6V, current consumption during access is measured with the output open.
(Access time: 200ns) The current depends on addressing.

*2 D0~D15

*3 BVD1, BVD2, RDY/BSY, WP

9.2 AC Characteristics (V_{CC}=4.5~5.5V, V_{pp}=0.0~1.5V, Ta=0~60°C)

Testing Conditions:

- 1) Input Pulse Level : 0.8~3.5V
- 2) Input Rise/Fall Time : 10ns
- 3) Input/Output Timing Reference Level : 1.5V
- 4) Output Load : 1TTL+C_L(100pF) (including scope and jig capacitance)

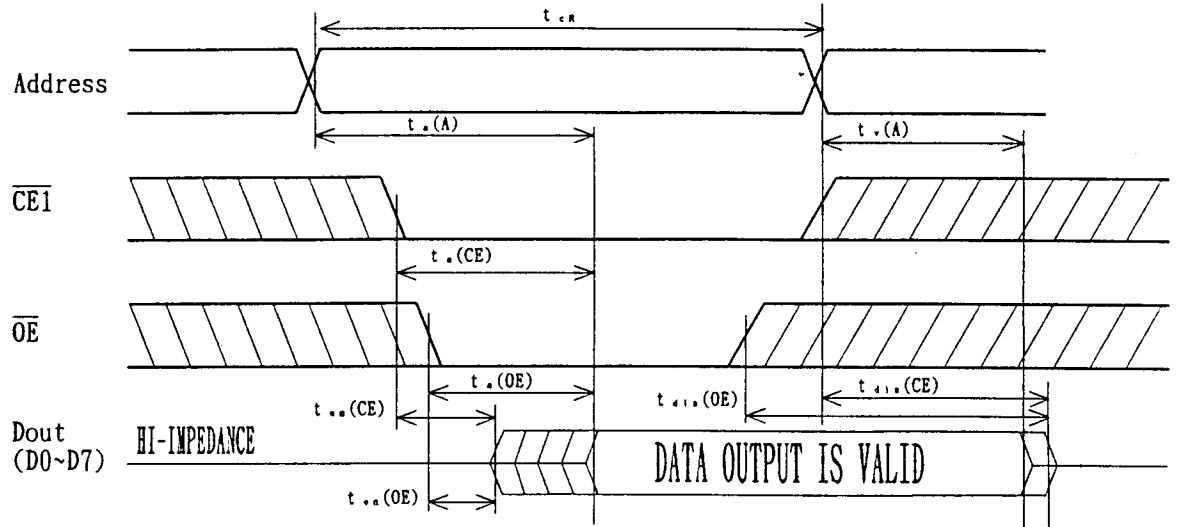
9.2.1 Read Cycle

(V_{CC}=4.5~5.5V, V_{pp}=0.0~1.5V, Ta=0~60°C)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Read Cycle Time	t _{AVAV}	t _{CR}	200	—	n s
Address Access Time	t _{AVQV}	t _a (A)	—	200	
Card Enable Access Time	t _{ELQV}	t _a (CE)	—	200	
Output Enable Access Time	t _{GLQV}	t _a (OE)	—	100	
Output Disable Time from CE*	t _{EHQV}	t _{di} (CE)	—	90	
Output Disable Time from OE*	t _{GHQZ}	t _{di} (OE)	—	90	
Output Enable Time from CE	t _{ELQX}	t _{en} (CE)	5	—	
Output Enable Time from OE	t _{GLQX}	t _{en} (OE)	5	—	
Data Valid from Add Change		t _v (A)	0	—	

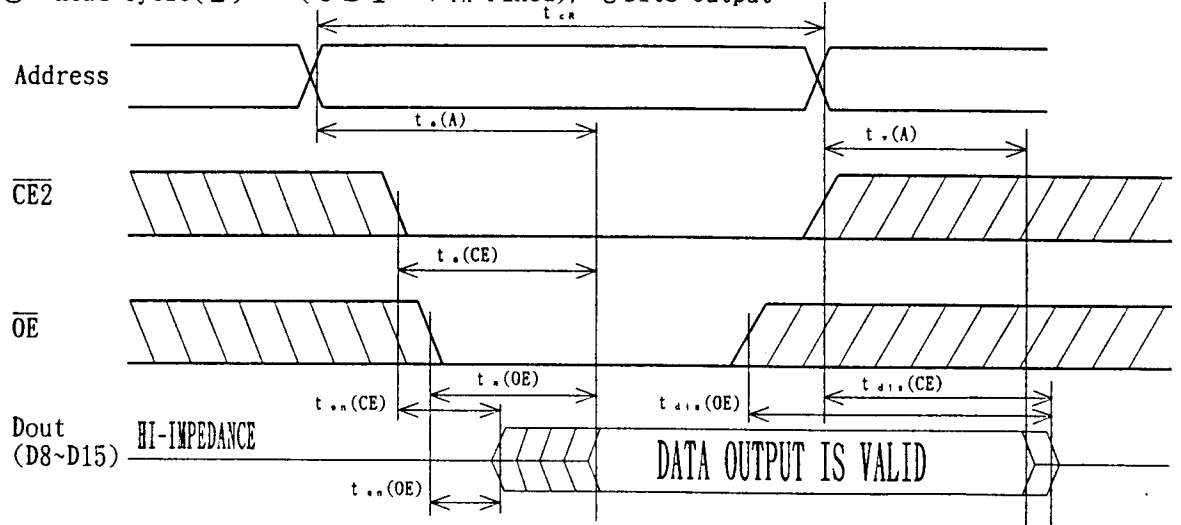
*Time until output becomes floating. (The output voltage is not defined.)

○ Read CYCLE(1) ($\overline{CE2} = V_{IH}$ Fixed), 8 Bits Output



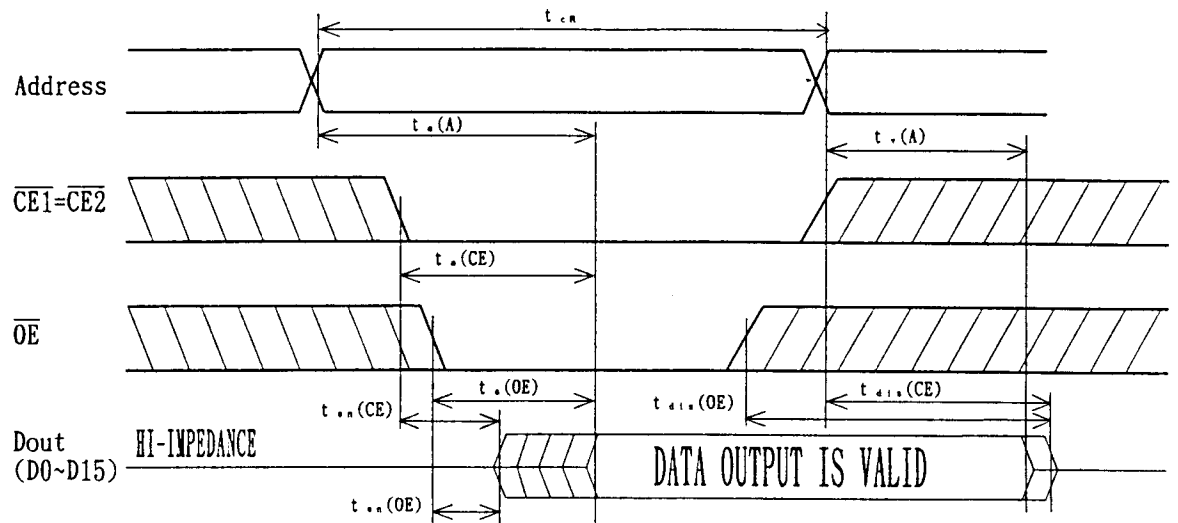
- Note) 1. \overline{WE} ="HIGH", during a read cycle.
 2. Either "HIGH" or "LOW" in diagonal areas.
 3. The output data becomes valid when last interval, $t_{a(A)}$, $t_{a(CE)}$ or $t_{a(CE)}$ have concluded.

○ Read Cycle(2) ($\overline{CE1} = V_{IH}$ Fixed), 8 Bits Output



- Note) 1. \overline{WE} ="HIGH", during a read cycle.
 2. Either "HIGH" or "LOW" in diagonal areas.
 3. The output data becomes valid when last interval, $t_{a(A)}$, $t_{a(CE)}$ or $t_{a(CE)}$ have concluded.

○ Read Cycle (3), 16 Bits Output



- Note) 1. \overline{WE} ="HIGH", during a read cycle.
 2. Either "HIGH" or "LOW" in diagonal areas.
 3. Change CE1 and CE2 at the same time.
 4. The output data becomes valid when last interval, $t_a(A)$, $t_a(CE)$ or $t_a(OE)$ have concluded.

10. Programming Operation
 10.1 DC Characteristics

($V_{CC}=4.5\sim 5.5V$, $V_{PP}=4.5\sim 5.5V/11.4\sim 12.6V$, $T_a=0\sim 60^\circ C$)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION	
Vpp1, Vpp2 operating Voltage	Read	V_{PPL}	0	1.5	V	
	Program	V_{PPH}	4.5	5.5		Vpp=4.5~5.5V
			11.4	12.6		Vpp=11.4~12.6V
Vpp1, Vpp2 operating Current (X16 Mode)	Read	I_{SB2}	-	1.6	mA	
	Program	I_{PP}	-	45		RMS Vpp=4.5~5.5V
			-	20		Vpp=11.4~12.6V
Vcc operating Current	Standby	I_{SB1}	-	2	Input open	
	Program	I_{CC}	-	75	RMS X16 Mode	
Input Voltage	V_{IL}	-0.3	1.5	V		
	V_{IH}	3.5	$V_{CC}+0.3$			
Output Voltage During Verify	V_{OL}	-	0.4	V	$I_{OL}=4mA$	
	V_{OH}	$V_{CC}-0.5$	-		$I_{OH}=-2mA$	

- Note) 1. Power on Vcc before power on Vpp, power off Vcc after power off Vpp.
 2. Keep Vpp including its overshoot, below 13V.
 3. Card insertion or removal while applying Vpp=12V may cause a loss of integrity.
 4. Do not turn on or turn off during \overline{CE} ="LOW".
 5. If V_{IH} goes above $V_{CC}+0.3V$, normal operation is not assured.

10.2 A C Characteristics (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60°C)

Testing Conditions:

- 1) Input Pulse Level : 0.8~3.5V
 2) Input Rise/Fall Time : 10ns
 3) Input/Output Timing Reference Level : 1.5V
 4) Output Load : 1TTL+CL(100pF) (including scope and jig capacitance)

10.2.1 Program Cycle

WE Controlled

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60°C)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time	t _{AVAV}	t _{cw}	200	—	n s
Address Setup Time	t _{AVWL}	t _{su(A)}	20	—	
Write Recovery Time	t _{WHAX}	t _{rec(WE)}	30	—	
Data Setup Time for WE	t _{DVWH}	t _{su(D-WEH)}	60	—	
Data Hold Time	t _{WHDX}	t _{h(D)}	30	—	
Write Recovery Before Read	t _{WHGL}		10	—	
Card Enable Setup time for WE	t _{ELWH}	t _{su(CE-WEH)}	140	—	
Address Setup for WE	t _{AVWH}	t _{su(A-WEH)}	140	—	
Card Enable Hold Time	t _{WHEH}		15	—	
Write Pulse Width	t _{WLWH}	t _{w(WE)}	120	—	
Write Pulse Width High	t _{WHWL}	t _{w(WEH)}	30	—	
WE High to RDY/BSY Going Low	t _{WHRL}		—	150	
Duration of write operation	Vpp=4.5~5.5V Vpp=11.4~12.6V	t _{WHQV1}	6.5	—	
			4.8	—	
Vpp Setup to WE Going High	t _{VPWH}		100	—	n s
Vpp Hold from Valid SRD, RDY/BSY High	t _{QVVL}		0	—	

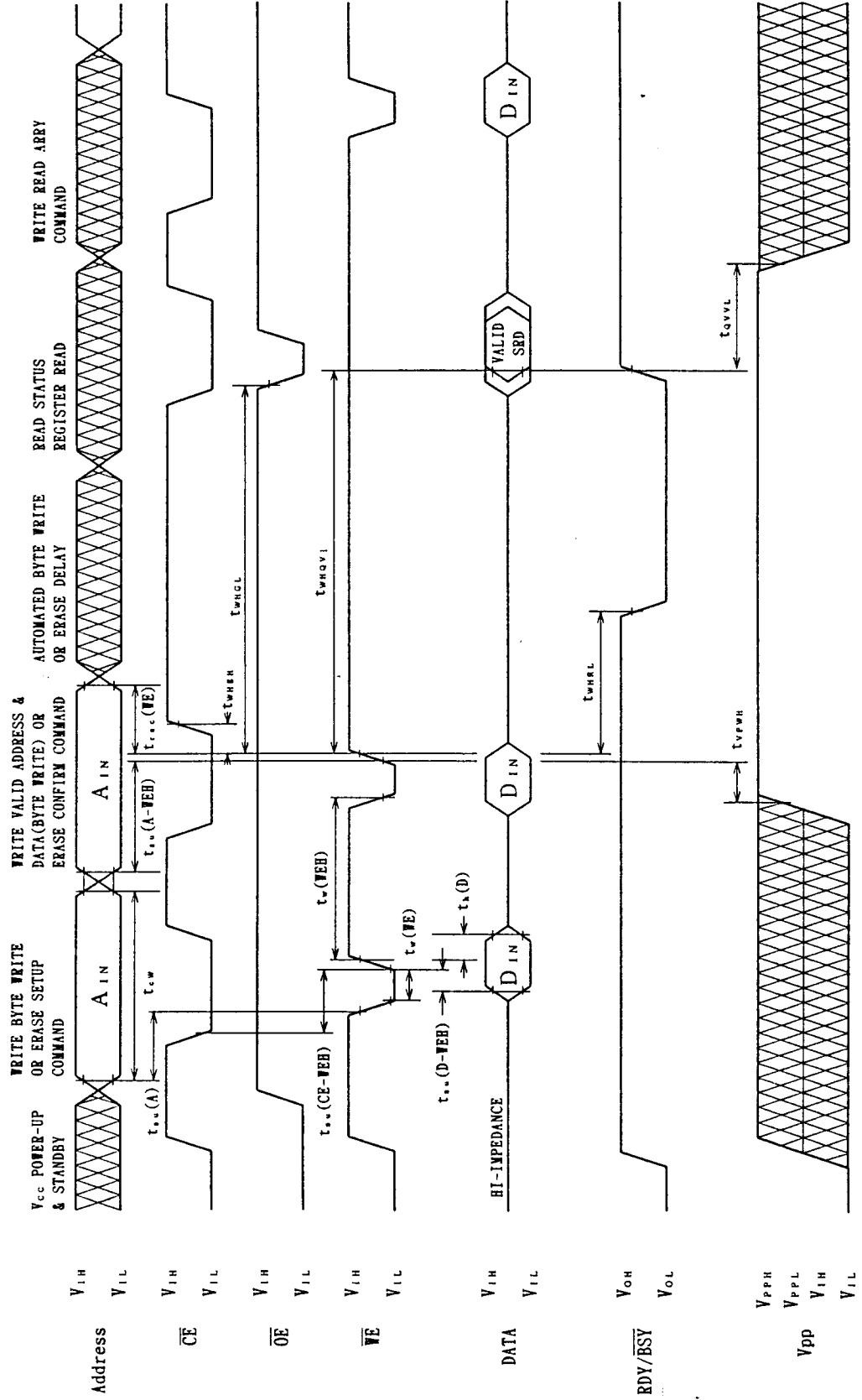
CE Controlled

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60°C)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time	t _{AVAV}	t _{cw}	200	—	n s
Address Setup Time	t _{AVEL}	t _{su(A)}	20	—	
Write Recovery Time	t _{EHAX}	t _{rec(CE)}	30	—	
Data Setup Time for CE	t _{DVEH}	t _{su(D-CEH)}	60	—	
Data Hold Time	t _{EHDX}	t _{h(D)}	30	—	
Write Recovery Before Read	t _{EHGL}		10	—	
Write Enable Setup time for CE	t _{WLEH}	t _{su(WE-CEH)}	140	—	
Address Setup for CE	t _{AVEH}	t _{su(A-CEH)}	140	—	
Write Enable Hold Time	t _{EHWL}		0	—	
Write Pulse Width	t _{ELEH}	t _{w(CE)}	120	—	
Write Pulse Width High	t _{EHEL}	t _{w(CEH)}	30	—	
WE High to RDY/BSY Going Low	t _{EHRL}		—	150	
Duration of write operation	Vpp=4.5~5.5V Vpp=11.4~12.6V	t _{EHQV1}	6.5	—	
			4.8	—	
Vpp Setup to WE Going High	t _{VP EH}		100	—	n s
Vpp Hold from Valid SRD, RDY/BSY High	t _{QVVL}		0	—	

1. Set CE1, CE2, OE and WE "HIGH", when Vpp changes from VppL to VppH or vice versa.

○ Program Cycle (\overline{WE} Controlled)



Note) While the data signal is in output mode, do not apply an opposite phase signal.

11. Erase Operation

11.1 D C Characteristics

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION	
Vpp1, Vpp2 Operating Voltage	Read	V _{PPL}	0	1.5	V	
	Program	V _{PPHE}	4.5	5.5		Vpp=4.5~5.5V
			11.4	12.6		Vpp=11.4~12.6V
Vpp1, Vpp2 Operating Current (X16 Mode)	Standby	I _{SB2}	—	1.6	mA	
	Erase	I _{PP}	—	45		RMS Vpp=4.5~5.5V
			—	20		Vpp=11.4~12.6V
	Erase Suspend	I _{PPS}	—	1.6		CE1, CE2=V _{IH} , RMS
Vcc Operating Current (X16 Mode)	Standby	I _{SB1}	—	2.0	V	
	Erase	I _{CCE}	—	75		RMS
	Erase Suspend	I _{CCEs}	—	22		CE1, CE2=V _{IH} , RMS
Input Voltage	V _{IL}	-0.3	1.5	V		
	V _{IH}	3.5	Vcc+0.3			
Output Voltage During Verify	V _{OL}	—	0.4	V	I _{OL} =4mA	
	V _{OH}	Vcc-0.5	—		I _{OH} =-2mA	

Note) Power on Vcc before power on Vpp, power off Vcc after power off Vpp. Keep Vpp including its overshoot, below 13V. Card insertion or removal while applying Vpp=12V may cause a loss of integrity. Do not turn on or turn off during CE="LOW". If V_{IH} goes above Vcc+0.3V, normal operation is not assured.

11.2 A C Characteristics (Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60°C)

Testing Conditions:

- 1) Input Pulse Level : 0.8~3.5V
- 2) Input Rise/Fall Time : 10ns
- 3) Input/Output Timing Reference Level : 1.5V
- 4) Output Load : 1TTL+C_L(100pF) (including scope and jig capacitance)

11.2.1 Erase Cycle

WE Controlled

(Vcc=4.5~5.5V, Vpp=4.5~5.5V/11.4~12.6V, Ta=0~60°C)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time	t _{AVAV}	t _{cw}	200	—	ns
Address Setup Time	t _{AVWL}	t _{su(A)}	20	—	
Write Recovery Time	t _{WHAX}	t _{rec(WE)}	30	—	
Data Setup Time for WE	t _{DVWH}	t _{su(D-WEH)}	60	—	
Data Hold Time	t _{WHDx}	t _{h(D)}	30	—	
Write Recovery Before Read	t _{WHGL}		10	—	
Card Enable Setup time for WE	t _{ELWH}	t _{su(CE-WEH)}	140	—	
Address Setup for WE	t _{AVWH}	t _{su(A-WEH)}	140	—	
Card Enable Hold Time	t _{WHEH}		15	—	
Write Pulse Width	t _{WLWH}	t _{w(WE)}	120	—	
Write Pulse Width High	t _{WHWL}	t _{w(WEH)}	30	—	
WE High to RDY/BSY Going Low	t _{WHRL}		—	150	
Duration of Erase operation	Vpp=4.5~5.5V	t _{WHQV2}	0.9	—	
	Vpp=11.4~12.6V		0.3	—	
Vpp Setup to WE Going High	t _{VPWH}		100	—	ns
Vpp Hold from Valid SRD, RDY/BSY High	t _{QVVL}		0	—	

$\overline{C E}$ Controlled(V_{CC}=4.5~5.5V, V_{PP}=4.5~5.5V/11.4~12.6V, T_a=0~60°C)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time	t _{AVAV}	t _{cw}	200	—	n s
Address Setup Time	t _{AVEL}	t _{su(A)}	20	—	
Write Recovery Time	t _{EHAX}	t _{rec(CE)}	30	—	
Data Setup Time for CE	t _{DVEH}	t _{su(D-CEH)}	60	—	
Data Hold Time	t _{EHDX}	t _{h(D)}	30	—	
Write Recovery Before Read	t _{EHGL}		10	—	
Write Enable Setup time for CE	t _{WLEH}	t _{su(WE-CEH)}	140	—	
Address Setup for CE	t _{AVEH}	t _{su(A-CEH)}	140	—	
Write Enable Hold Time	t _{EHWH}		0	—	
Write Pulse Width	t _{ELEH}	t _{w(CE)}	120	—	
Write Pulse Width High	t _{EHEL}	t _{w(CEH)}	30	—	
\overline{WE} High to RDY/BSY Going Low	t _{EHRL}		—	150	
Duration of Erase operation	V _{pp} =4.5~5.5V	t _{EHQV2}	0.9	—	
	V _{pp} =11.4~12.6V		0.3	—	
V _{pp} Setup to \overline{WE} Going High	t _{VPEH}		100	—	n s
V _{pp} Hold from Valid SRD, RDY/BSY High	t _{QVVL}		0	—	

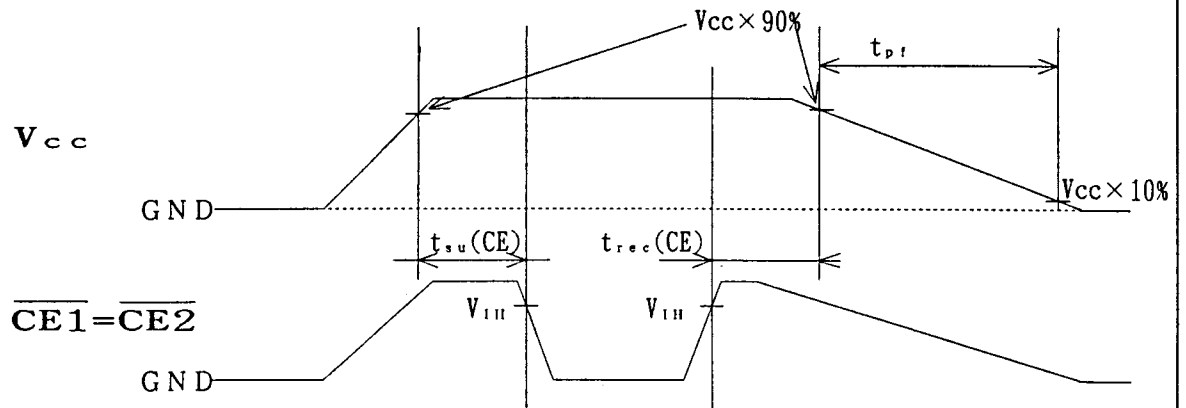
1. Set $\overline{CE1}$, $\overline{CE2}$, \overline{OE} and \overline{WE} "HIGH", when V_{pp} changes from PPr to PPH or vice versa.

12. Block Erase and Data Write Characteristics

($V_{cc}=4.5\sim 5.5V$, $V_{pp}=4.5\sim 5.5V/11.4\sim 12.6V$, $T_a=0\sim 60^\circ C$)

PARAMETER		MIN	TYP	MAX	UNIT
Block Pair Erase Time	$V_{pp}=4.5\sim 5.5V$	—	1.1	10	s
Block Pair Erase Time	$V_{pp}=11.4\sim 12.6V$	—	1.0	10	
Block Pair Write Time	$V_{pp}=4.5\sim 5.5V$	—	0.5	2.1	
Block Pair Write Time	$V_{pp}=11.4\sim 12.6V$	—	0.4	2.1	

13. Voltage Timing ($T_a = 25^\circ C$)



$$3.5V < V_{IH} < V_{cc} + 0.3$$

PARAMETER	SYMBOL	MIN	MAX	UNIT
CE Setup Time	$t_{s,u}(CE)$	4.0	—	ms
CE Recovery Time	$t_{r,e,c}(CE)$	1.0	—	μs
Vcc Falling Time	$t_{p,f}$	3.0	300	ms

Note)

- When $V_{cc}(4.5\sim 5.5V)$ is applied to the memory card and you are inserting or removing the card, $\overline{CE1}$, $\overline{CE2}$ should both be high-impedance. At such a time, other signal line should also be hi-impedance. After inserting the memory card, do not access it during the CE setup time (minimum of 4ms).
(During this time, neither $\overline{CE1}$ nor $\overline{CE2}$ ="LOW".)
- When V_{cc} is turn on, if the condition (for example, V_{cc} rising time, etc) is not sufficient to as specified, it is possible that device's Status Register is not cleared or device not becomes to Read Array Mode. To prevent these, it is recommended that using software command, reset the Status Register or set the device to Read Array Mode.

ex.

Reset the Status Register 50H(5050H)

Set to Read Array Mode FFH(FFFFH)

14. Attribute Memory

The attribute memory holds the attribute informations of the card such as the type of card, bit configuration, speed and so on.

EEPROM Model

Card has 2k bytes of EEPROM attribute memory. To read the attribute memory, set $\overline{\text{REG}} = \text{"LOW"}$ and perform a read with the same access timing as common memory read. For this operation, access time is 300ns maximum. To allow 2k bytes of attribute memory, even addresses from 0 to 4096 are reserved. Since only the even-numbered bytes are used, reading odd-numbered bytes will result in invalid data.

Note) We have another type of attribute memory as follows,

No EEPROM Model. (Model no. ID244E02: 5 bytes device informations in even address 0 to 8, read only in card's control circuit, with the same access timing as common memory read)

14.1 Attribute Memory Read/Write Function Chart

CE1	CE2	A0	WE	OE	REG	MODE	D ₀ ~D ₇	D ₈ ~D ₁₅	STATUS
H	H	X	X	X	X		High-Z	High-Z	Standby
L	H	L	H	L	L	Read (×8)	D ₀ (even byte)	High-Z	Byte Access
L	H	H	H	L	L		High-Z	High-Z	Standby
L	L	X	H	L	L	Read (×8)	D ₀ (even byte)	High-Z	Byte Access
H	L	X	H	L	L		High-Z	High-Z	Standby
L	H	L	L	H	L	Write (×8)	D ₁ (even byte)	xxx	Byte Access
L	H	H	L	H	L		xxx	xxx	Standby
L	L	X	L	H	L	Write (×8)	D ₁ (even byte)	xxx	Byte Access
H	L	X	L	H	L		xxx	xxx	Standby
L	X	X	H	L	L	Attribute Memory Address 0~8	D ₀	High-Z	Byte Access

H : High

L : Low

X : High/Low not applicable

D₁ : Input Data

D₀ : Output Data

High-Z : High Impedance

xxx : Don't Care

Notes:

- 1) When the write protect switch is in protect-mode, the WP output signal is "HIGH" and write operations (including attribute memory) are not allowed.
- 2) A0-A11 are attribute memory addresses. Addresses after A12 are not decoded, so care should be taken.

14.2 AC Characteristics (VCC=4.5V~5.5V, Ta=0~60°C)

Testing Conditions

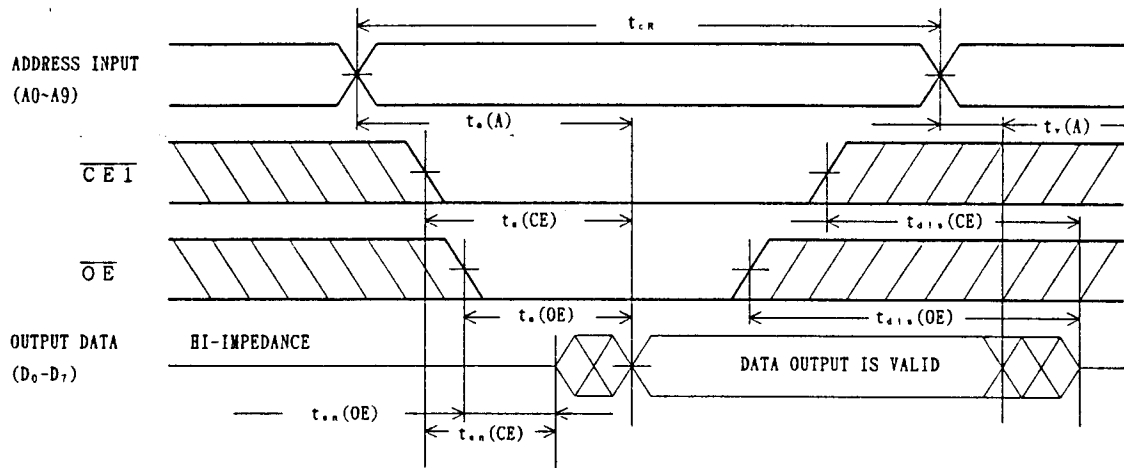
- 1) Input Pulse Level : 0.8~3.5V
- 2) Input Rise/Fall Time : 10ns
- 3) Input/Output Timing Reference Level : 1.5V
- 4) Output Load Capacitance : 1TTL + C_L (100pF)
(including scope and jig capacitance)

14.3 Attribute Memory Read Cycle

($V_{CC} = 4.5 \sim 5.5V, T_a = 0 \sim 60^\circ C$)

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Read Cycle Time	t_{CR}	t_{cR}	300	—	ns
Address Access Time	t_{ACC}	$t_a(A)$	—	300	
Card Enable Access Time	t_{CE}	$t_a(CE)$	—	300	
Output Enable Access Time	t_{OE}	$t_a(OE)$	—	150	
Output Disable Time from \overline{CE}		$t_{dis}(CE)$	—	100	
Output Disable Time from \overline{OE}	t_{DF}	$t_{dis}(OE)$	—	100	
Output Enable Time from \overline{CE}		$t_{en}(CE)$	5	—	
Output Enable Time from \overline{OE}		$t_{en}(OE)$	5	—	
Data Valid from Add Change	t_{OH}	$t_v(A)$	0	—	

○ Attribute Memory Read Cycle



- Note: 1. To read attribute memory, $\overline{REG} = \text{"LOW"}$, $\overline{WE} = \text{"HIGH"}$ and either $\overline{CE2} = \text{"LOW"}$ or else $\overline{CE2} = \text{"HIGH"}$ and $A0 = \text{"LOW"}$.
2. The output data becomes valid when last interval, $t_a(A)$, $t_a(CE)$ or $t_a(OE)$ have concluded.

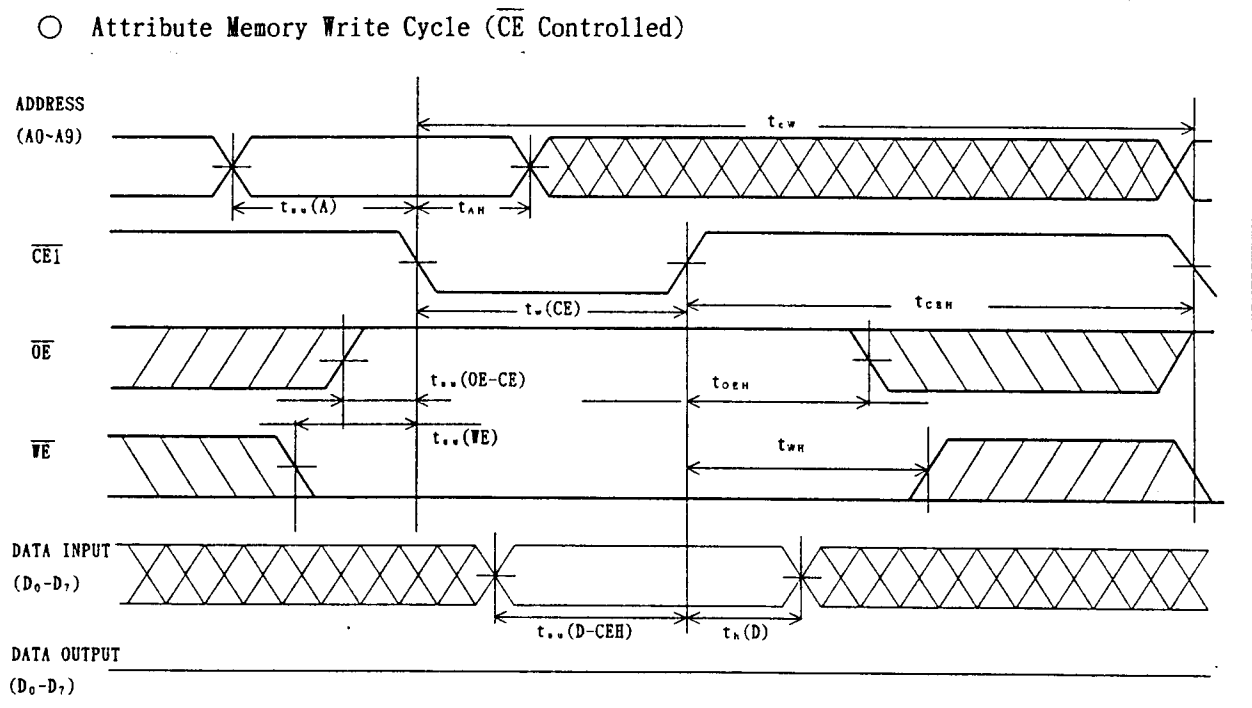
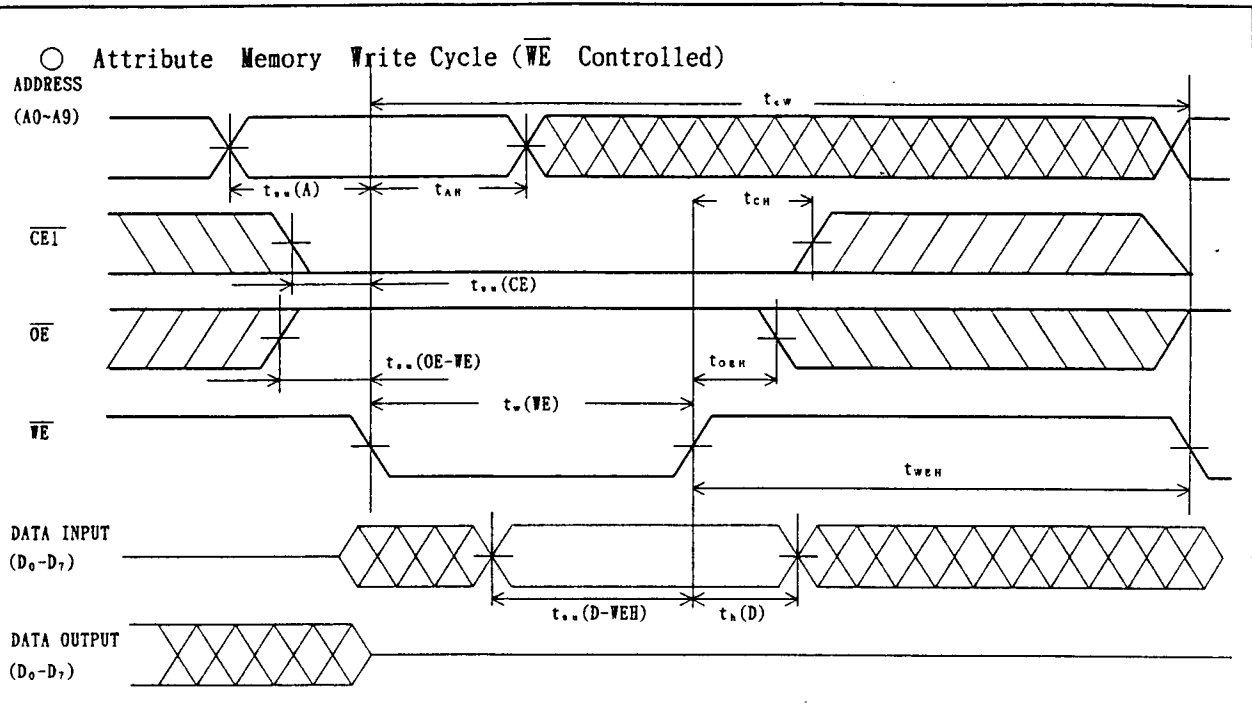
14.4 Attribute Memory Write Cycle

 \overline{WE} Controlled $(V_{CC}=4.5V\sim 5.5V, T_a=0\sim 60^\circ C)$

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time	t_{WC}	t_{cW}	10	—	ms
Write Pulse Width	t_{WP}	$t_w(WE)$	180	—	ns
Address Setup Time	t_{AS}	$t_{s,u}(A)$	10	—	
Data Setup Time for \overline{WE}	t_{DS}	$t_{s,u}(D-WEH)$	100	—	
Crad Enable Setup Time	t_{CES}	$t_{s,u}(CE)$	0	—	
Output Enable Setup Time	t_{OES}	$t_{s,u}(OE-WE)$	45	—	
Address Hold Time	t_{AH}		260	—	
Write Hold Time	t_{CH}		0	—	
Output Enable Hold Time	t_{OEH}		70	—	
\overline{WE} HIGH Hold Time	t_{WEH}		9.9	—	ms
Data Hold Time	t_{DH}	$t_h(D)$	80	—	ns

 \overline{CE} Controlled $(V_{CC}=4.5V\sim 5.5V, T_a=0\sim 60^\circ C)$

PARAMETER	SYMBOL		MIN	MAX	UNIT
	SYMBOL	SYMBOL(PCMCIA)			
Write Cycle Time	t_{WC}	t_{cW}	10	—	ms
Write Pulse Width	t_{WP}	$t_w(CE)$	210	—	ns
Address Setup Time	t_{AS}	$t_{s,u}(A)$	10	—	
Data Setup Time for \overline{CE}	t_{DS}	$t_{s,u}(D-CEH)$	100	—	
Write Enable Setup Time	t_{WES}	$t_{s,u}(WE)$	0	—	
Output Enable Setup Time	t_{OES}	$t_{s,u}(OE-CE)$	45	—	
Address Hold Time	t_{AH}		260	—	
Write Hold Time	t_{WH}		0	—	
Output Enable Hold Time	t_{OEH}		70	—	
\overline{CE} HIGH Hold Time	t_{CEH}		9.9	—	ms
Data Hold Time	t_{DH}	$t_h(D)$	80	—	ns



Note: To write attribute memory, \overline{REG} ="LOW" and either $\overline{CE2}$ ="LOW" or else $\overline{CE2}$ ="HIGH" and $A0$ ="LOW".

15. Specification Changes

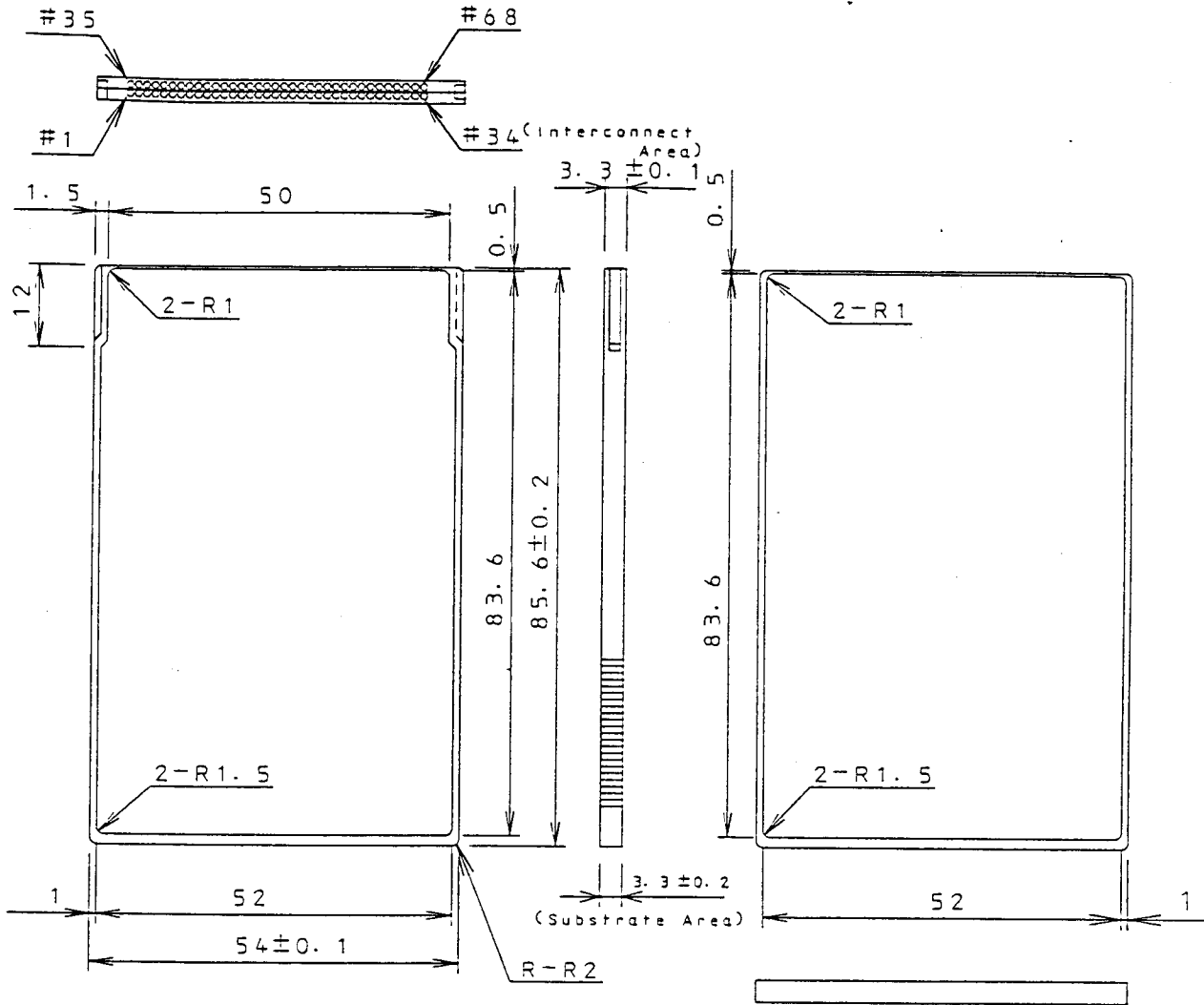
Specifications may be changed upon discussion and agreement between both parties.

16. Othes Precautions

- Permanent damage occurs if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

SHARP

17. External Diagrams



FRONT

BACK

APPLICABLE		SCALE	UNIT	△		
MODEL		1/1	mm	△		
THICKNESS		MATERIAL	FINISH	CH. DATE	REVISE	CHARGE
DATE	1994.11.16			MEMORY CARD EXTERNAL DIAGRAM		
DESIGN	DRAM	TRACE	CHECK	APPROVE	PCMCIA Rel. 2.0 TYPE I	
					Memory Card Business Project Team	
					IC GROUP	
					SHARP CORPORATION	
				DRAWING NO.	IMC001-A102	

18. PACKING SPECIFICATION

1D24XXXX

Parts List

Parts Name	Quantity
A Flexible Plastic Case	1
B Inner Carton (25 pieces contained)	25
C Outer Carton (100 pieces contained)	1
D Outer Case (100 pieces contained)	1

Packing Specification

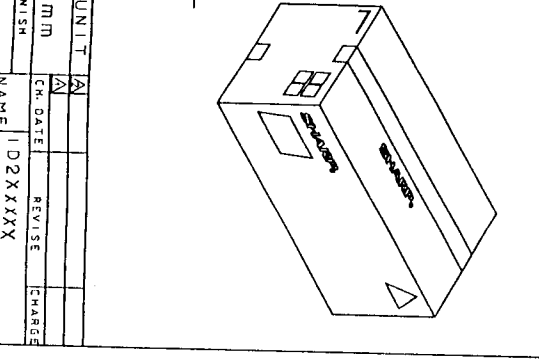
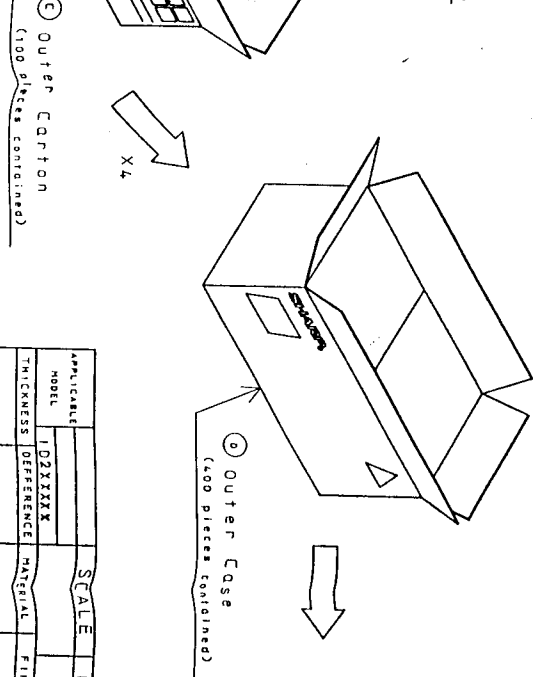
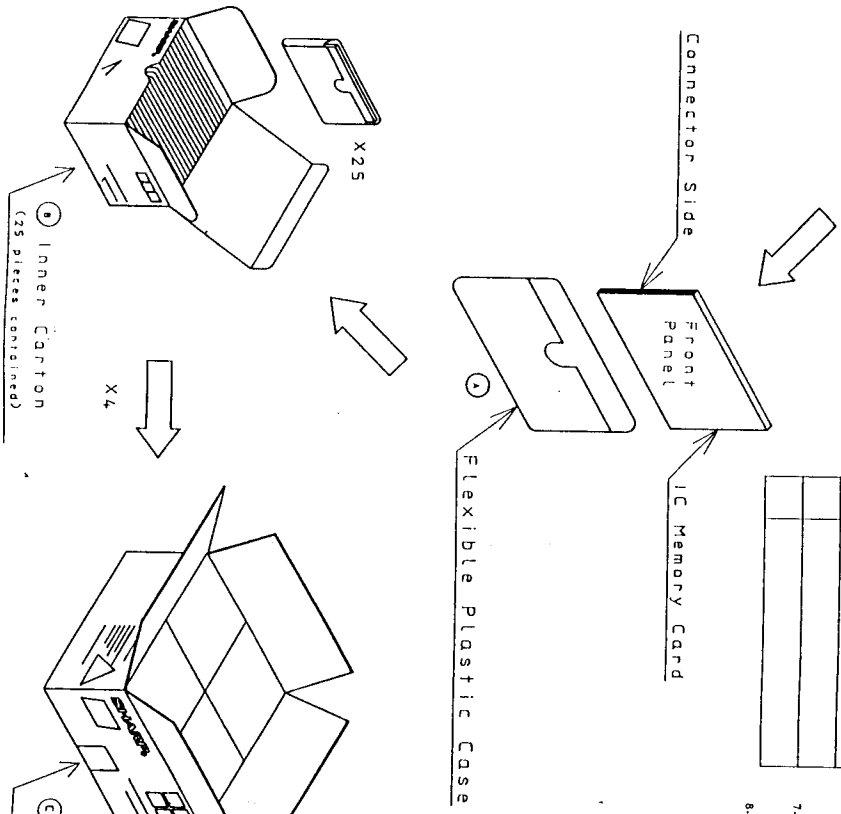
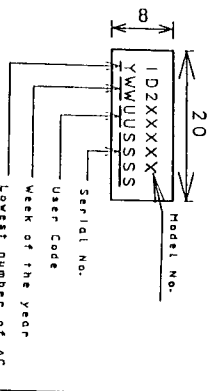
1. Label the Model No. and Manufacturing No. on the back panel of the card.
2. Each memory card is contained in the flexible plastic case. The "read" side of the card comes to the plate where the card is held, and the connector side is placed against the card point, so that the connector is not touched by fingers as shown in the figure.)
3. The inner carton contains 25 pieces of the card with the case. (Note 1.)
4. The product name, lot no. (product no.), quantity and the date are either written directly on the inner carton, or printed on the label which is then attached on inner carton.
5. The outer carton contains 4 inner cartons. (Note 2.)
6. The product name, lot no. (product no.), quantity and the date are either written directly on the outer carton, or printed on the label which is then attached on the outer carton.
7. The outer carton is then put in the outer case, which contains 4 outer cartons. (Note 3.)
8. The product name, lot no. (product no.), quantity and the date are either written directly on the case, or printed on the label which is then attached on the case.

Note 1: The least packing unit is 25 pieces which is the number contained in the inner carton.

2: The space inside the outer carton is filled card poor.

3: The other size of outer case may be used if there is not enough quantity to fill the normal outer cartons.

4: Size of label and denotations are following (unit: mm)

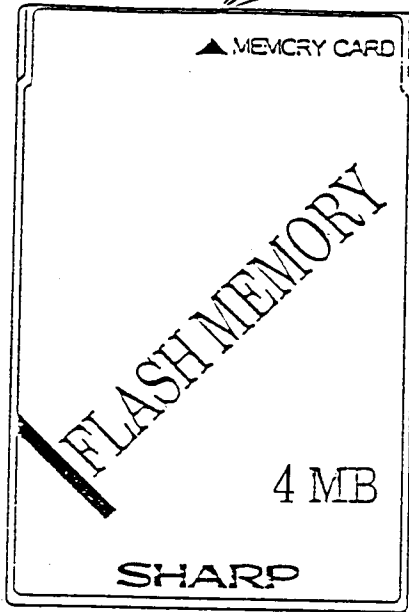


APPLICABLE	SCALE	UNIT	A
MODEL	ID2XXXXX	MM	A
THICKNESS	DIFFERENCE	MATERIAL	FINISH
DATE	1995.10.10		
DRAWING NO. IMC025-J300 SHARP CORPORATION DRAWING NO. IMC025-J300			

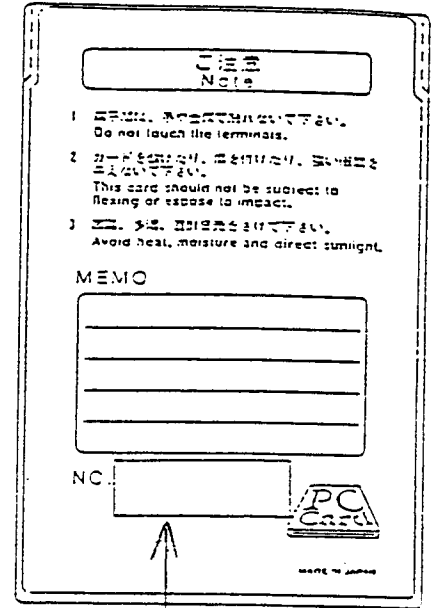
SHARP

19. EXTERNAL APPEARANCES

CONNECTOR SIDE

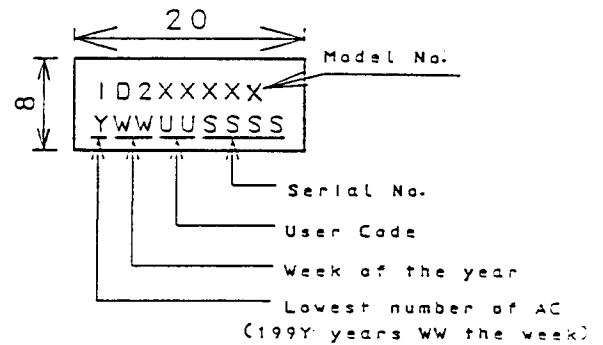


FRONT PANEL



LABELING POSITION
BACK PANEL

LABEL SIZE AND DENOTATIONS



APPLICABLE		SCALE	UNIT	△		
MODEL			mm	△	CH. DATE	REVISE
THICKNESS	DEFERENCE	MATERIAL	FINISH		NAME	
DATE	1995. 10. 10	MEMORY CARD BUSINESS PROJECT TEAM				
		INTEGRATED CIRCUITS GROUP				
		SHARP CORPORATION			DRAWING NO.	

FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM
READ ONLY MEMORY ETOX ID244E01 4M PC Card Conforms to PCMCIA Rel. 2.0 (ID24M040)