Integrated
Circuit
Systems, Inc.

ICS843252

FemtoClocks™ Crystal-to-3.3V LVPECL Frequency Synthesizer

General Description

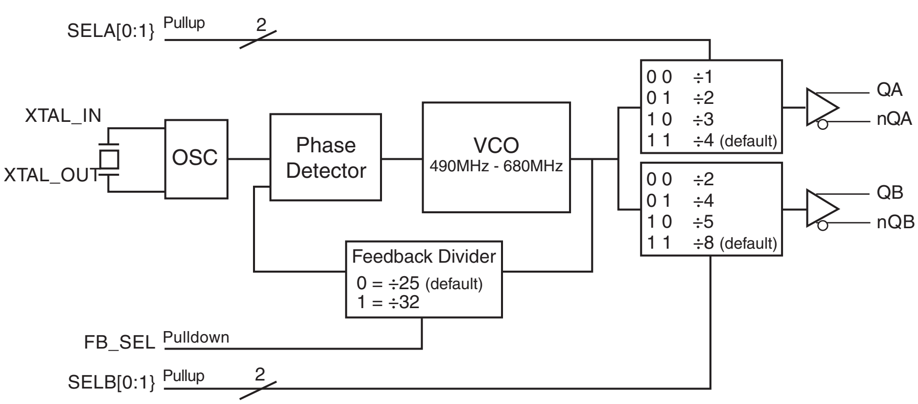
The ICS843252 is a 2 differential output LVPECL Synthesizer designed to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 19.53125MHz or 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (SEL[A1:A0], SEL[B1:B0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The ICS843252 ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS843252 is packaged in a small 16-pin TSSOP package.

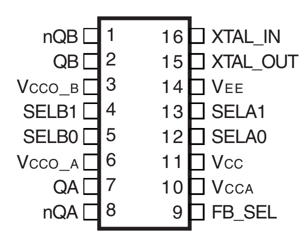
Features

- Two 3.3V differential LVPECL output pairs
- Using a 19.53125MHz or 25MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Crystal oscillator interface
- VCO range: 490MHz to 680MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.47ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature available upon request
- Available in both standard and lead-free RoHS-compliant packages

Block Diagram



Pin Assignment



ICS843252
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Νυμ βερ	Ναμ ε	Τψπε		∆εσχριπτιον
1, 2	nQB, QB	Output		Differential clock outputs. LVPECL interface levels.
3	V_{CCO_B}	Power		Output supply pin for QB, nQB outputs.
4, 5	SELB1, SELB0	Input	Pullup	Division select pins for Bank B. Default = High. LVCMOS/LVTTL interface levels.
6	V_{CCO_A}	Power		Output supply pin for QA output.
7, 8	QA, nQA	Output		Differential clock outputs. LVPECL interface levels.
9	FB_SEL	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷25. When HIGH, the feedback divider is set for ÷32. LVCMOS/LVTTL interface levels.
10	V_{CCA}	Power		Analog supply pin.
11	V_{CC}	Power		Core supply pin.
12, 13	SELA0, SELA1	Input	Pullup	Division select pins for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
14	V_{EE}	Power		Negative supply pin.
15, 16	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. BANK A FREQUENCY TABLE

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA/nQA Output Frequency (MHz)
Crystal Frequency (MHz)	FB_SEL	SELA1	SELA0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.500	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

TABLE 3B. BANK B FREQUENCY TABLE

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB/nQB Output Frequency (MHz)
Crystal Frequency (MHz)	FB_SEL	SELB1	SELB0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

TABLE 3C. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLES

Inputs		Outputs
SELA1	SELA0	QA
0	0	÷1
0	1	÷2
1	0	÷3
1	1	÷4 (default)

Inputs		Outputs
SELB1	SELB0	QB
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷8 (default)

TABLE 3D. FEEDBACK DIVIDER CONFIGURATION SELECT FUNCTION TABLE

Inputs	
FB_SEL	Feedback Divide
0	÷25 (default)
1	÷32

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A}, V_{CCO\_B}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			122		mA
I_{CCA}	Analog Supply Current			7		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FB_SEL	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		SELA0, SELA1, SELB0, SELB1	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	FB_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		SELA0, SELA1, SELB0, SELB1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_B} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_SEL = ÷25		19.6		27.2	MHz
	FB_SEL = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

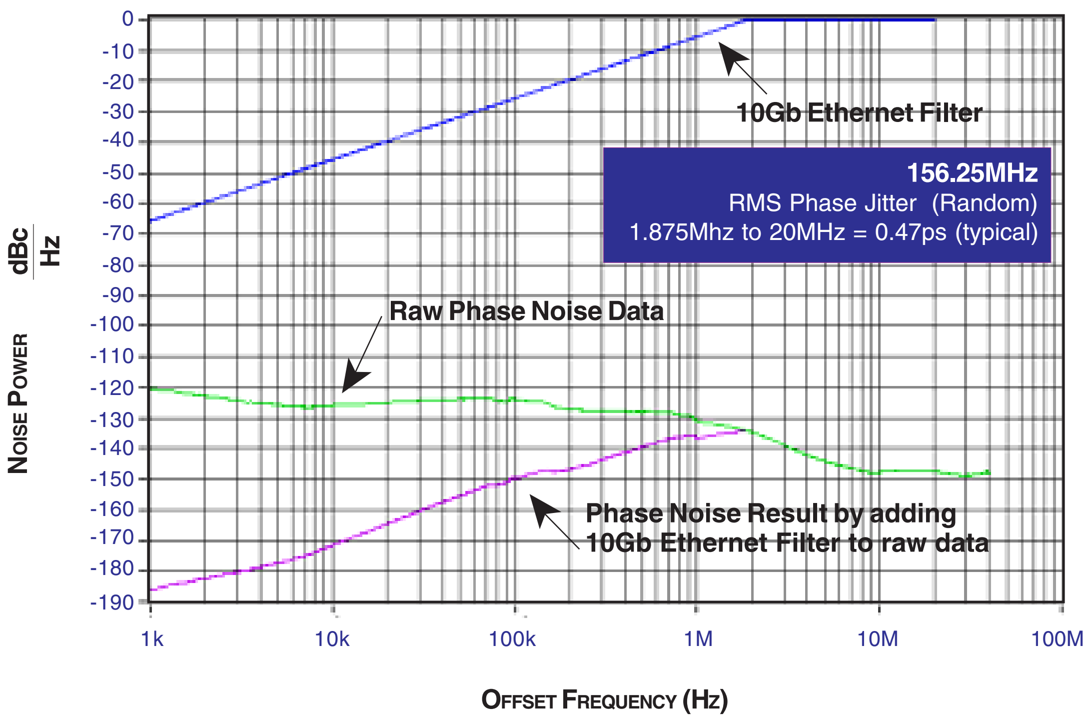
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO\_A,}\ V_{CCO\_B} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

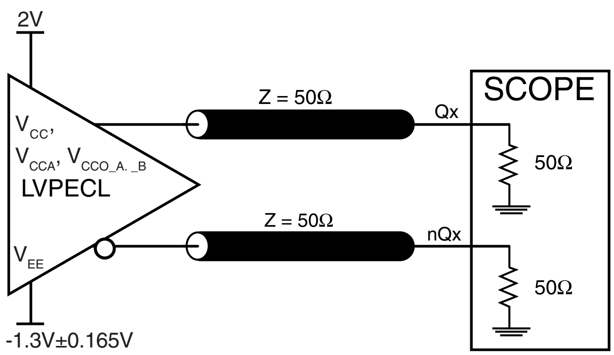
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	Output Divider = ÷1	490		680	MHz
		Output Divider = ÷2	245		340	MHz
		Output Divider = ÷3	163.33		226.67	MHz
		Output Divider = ÷4	122.5		170	MHz
		Output Divider = ÷5	98		136	MHz
		Output Divider = ÷8	61.25		85	MHz
*t*sk(o)	Output Skew; NOTE 1, 3	Outputs @ Same Frequency		TBD		ps
		Outputs @ Different Frequencies		TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	625MHz (1.875MHz - 20MHz)		0.36		ps
		312.5MHz (1.875MHz - 20MHz)		0.43		ps
		156.25MHz (1.875MHz - 20MHz)		0.47		ps
		125MHz (1.875MHz - 20MHz)		0.47		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

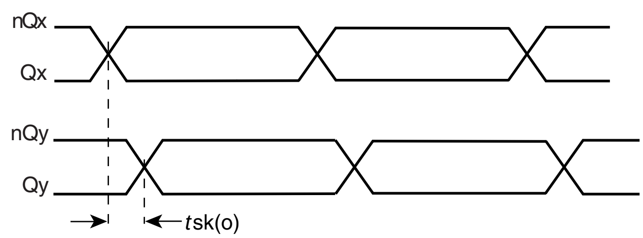
TYPICAL PHASE NOISE AT 156.25MHZ



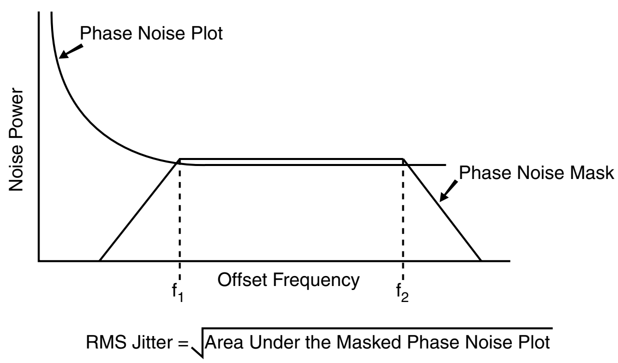
PARAMETER MEASUREMENT INFORMATION



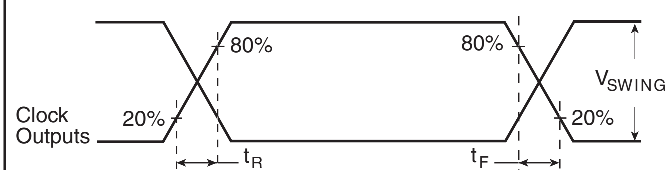
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



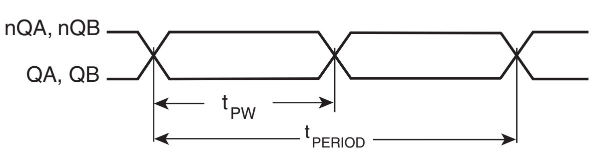
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843252 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_X} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

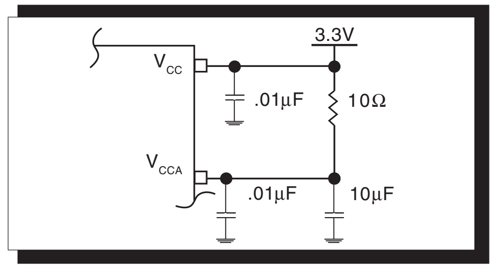


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843252 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 19.53125 or 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

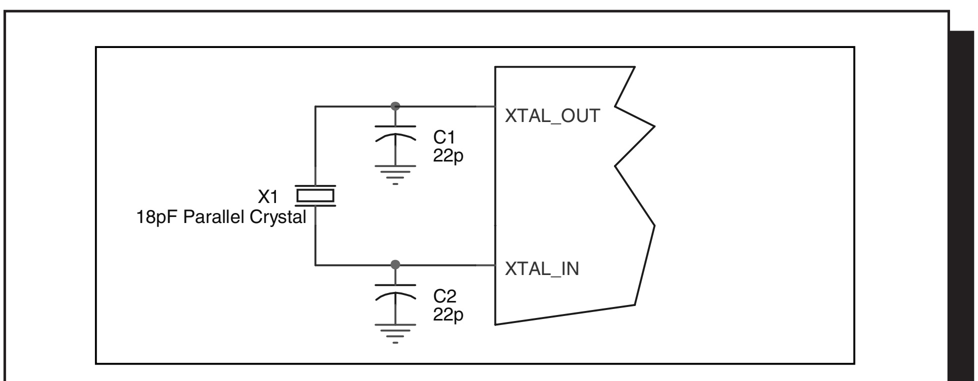


Figure 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

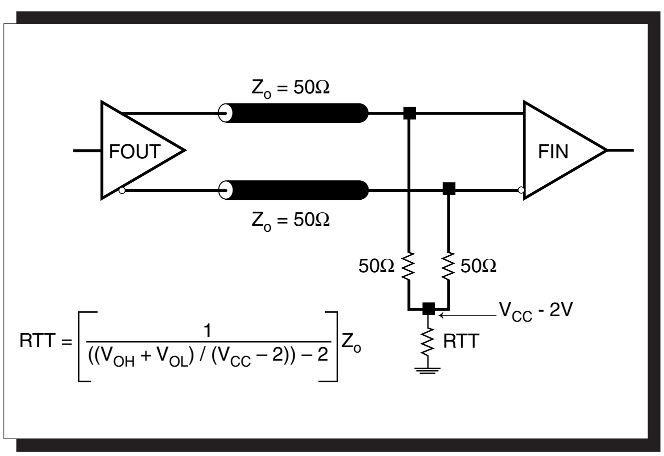


FIGURE 3A. LVPECL OUTPUT TERMINATION

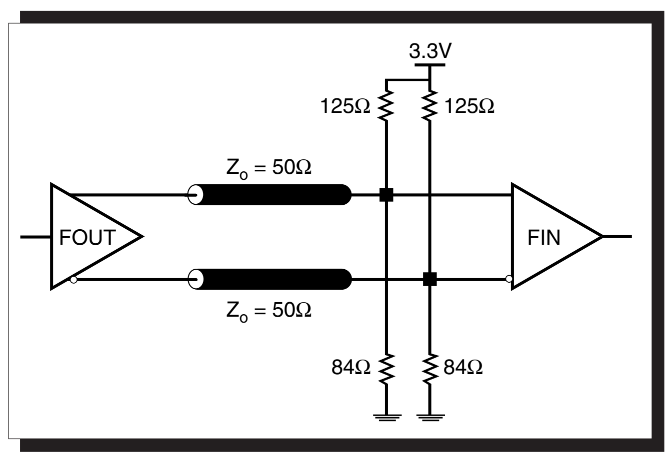


FIGURE 3B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843252. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843252 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 122mA = **422.73mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 422.73mW + 60mW = **482.73mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 81.8°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.483W * 81.8°C/W = 109.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

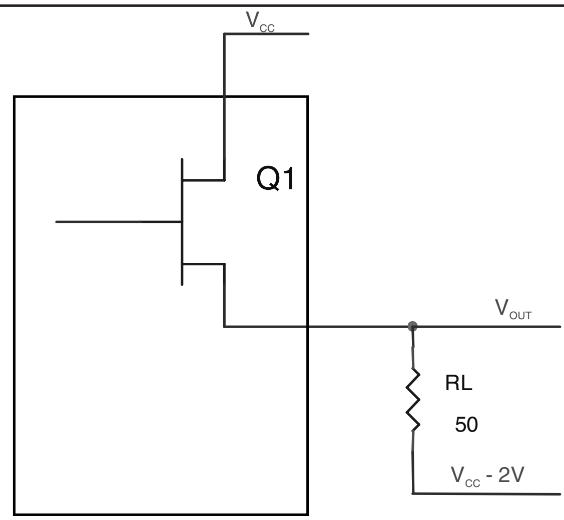


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS843252 is: 3822

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

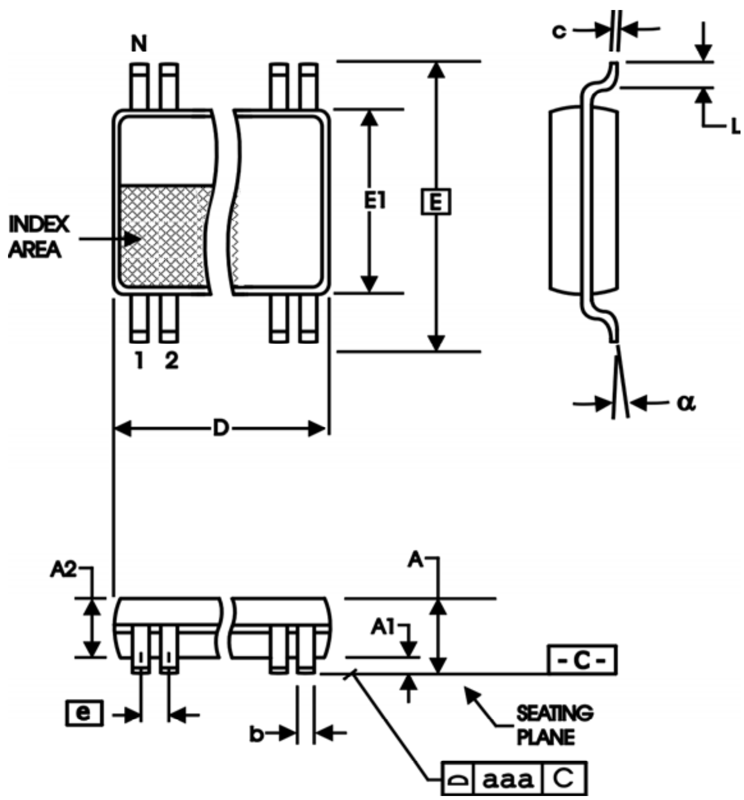


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843252AG	843252AG	16 Lead TSSOP	tube	0°C to 70°C
ICS843252AGT	843252AG	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843252AGLF	TBD	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843252AGLFT	TBD	16 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.