

Digital Filter

The HSP43881/883 is a video speed Digital Filter (DF) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally and a shift and add output stage, all in a single integrated circuit. Each filter cell contains a 8 x 8-bit multiplier, three decimation registers and a 26-bit accumulator. The output stage contains an additional 26-bit accumulator which can add the contents of any filter cell accumulator to the output stage accumulator shifted right by 8-bits. The HSP43881/883 has a maximum sample rate of 25.6MHz. The effective multiply accumulate (mac) rate is 204MHz.

The HSP43881/883 DF can be configured to process expanded coefficient and word sizes. Multiple DFs can be cascaded for larger filter lengths without degrading the sample rate or a single DF can process larger filter lengths at less than 25.6MHz with multiple passes. The architecture permits processing filter lengths of over 1000 taps with the guarantee of no overflows. In practice, most filter coefficients are less than 1.0, making even larger filter lengths possible. The DF provides for 8-bit unsigned or two's complement arithmetic, independently selectable for coefficients and signal data.

Each DF filter cell contains three resampling or decimation registers which permit output sample rate reduction at rates of 1/2, 1/3 or 1/4 the input sample rate. These registers also provide the capability to perform 2-D operations such as matrix multiplication and N x N spatial correlations/convolutions for image processing applications.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 0MHz to 25.6MHz Sample Rate
- Eight Filter Cells
- 8-Bit Coefficients and Signal Data
- Low Power CMOS Operation
- I_{CCSB} 500µA Maximum
- I_{CCOP} 160mA Maximum at 20MHz
- 26-Bit Accumulator Per Stage
- Filter Lengths Up to 1032 Taps
- Expandable Coefficient Size, Data Size and Filter Length
- Decimation by 2, 3 or 4

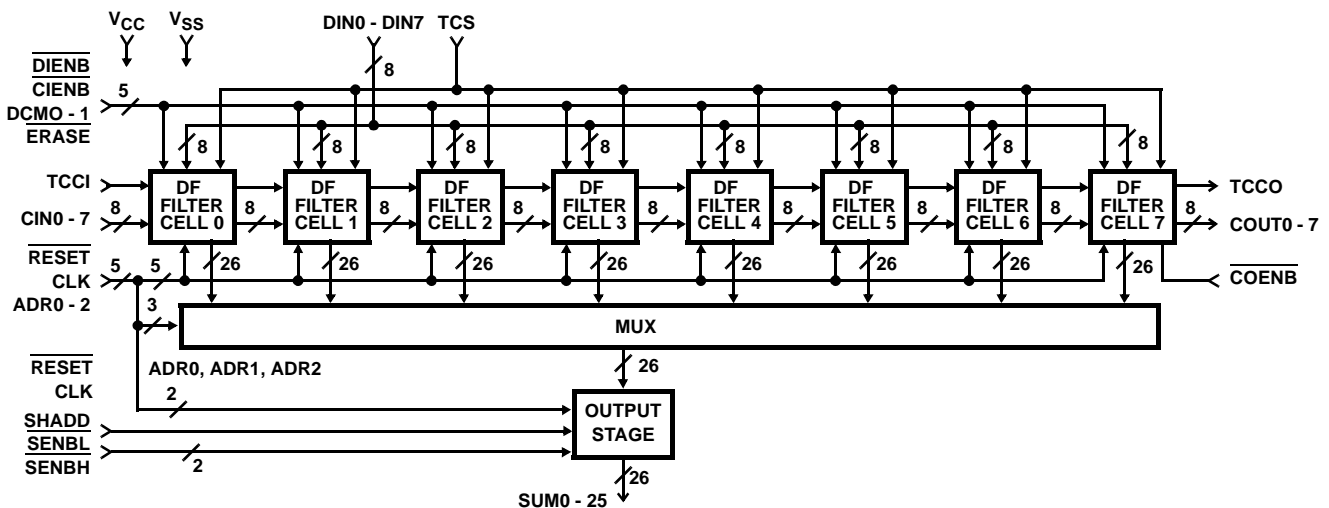
Applications

- 1-D and 2-D FIR Filters
- Radar/Sonar
- Adaptive Filters
- Echo Cancellation
- Complex Multiply-Add
- Sample Rate Converters

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP43881GM-25/883	-55 to 125	85 Ld PGA	G85.A

Block Diagram



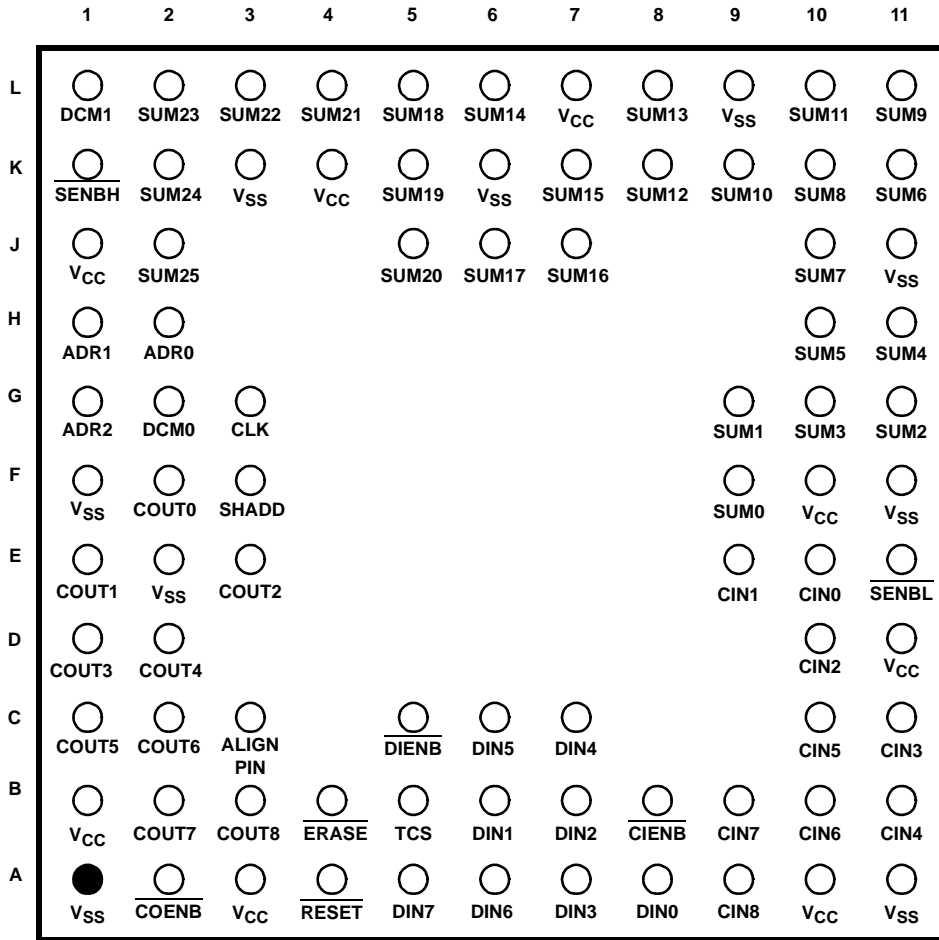
Pinouts

85 PIN PGA
TOP VIEW, PINS DOWN

	1	2	3	4	5	6	7	8	9	10	11
A	V _{SS}	COENB	V _{CC}	RESET	DIN7	DIN6	DIN3	DIN0	TCCI	V _{CC}	V _{SS}
B	V _{CC}	COU7	TCCO	ERASE	TCS	DIN1	DIN2	CIENB	CIN7	CIN6	CIN4
C	COU5	COU6	ALIGN PIN		DIENB	DIN5	DIN4			CIN5	CIN3
D	COU3	COU4								CIN2	V _{CC}
E	COU1	V _{SS}	COU2						CIN1	CIN0	SENBL
F	V _{SS}	COU0	SHADD						SUM0	V _{CC}	V _{SS}
G	ADR2	DCM0	CLK						SUM1	SUM3	SUM2
H	ADR1	ADR0								SUM5	SUM4
J	V _{CC}	SUM25			SUM20	SUM17	SUM16			SUM7	V _{SS}
K	SENBH	SUM24	V _{SS}	V _{CC}	SUM19	V _{SS}	SUM15	SUM12	SUM10	SUM8	SUM6
L	DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	V _{CC}	SUM13	V _{SS}	SUM11	SUM9

Pinouts (Continued)

85 PIN PGA
BOTTOM VIEW, PINS UP



NOTE: An overbar on a signal name represents an active LOW signal.

Absolute Maximum Ratings

Supply Voltage 8.0V
 Input, Output Voltage GND -0.5 to V_{CC} +0.5V
 ESD Rating Class 1

Operating Conditions

Voltage Range +4.5V to +5.5V
 Temperature Range -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PGA Package. 36.0 7.0
 Maximum Package Power Dissipation at 125°C
 PGA 1.44W
 Maximum Junction Temperature 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

Die Characteristics

Gate Count 17,762 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Logical One Input Voltage	V _{IH}	V _{CC} = 5.5V	1, 2, 3	-55 ≤ T _A ≤ 125	2.2	-	V
Logical Zero Input Voltage	V _{IL}	V _{CC} = 4.5V	1, 2, 3	-55 ≤ T _A ≤ 125	-	0.8	V
Output HIGH Voltage	V _{OH}	I _{OH} = -400µA V _{CC} = 4.5V (Note 2)	1, 2, 3	-55 ≤ T _A ≤ 125	2.6	-	V
Output LOW Voltage	V _{OL}	I _{OH} = -400mA V _{CC} = 4.5V (Note 2)	1, 2, 3	-55 ≤ T _A ≤ 125	-	0.4	V
Input Leakage Current	I _I	V _{IN} = V _{CC} or GND V _{CC} = 4.5V	1, 2, 3	-55 ≤ T _A ≤ 125	-10	+10	µA
Output Leakage Current	I _O	V _{IN} = V _{CC} or GND V _{CC} = 5.5V	1, 2, 3	-55 ≤ T _A ≤ 125	-10	+10	µA
Clock Input High	V _{IHC}	V _{CC} = 5.5V	1, 2, 3	-55 ≤ T _A ≤ 125	3.0	-	V
Clock Input Low	V _{ILC}	V _{CC} = 4.5V	1, 2, 3	-55 ≤ T _A ≤ 125	-	0.8	V
Standby Power Supply Current	I _{CCSB}	V _{IN} = V _{CC} or GND V _{CC} = 5.5V, Outputs Open	1, 2, 3	-55 ≤ T _A ≤ 125	-	500	µA
Operating Power Supply Current	I _{CCOP}	f = 20.0MHz V _{CC} = 5.5V (Note 3)	1, 2, 3	-55 ≤ T _A ≤ 125	-	160.0	mA
Functional Test	FT	(Note 4)	7, 8	-55 ≤ T _A ≤ 125	-	-	

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating supply current is proportional to frequency, typical rating is 8.0mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} = 2.6, V_{IL} = 0.4, V_{OH} ≥ 1.5V, V_{OL} ≤ 1.5V, V_{IHC} = 3.4V and V_{ILC} = 0.4V.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	NOTES	GROUP A SUBGROUPS	TEMPERATURE (°C)	-25 (25.6MHz)		UNITS
					MIN	MAX	
Clock Period	t _{CP}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	39	-	ns
Clock Low	t _{CL}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	16	-	ns
Clock High	t _{CH}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	16	-	ns
Input Setup	t _{IS}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	17	-	ns
Input Hold	t _{IH}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	0	-	ns
CLK to Coefficient Output Delay	t _{ODC}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	-	20	ns
Output Enable Delay	t _{OED}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	-	15	ns
CLK TO SUM Output Delay	t _{ODS}	Note 5	9, 10, 11	-55 ≤ T _A ≤ 125	-	25	ns

NOTE:

- AC Testing: V_{CC} - 4.5V and 5.5V. Inputs are driven at 3.0V for a Logic “1” and 0.0V for a Logic “0”. Input and output timing measurements are made at 1.5V for both a Logic “1” and “0”. CLK is driven at 4.0V and 0V and measured at 2.0V.

TABLE 3. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	NOTES	TEMP (°C)	-25 (25.6MHz)		UNITS
					MIN	MAX	
Input Capacitance	C _{IN}	VCC = Open, f = 1MHz All measurements are referenced to device GND	6	T _A = 25	-	15	pF
Output Capacitance	C _{OUT}		6	T _A = 25	-	15	pF
Output Disable Delay	t _{ODD}		6, 7	-55 ≤ T _A ≤ 125	-	15	ns
Output Rise Time	t _{OR}		6, 7	-55 ≤ T _A ≤ 125	-	6	ns
Output Fall Time	t _{OF}		6, 7	-55 ≤ T _A ≤ 125	-	6	ns

NOTES:

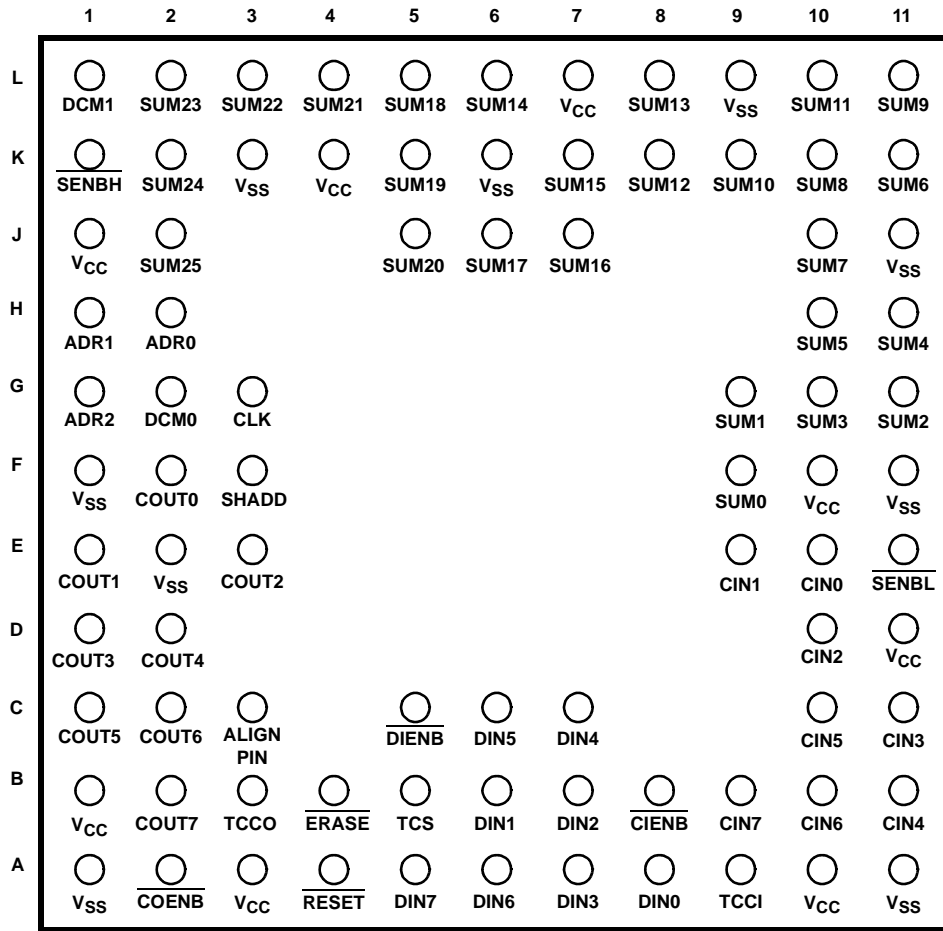
- The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
- Loading is as specified in the test load circuit, C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Burn-In Circuit

BOTTOM VIEW, PINS UP



BURN-IN SIGNALS

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	V _{SS}	GND	C1	COU5	V _{CC} /2	F10	V _{CC}	V _{CC}	K4	V _{CC}	V _{CC}
A2	$\overline{\text{COENB}}$	F10	C2	COU6	V _{CC} /2	F11	V _{SS}	GND	K5	SUM19	V _{CC} /2
A3	V _{CC}	V _{CC}	C3	ALIGN	NC	G1	ADR2	F2	K6	V _{SS}	GND
A4	RESET	F11	C5	$\overline{\text{DIENB}}$	F10	G2	DCMO	F5	K7	SUM15	V _{CC} /2
A5	DIN7	F8	C6	DIN5	F5	G3	CLK	F0	K8	SUM12	V _{CC} /2
A6	DIN6	F6	C7	DIN4	F4	G9	SUM1	V _{CC} /2	K9	SUM10	V _{CC} /2
A7	DIN3	F3	C10	CIN5	F5	G10	SUM3	V _{CC} /2	K10	SUM8	V _{CC} /2
A8	DIN0	F0	C11	CIN3	F3	G11	SUM2	V _{CC} /2	K11	SUM6	V _{CC} /2
A9	CIN8/5CCI	F8	D1	COU3	V _{CC} /2	H1	ADR1	F1	L1	DCM1	F6
A10	V _{CC}	V _{CC}	D2	COU4	V _{CC} /2	H2	ADR0	F0	L2	SUM23	V _{CC} /2
A11	V _{SS}	GND	D10	CIN2	F2	H10	SUM5	V _{CC} /2	L3	SUM22	V _{CC} /2
B1	V _{CC}	V _{CC}	D11	V _{CC}	V _{CC}	H11	SUM4	V _{CC} /2	L4	SUM21	V _{CC} /2
B2	COU7	V _{CC} /2	E1	COU1	V _{CC} /2	J1	V _{CC}	V _{CC}	L5	SUM18	V _{CC} /2
B3	COU8/TCC0	V _{CC} /2	E2	V _{SS}	GND	J2	SUM25	V _{CC} /2	L6	SUM14	V _{CC} /2
B4	$\overline{\text{ERASE}}$	F10	E3	COU2	V _{CC} /2	J5	SUM20	V _{CC} /2	L7	V _{CC}	V _{CC}
B5	DIN8/TCS	F7	E9	CIN1	F1	J6	SUM17	V _{CC} /2	L8	SUM13	V _{CC} /2
B6	DIN1	F1	E10	CIN0	F0	J7	SUM16	V _{CC} /2	L9	V _{SS}	GND
B7	DIN2	F2	E11	$\overline{\text{SENBL}}$	F10	J10	SUM7	V _{CC} /2	L10	SUM11	V _{CC} /2
B8	$\overline{\text{CIENB}}$	F10	F1	V _{SS}	GND	J11	V _{SS}	GND	L11	SUM9	V _{CC} /2
B9	CIN7	F7	F2	COU0	V _{CC} /2	K1	$\overline{\text{SENBH}}$	F10			
B10	CIN6	F6	F3	SHADD	F9	K2	SUM24	V _{CC} /2			
B11	CIN4	F4	F9	SUM0	V _{CC} /2	K3	V _{SS}	GND			

NOTES:

8. V_{CC}/2 (2.7 ±10% used for outputs only).
9. 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
10. V_{CC} = 5.5V ±0.5V.
11. 0.1μF (minimum) capacitor between V_{CC} and GND per device.
12. F0 = 100kHz ±10%, F1 = F0/2, F2 = F1/2..., F11 = F10/2, 40% - 60% duty cycle.
13. Input voltage limits: V_{IL} = 0.8V maximum, V_{IH} = 4.5V ±10%.

Die Characteristics**DIE DIMENSIONS:**

328 mils x 283 mils x ±1 mil

METALLIZATION:

Type: Si-Al or Si-Al-Cu
 Thickness: 8kÅ

GLASSIVATION

Type: Nitrox
 Silox Thickness: 10kÅ

WORST CASE CURRENT DENSITY:1.2 x 10⁵ A/cm²

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