

# CML Semiconductor Products

PRODUCT INFORMATION

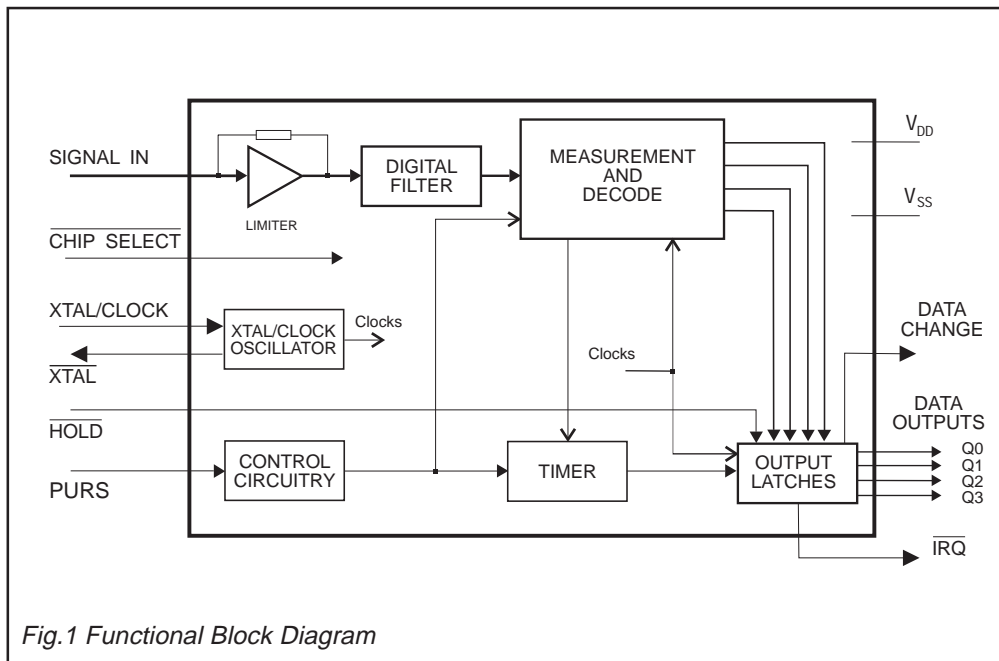
## FX623 Call Progress Tone Decoder

Publication D/623/3 July 1994

Provisional Issue

### Features

- Measures Call Progress Tone Frequencies ['Busy', 'Dial', 'Fax-Tone' etc.]
- Telephone, PABX, Fax and Dial-Up Modem Applications
- Low-Power Requirement (600 $\mu$ A at 3.3 Volts<sub>TYP</sub>) for Line-Powered Applications
- Custom Tone Decoder [13 Call-Progress Frequencies Recognized]
- Operates to a 3.579545MHz Telephone System Clock
- Operates Under Simple Logic or  $\mu$ Processor System Control



# FX623

### Brief Description

The FX623 is a low-power decoding microcircuit that measures the frequency of telephone system call progress tones.

With progress signals input from the telephone line, this single-chip product is programmed to recognize up to thirteen of the World's most commonly used call-progress frequencies, analyze signal quality and present the measured result as a 4-bit parallel data word at the tri-state Data Output.

Using the parallel information from the FX623, the host system suitably configured, can recognize such call progress information as: 'Dial', 'Busy', 'Number Unobtainable', 'Ringing' and Fax/Modem system signals.

This information can then be employed in telephone applications (simple or complex) to control telephone operations. The data output will require a suitable software format to analyze the frequency information from the FX623.

Requiring only a single 3.0<sub>MIN</sub> volt power supply, the FX623 may be line-powered and will operate under simple logic or system  $\mu$ Processor control using the 'Data-Change', 'Hold' and 'Chip-Select' functions.

The FX623, whose small size and low power consumption makes it ideal for remote applications, requires a 3.579545MHz telephone system clock or Xtal input, is available in a 16-pin plastic DIL package.

## Pin Number

## Function

FX623P	
<p>1 2 3 4</p>	<p><b>Q3: Data Outputs:</b> A 4-bit parallel data word, forming a HEX character representing the decoded tone frequency. This word is output after a successful decode. Table 1 details the Hex character output codes for the relevant decoded tone frequencies. Upon power-up this output is set to 'E<sub>H</sub>', but no Data Change pulse generated. These are tri-state outputs.</p>
5	<p><b>V<sub>DD</sub>:</b> Positive supply rail. A minimum supply voltage of 3.0 volts is required. Levels and voltages within this decoder are dependent upon this supply.</p>
6	<p><b>Signal In:</b> The composite audio input. Signals to this pin should be a.c. coupled. The d.c. bias of the limiter section is set internally; this pin should not be loaded with any other circuitry.</p>
7	<p>No internal connection. Leave open circuit.</p>
8	<p><b>Xtal:</b> The output of the on-chip clock oscillator inverter.</p>
9	<p>No internal connection. Leave open circuit.</p>
10	<p><b>Xtal/Clock:</b> The input to the clock oscillator inverter. A 3.579545MHz Xtal or externally derived clock should be connected here (see Figure 2).</p>
11	<p><b>V<sub>SS</sub>:</b> Negative supply rail (GND).</p>
12	<p><b>Hold:</b> An input to control the Output Latch condition; employed in combination with the Data Change output to facilitate, if required, Interrupt and/or handshake operations with a <math>\mu</math>Processor. With Hold placed "Low", with a tone input, the Data Change output will be held "High" at the next data change, and the current output code is locked in the Output Latches regardless of any changes to the input signal. The output code remains as held until this input is returned "High" (see Figure 3). Whilst this input is "High" the output data, Q0 - Q3, cycles normally with the input audio. This pin has an internal 1.0M<math>\Omega</math> pullup resistor.</p>
13	<p><b>PURS:</b> Power-Up ReSet. To reset internal circuitry at power-up; a logic "1" level is required at this pin for a duration of at least 2.5mS after the Xtal/Clock input and full V<sub>DD</sub> levels are applied. The component configuration shown in Figure 2 is recommended; for slow-rising power supplies the time constant of components should be increased accordingly.</p>
14	<p><b>IRQ:</b> Interrupt Request. An output for <math>\mu</math>Processor operation; normally "High" this output is latched "Low" when an internal data change occurs if the Chip Select input is "High". This output is reset ("High") the when Chip Select line is taken "Low". To permit "wire-OR" connection with other peripherals, this output has a low-impedance when "Low" and a high-impedance when "High".</p>
15	<p><b>CS:</b> Chip Select- A controlling function. When held "High" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are disabled. When taken "Low" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are enabled; the Interrupt Request (IRQ) is reset ("High") when CS is taken "Low". See Figures 3 and 4.</p>
16	<p><b>Data Change:</b> A positive-going pulse is generated at this output when the data changes (Tone or NOTONE). New tone-data is presented to the Q0, Q1, Q2 and Q3 Data Outputs if the Hold input is set "High". This is a tri-state output.</p>

# Application Information

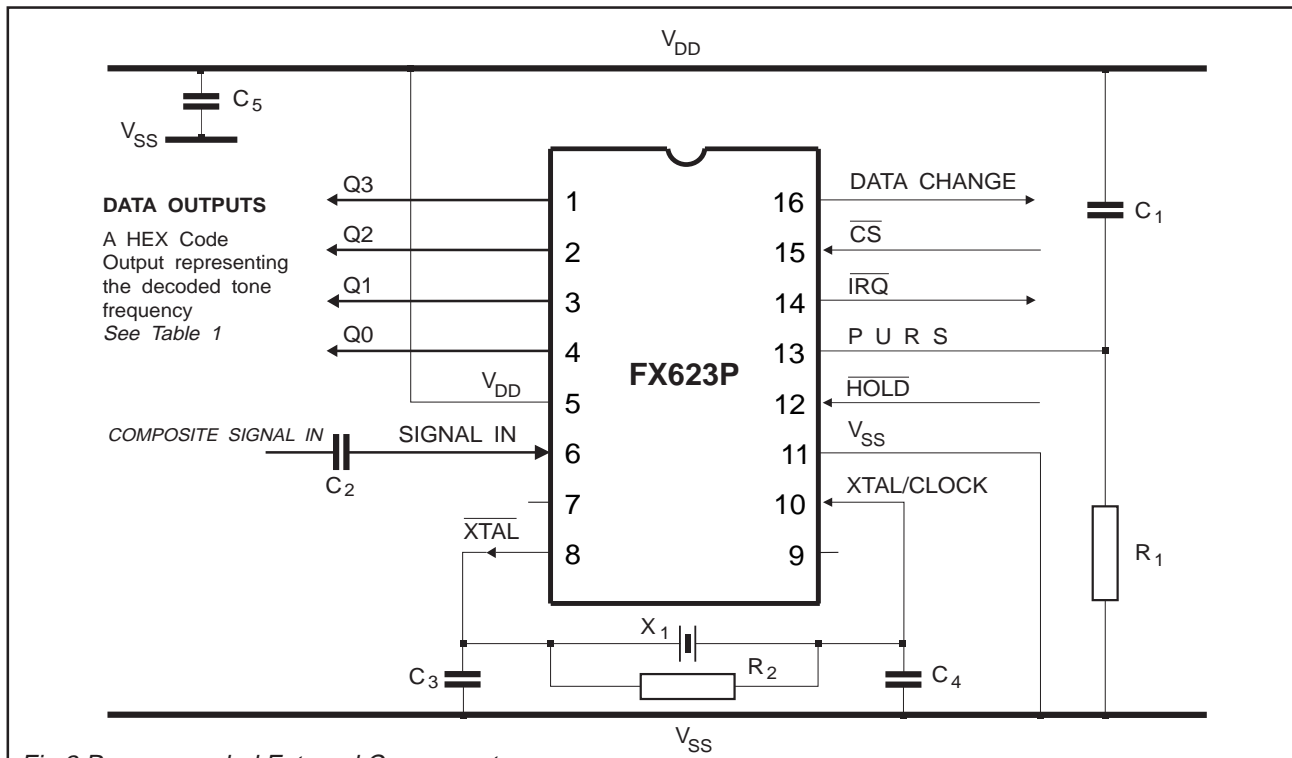


Fig.2 Recommended External Components

Hex Character	Output Code Q3 Q2 Q1 Q0	Band Edges (Hz) Lower Edge	Upper Edge	Nominal Centre Freq.
0	0 0 0 0	364	386	375
1	0 0 0 1	488	520	500
2	0 0 1 0	520	580	550
3	0 0 1 1	580	618	600
4	0 1 0 0	386	412	400
5	0 1 0 1	412	436	425
6	0 1 1 0	436	463	450
7	0 1 1 1	463	487	475
8	1 0 0 0	900	1008	950
9	1 0 0 1	1273	1325	1300
A	1 0 1 0	1350	1455	1400
B	1 0 1 1	1750	1855	1800
C	1 1 0 0	2062	2140	2100
D	1 1 0 1	frequency not guaranteed		
E	1 1 1 0	frequency not guaranteed		
F	1 1 1 1	NOTONE		

Table 1 Tone Decode Frequencies

Component	Value
R <sub>1</sub>	1.0MΩ
R <sub>2</sub>	1.0MΩ
C <sub>1</sub>	47.0nF
C <sub>2</sub>	4.7nF
C <sub>3</sub>	33.0pF
C <sub>4</sub>	33.0pF
C <sub>5</sub>	1.0μF
X <sub>1</sub>	3.579545MHz

Tolerances R = ±10% C = ±20%

## Timing Information

With CS Low - Figure 3.

After initial power-up and the Hold input inactive (High), as frequencies are input, with the Data Change output as an active (High) indicator, the data is presented at the Data Outputs.

If/when the Hold input is placed active (Low), the data at the Data Outputs is frozen and the Data Change output held High at its next active excursion - until the Hold input is returned High.

With the Hold input held High - Figure 4.

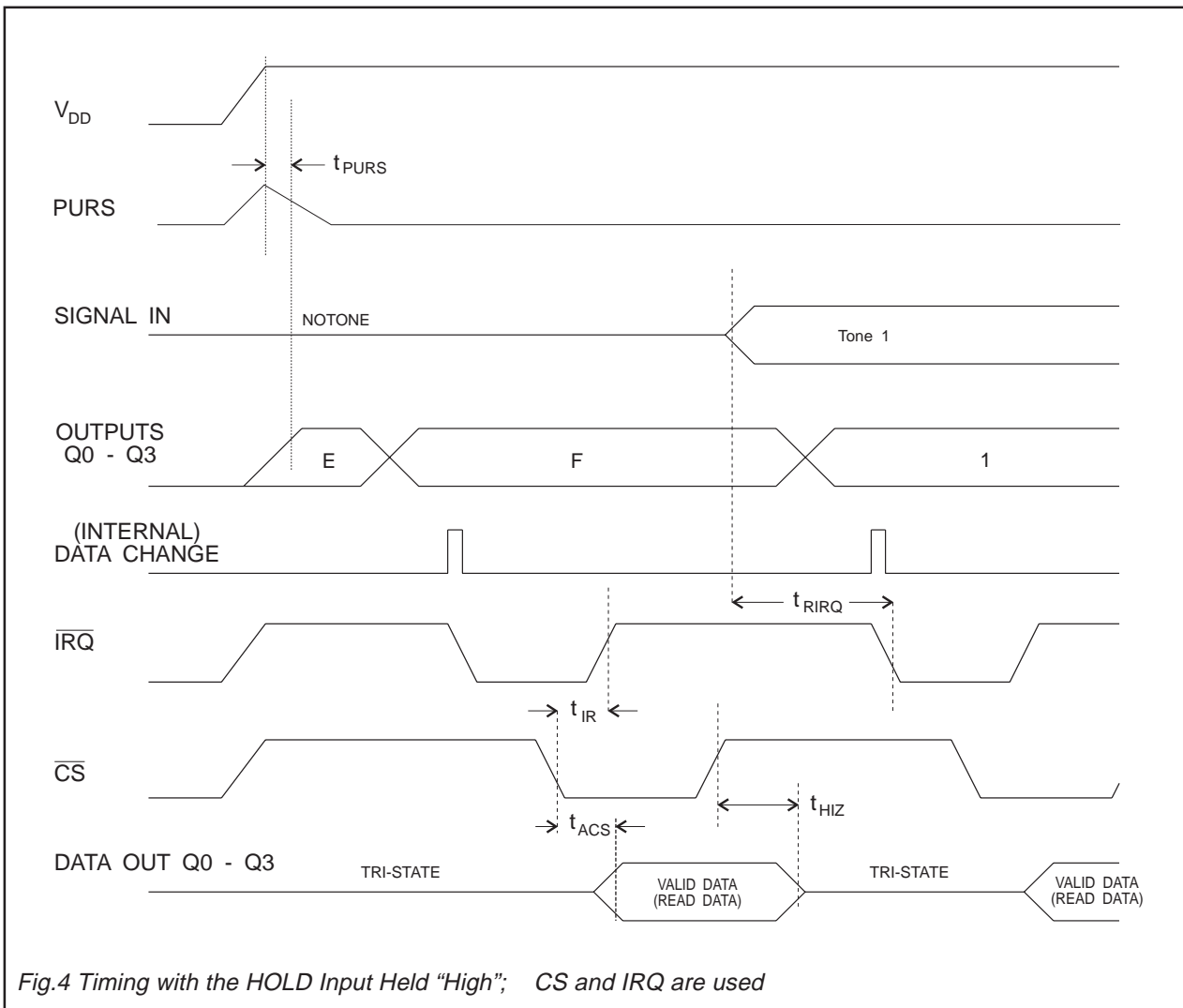
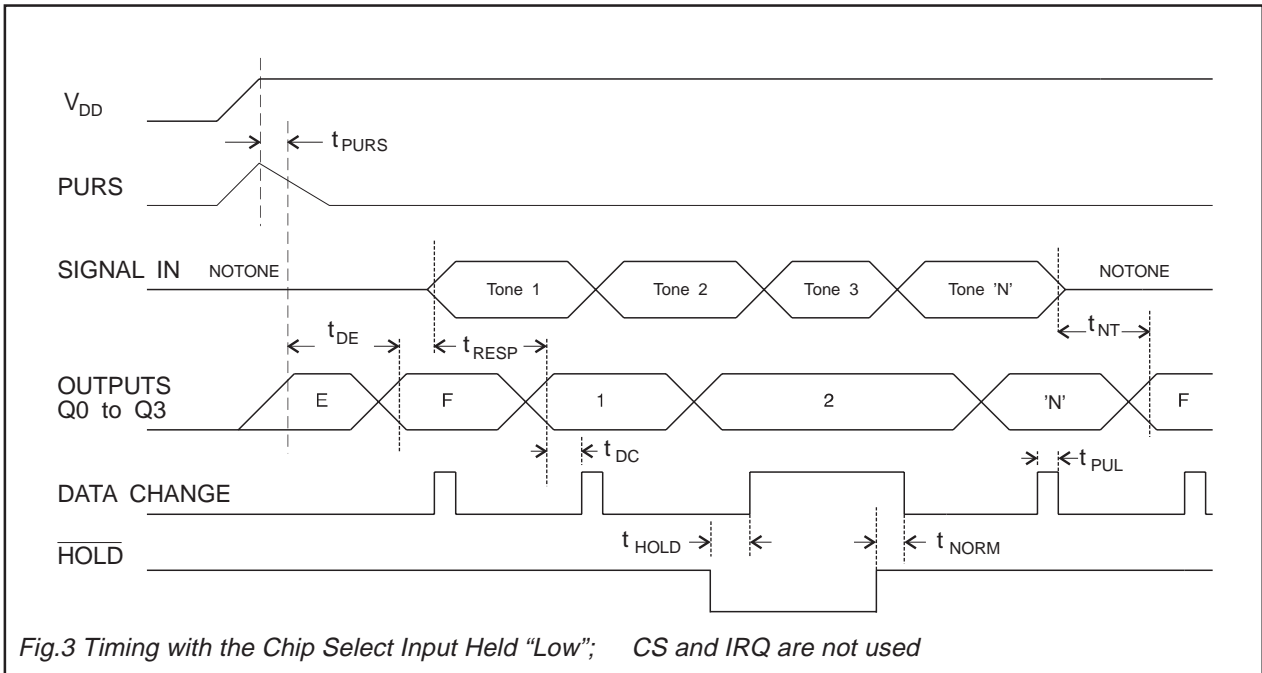
As frequencies are input a correct decode will produce an active (Low) interrupt level.

This interrupt (IRQ) is serviced and reset by an active (Low) CS input.

Note the 'valid data' period at the Data Outputs.

# Application Information

## Decoder Timing



## Specification

### Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref $V_{SS} = 0V$ )	-0.3 to ( $V_{DD} + 0.3V$ )
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ $T_{AMB} = 25^{\circ}C$	800mW Max.
Derating	10mW/ $^{\circ}C$
Storage temperature range: <b>FX623P</b>	-40 $^{\circ}C$ to +85 $^{\circ}C$ (plastic)

### Operating Limits .....

	Min.	Max.	Unit	
Supply Voltage ( $V_{DD}$ )	3.0	5.5	V	at 25 $^{\circ}C$
Operating Temperature .....	-40	+85	$^{\circ}C$	

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD} = 3.3V$ ,  $T_{OP} = -40$  to +85  $^{\circ}C$ . Audio Level 0dB ref: = 775mVrms. Xtal/Clock Frequency = 3.579545MHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Static Values</b>					
Supply Current		-	0.6	1.0	mA
Input Logic "1"		0.7	-	-	% $V_{DD}$
Input Logic "0"		-	-	0.3	% $V_{DD}$
Output Logic "1"		0.8	-	-	% $V_{DD}$
Output Logic "0"		-	-	0.2	% $V_{DD}$
<b>Impedance</b>					
CS and PURS Input		10.0	-	-	M $\Omega$
Hold Input	1	0.5	-	-	M $\Omega$
Signal Input		0.1	-	-	M $\Omega$
IRQ Output (logic "1")		-	30.0	100	k $\Omega$
IRQ Output (logic "0")		-	175	500	$\Omega$
Q0 - Q3 & Data-Change Outputs (logic "1")		-	0.7	2.0	k $\Omega$
Q0 - Q3 & Data-Change Outputs (logic "0")		-	175	500	$\Omega$
Q0 - Q3 & Data-Change Outputs (high Z)		1.0	-	-	M $\Omega$
<b>Dynamic Values</b>					
Signal Input Range	2, 5	35.0	-	1,166	mVrms
Decode Bandedge Tolerance	3	-1.0	-	1.0	%
<b>Xtal Inverter</b>					
Voltage Gain		20.0	-	-	V/V
Input Impedance		10.0	-	-	M $\Omega$
Output Impedance		-	-	160	k $\Omega$
<b>Decoder Timing - Figures 3 and 4</b>					
Power Up Reset Time		$t_{PURS}$	2.5	-	ms
Data 'E' Time		$t_{DE}$	31.0	-	ms
NOTONE to Tone Response Time	4	$t_{RESP}$	-	27.0	50.0
Tone to NOTONE Response Time	4	$t_{NT}$	-	-	60.0
Data to Data-Change Pulse Time		$t_{DC}$	0.625	-	1.15
Data-Change Pulse Width		$t_{PUL}$	-	1.25	-
Hold to Data-Change Rise Time		$t_{HOLD}$	63.0	-	$\mu s$
HOLD to Data-Change Fall Time		$t_{NORM}$	-	-	150
IRQ Tone Response Time		$t_{RIRQ}$	-	29.0	52.0
IRQ Reset Time		$t_{IR}$	-	-	250
Data Access Time		$t_{ACS}$	-	-	250
CS High to Output Tri-State Time		$t_{HIZ}$	-	-	100

#### Notes

1. This pin has an on-chip 1.0M $\Omega$  pullup resistor.
2. An a.c. coupled sine or squarewave.
3. See Table 1, Tone Decode Frequencies.
4. Delay between the change of input (Tone/NOTONE) and the change at the Q0 - Q3 outputs.
5. The signal input maximum value is determined by the formula  $V_{DD}/2.83$ .

## Package Outlines

The FX623 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.

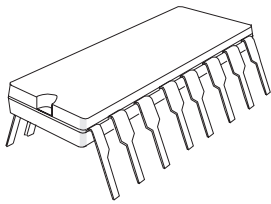
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

## Handling Precautions

The FX623 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

**FX623P** 16-pin plastic DIL **(P3)**

**NOT TO SCALE**



Max. Body Length 20.57mm  
Max. Body Width 6.60mm

## Ordering Information

**FX623P** 16-pin plastic DIL **(P3)**