

## FQP7P20

### 200V P-Channel MOSFET

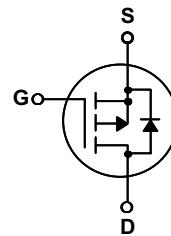
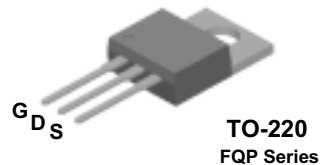
#### General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

#### Features

- -7.3A, -200V,  $R_{DS(on)} = 0.69\Omega @ V_{GS} = -10V$
- Low gate charge ( typical 19 nC)
- Low Crss ( typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



#### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQP7P20	Units
V <sub>DSS</sub>	Drain-Source Voltage	-200	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	-7.3	A
		-4.6	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	-29.2	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	570	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	-7.3	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	9.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-5.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	90	W
		0.72	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

#### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	--	1.39	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink	0.5	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-200	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25°C	--	-0.1	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -200 V, V <sub>GS</sub> = 0 V	--	--	-1	μA
		V <sub>DS</sub> = -160 V, T <sub>C</sub> = 125°C	--	--	-10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA

<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-3.0	--	-5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.65 A	--	0.54	0.69	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -40 V, I <sub>D</sub> = -3.65 A (Note 4)	--	4.4	--	S

<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	590	770	pF
C <sub>oss</sub>	Output Capacitance		--	140	180	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	25	35	pF

<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -100 V, I <sub>D</sub> = -7.3 A, R <sub>G</sub> = 25 Ω  (Note 4, 5)	--	15	40	ns
t <sub>r</sub>	Turn-On Rise Time		--	110	230	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	30	70	ns
t <sub>f</sub>	Turn-Off Fall Time		--	42	90	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -160 V, I <sub>D</sub> = -7.3 A, V <sub>GS</sub> = -10 V  (Note 4, 5)	--	19	25	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4.6	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	9.5	--	nC

<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	-7.3	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-29.2	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -7.3 A	--	--	-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -7.3 A, di <sub>F</sub> / dt = 100 A/μs (Note 4)	--	180	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.07	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 16mH, I<sub>AS</sub> = -7.3A, V<sub>DD</sub> = -50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ -7.3A, di/dt ≤ 300A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

# Typical Characteristics

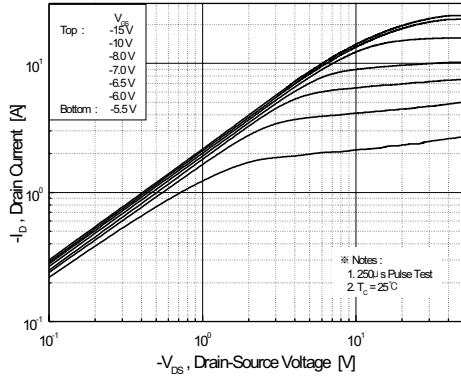


Figure 1. On-Region Characteristics

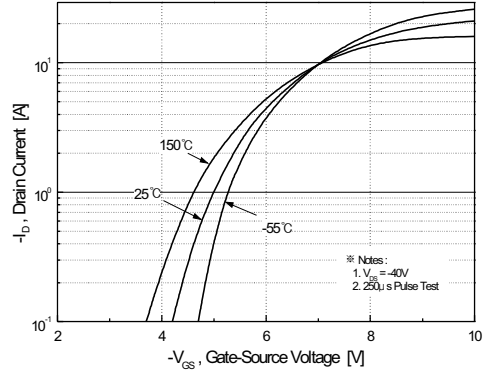


Figure 2. Transfer Characteristics

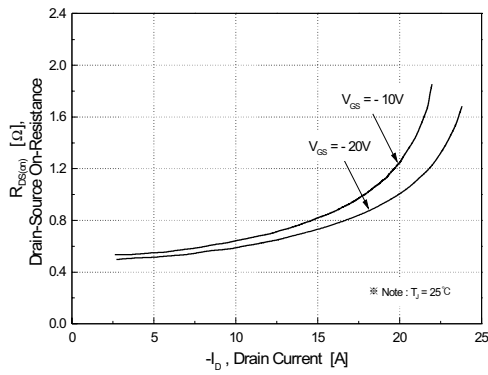


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

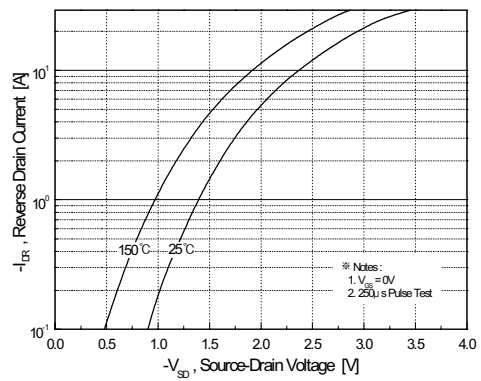


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

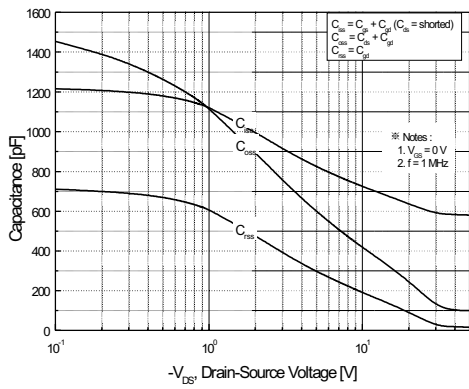


Figure 5. Capacitance Characteristics

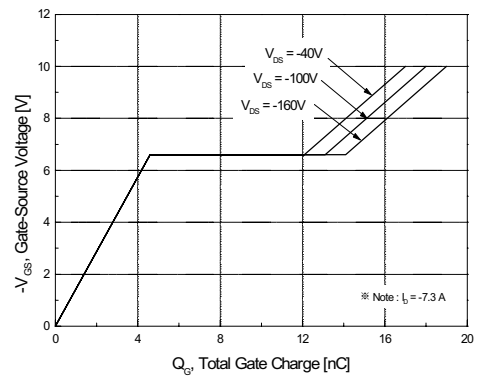


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

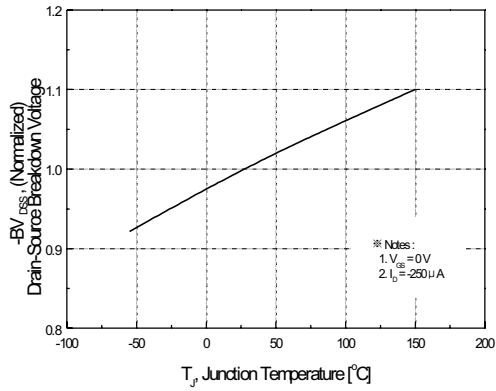


Figure 7. Breakdown Voltage Variation vs. Temperature

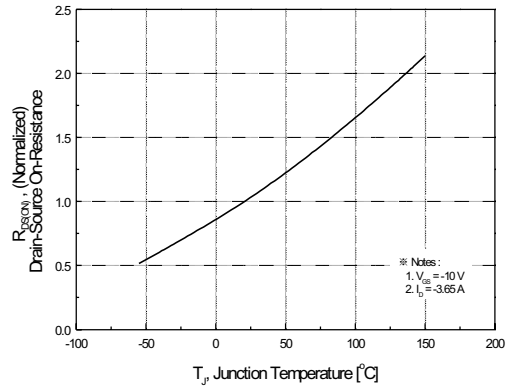


Figure 8. On-Resistance Variation vs. Temperature

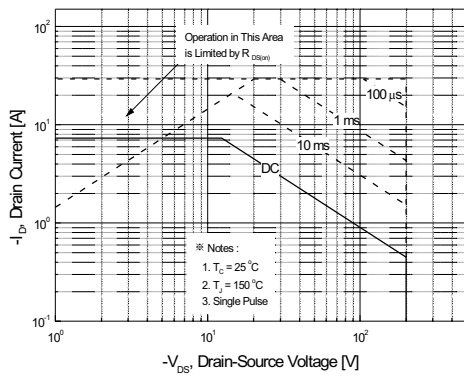


Figure 9. Maximum Safe Operating Area

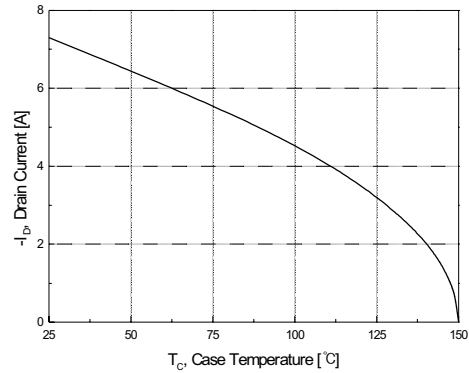


Figure 10. Maximum Drain Current vs. Case Temperature

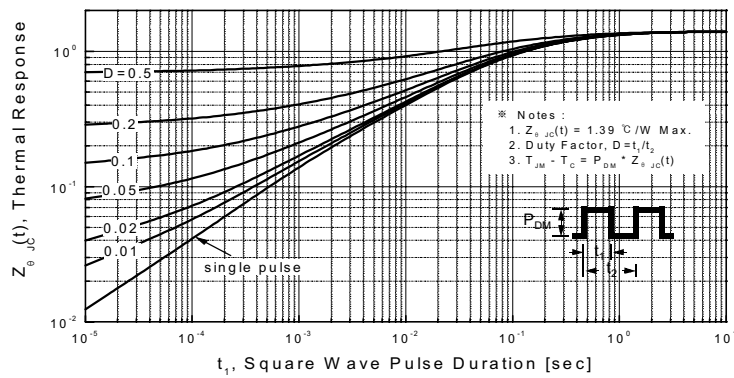
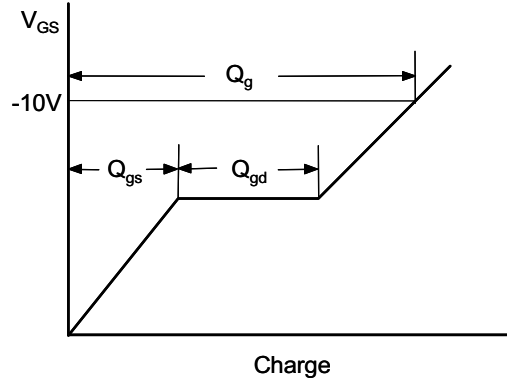
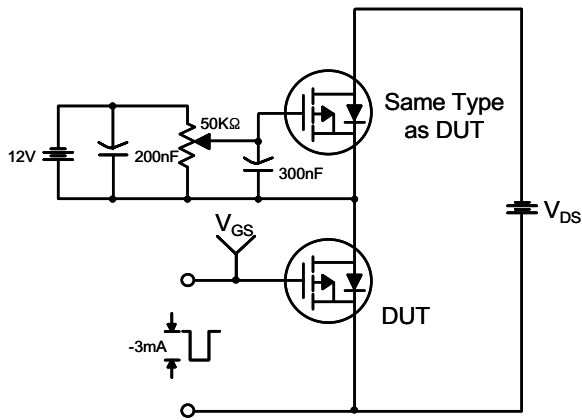
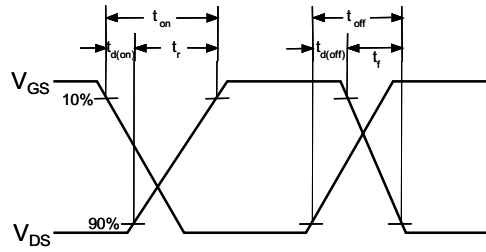
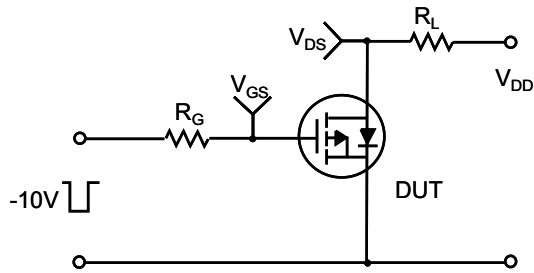


Figure 11. Transient Thermal Response Curve

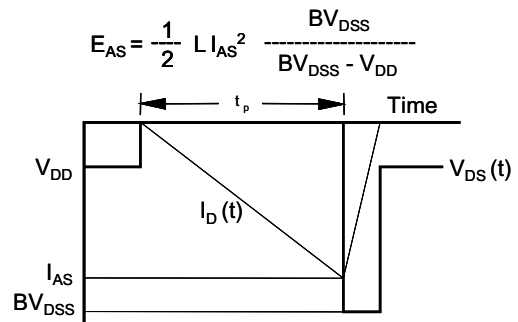
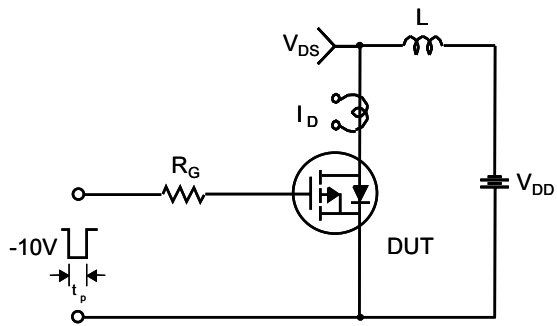
Gate Charge Test Circuit & Waveform



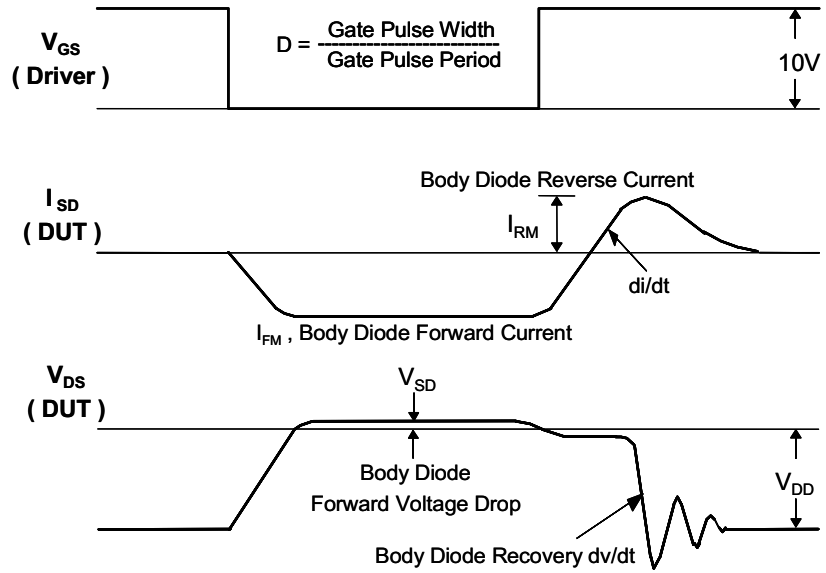
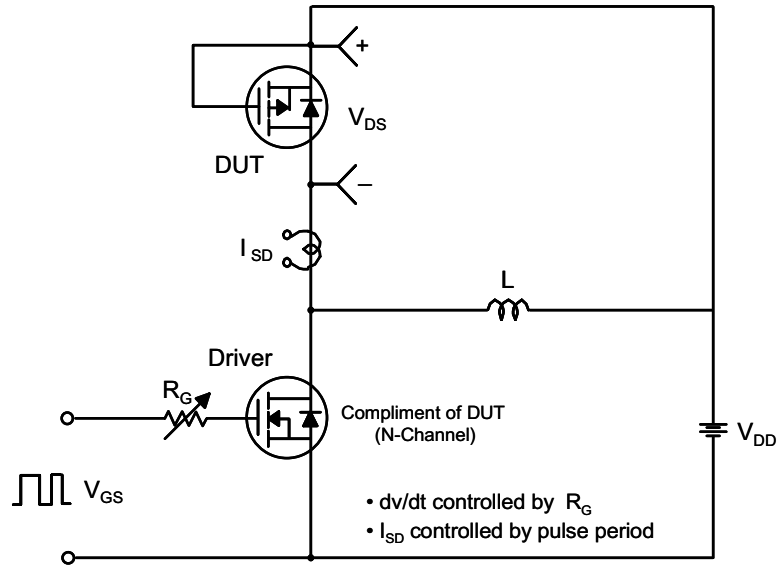
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220



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