SUMITOMO ELECTRIC

ADVANCE

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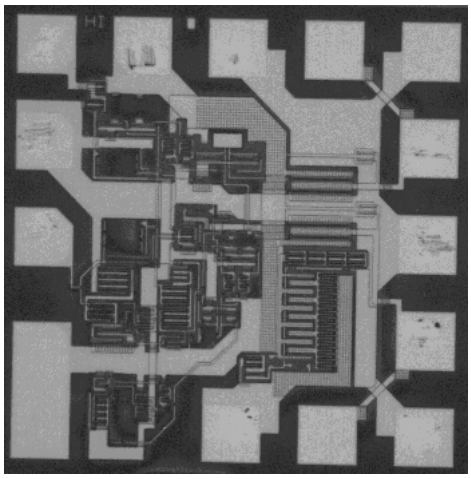
F0100209B

3.3 V /5V 622 Mb/s Receiver

Transimpedance Amplifier



♦ *Features*

- Low voltage of +3.3 V or +5.0V single power supply
- 10 kΩ high transimpedance
- 35 dB high gain
- 0 dBm large optical input
- Over 32 dB wide dynamic range
- Differential output

♦ *Applications*

- Preamplifier of an optical receiver circuit for OC-12/STM-4 (622 Mb/s)

♦ *Functional Description*

The F0100209B is a stable GaAs integrated transimpedance amplifier capable of 35 dB gain at a typical 200 MHz 3 dB-cutoff-frequency, making it ideally suited for a 622 Mb/s optical receiver circuit, for example, OC-12/STM-4, instrumentation, and measurement applications. The integrated feedback loop design provides broad bandwidth and stable operation. The F0100209B typically specifies a high transimpedance of 10 kΩ(Rs=RL=50 Ω) with a wide dynamic range of over 32 dB. It also provides a large optical input overload of more than 0dBm. Furthermore, it can operate with a low supply voltage of single +3.3 V or +5.0V. It features a typical dissipation current of 36 mA.

Only chip-shipment is available for all product lineups of GaAs transimpedance amplifiers, because the packaged preamplifier can not operate with the maximum performance owing to parasitic capacitance of the package.

♦ *Absolute Maximum Ratings*

T_a=25 °C, unless specified

Parameter	Symbol	Value	Units
Supply Voltage	$V_{DD5.0}$	V_{SS}-0.5 to V_{SS}+7.0	V
Supply Voltage	$V_{DD3.3}$	V_{SS}-0.5 to V_{SS}+5.0	V
Supply Current	I_{DD}	60	mA
Input Current	I_{IN}	3	mA
Ambient Operating Temperature	T_a	-40 to +90	° C
Storage Temperature	T_{stg}	-50 to +125	° C

♦ *Recommended Operating Conditions*

T_a=25 °C, V_{SS}=GND, unless specified

Parameter	Symbol	Value		Units
		min.	max.	
Supply Voltage	$V_{DD5.0}$	4.75	5.25	V
Supply Voltage	$V_{DD3.3}$	3.1	3.6	V
Ambient Operating Temperature	T_a	0	85	° C
Input Capacitance	C_{PD}		0.5	pF

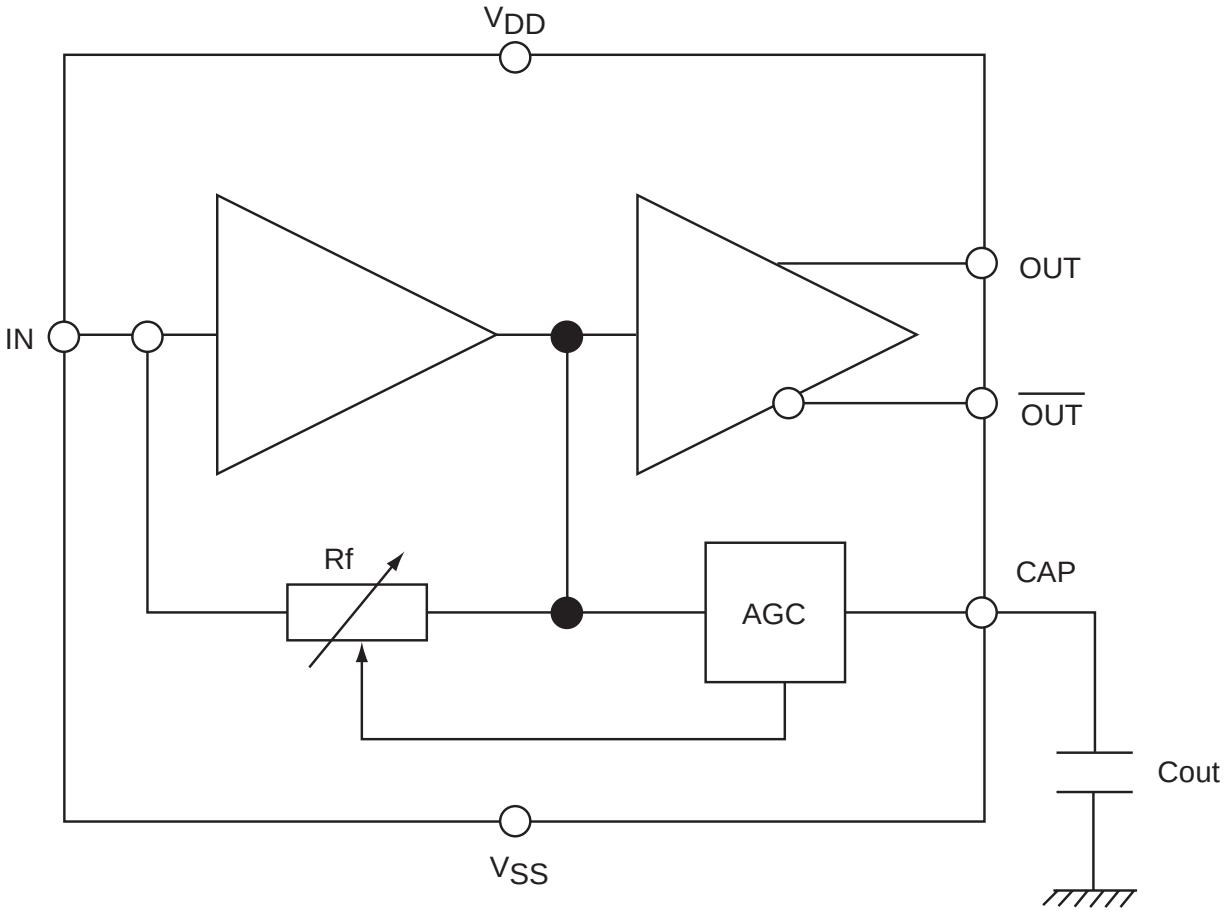
♦ *Electrical Characteristics*

T_a=25 °C, V_{DD}=3.3 V, V_{SS}= GND, unless specified

Parameter	Symbol	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Supply Current	I_{DD}	DC	-	43	-	mA
Gain(Positive)	S_{21P}	PIN=-50dBm f=1MHz, RL=50Ω	-	TBD	-	dB
Gain(negative)	S_{21N}	PIN=-50dBm f=1MHz, RL=50Ω	-	TBD	-	dB
-3dB High Frequency Cut-off (positive)	F_{CP}	PIN=-50dBm RL=50Ω	-	TBD	-	MHz
-3dB High Frequency Cut-off (negative)	F_{CN}	PIN=-50dBm RL=50Ω	-	TBD	-	MHz
Input Impedance	R_I	f=1MHz	-	280	-	Ω
Trans-Impedance(positive)	Z_{TP}*	f=1MHz RL=50Ω	-	11	-	KΩ
Trans-Impedance(negative)	Z_{TN}*	f=1MHz RL=50Ω	-	11	-	KΩ
Output Voltage(positive)	V_{OP}	DC	-	TBD	-	V
Output Voltage(negative)	V_{ON}	DC	-	TBD	-	V
Input Voltage	V_I	DC	-	0.95	-	V
AGC time constant	tagc	Cout=2200pF	-	100	-	µsec

*1 $Z_{TP,\,N} = \frac{(R_I+50)}{2} \times 10^{\frac{S_{21P,N}}{20}}$

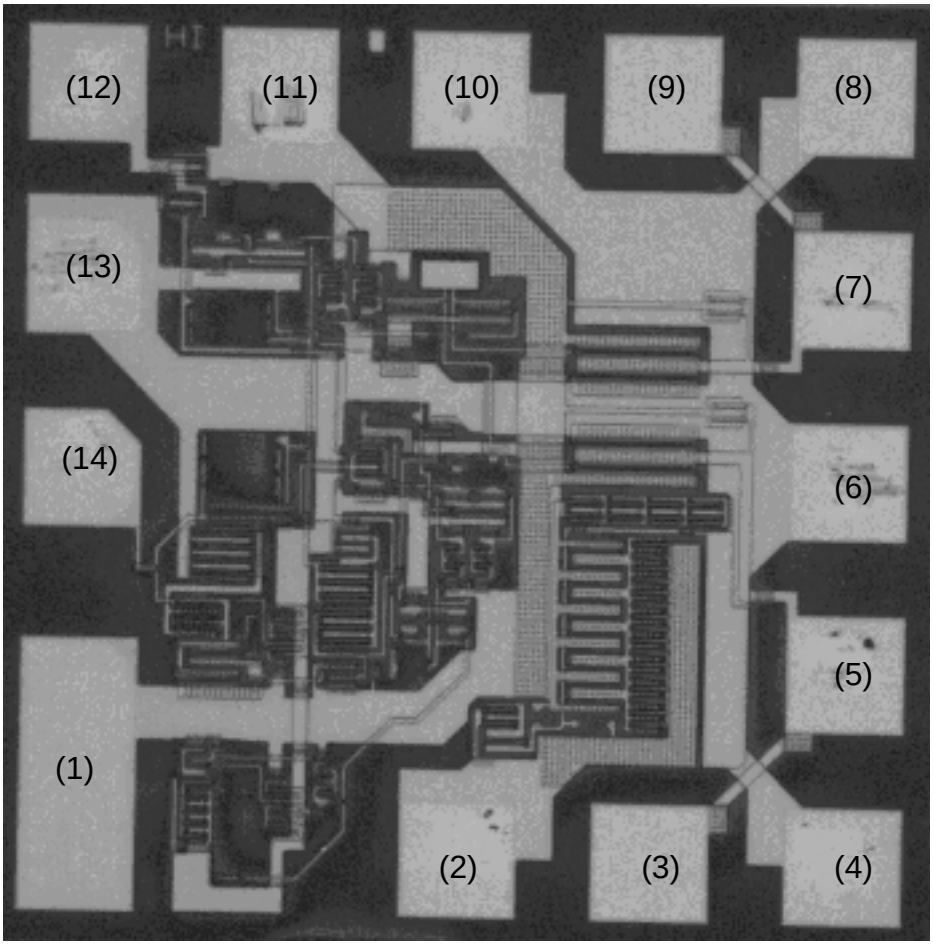
♦ *Block Diagram*



♦ *Die Pad Assignments*

V_{DD}	Supply Voltage
V_{SS}	Supply Voltage
IN	Input
OUT	Output
$\overline{OUT}$	Output
CAP	Connect outer Capasitance

♦ *Test Circuits*



No.	Symbol	Center Coordinates(μm)	No.	Symbol	Center Coordinates(μm)
(1)	$V_{DD3.3}$	(75,140)	(10)	V_{SS}	(395,715)
(2)	$V_{DD5.0}$	(395,75)	(11)	$V_{DD3.3}$	(235,715)
(3)	$\overline{OUT}$	(555,75)	(12)	CAP	(75,715)
(4)	V_{SS}	(715,75)	(13)	V_{SS}	(75,555)
(5)	$\overline{OUT}$	(715,235)	(14)	IN	(75,395)
(6)	V_{SS}	(715,395)			
(7)	OUT	(715,555)			
(8)	V_{SS}	(715,715)	O		(0,0)
(9)	OUT	(555,715)	A		(790,790)

♦ *General Description*

A transimpedance amplifier is applied as a pre-amplifier which is an amplifier for a faint photo-current from a PIN photo diode (PD). The performance in terms of sensitivity, bandwidth, and so on, obtained by this transimpedance amplifier strongly depend on the capacitance brought at the input terminal; therefore, "typical", "minimum", or "maximum" parameter descriptions can not always be achieved according to the employed PD and package, the assembling design, and other technical experts. This is the major reason that there is no product lineup of packaged transimpedance amplifiers.

Thus, for optimum performance of the transimpedance amplifier, it is essential for customers to design the input capacitance carefully.

Hardness to electro-magnetic interference and fluctuation of a power supply voltage is also an important point of the design, because very faint photo-current flows into the transimpedance amplifier. Therefore, in the assembly design of the interconnection between a PD and a transimpedance, noise should be taken into consideration.

♦ *Low Voltage Operation*

The F0100209B features a single 3.3 V supply operation, which is in great demand recently, because most of logic IC's operate with the supply voltage of 3.3 V. The analog IC's with a single 3.3 V supply for use in fiber optic communication systems are offered by only SEI.

♦ *Recommendation*

SEI basically recommends the F08 series PINAMP modules for customers of the transimpedance amplifiers. In this module, a transimpedance amplifier, a PD, and a noise filter circuit are mounted on a TO-18-can package hermetically sealed by a lens cap, having typically a fiber pigtail. The F08 series lineups are the best choice for customers to using the F01 series transimpedance amplifiers. SEI's F08 series allows the customers to resolve troublesome design issues and to shorten the development lead time.

♦ *Noise Performance*

The F0100209B based on GaAs FET's shows excellent low-noise characteristics compared with IC's based on the silicon bipolar process. Many transmission systems often demand superior signal-to-noise ratio, that is, high sensitivity; the F0100209B is the best

choice for such applications.

The differential circuit configuration in the output enable a complete differential operation to reduce common mode noise: simple single ended output operation is also available.

♦ *Die-Chip Description*

The F0100209B is shipped like the die-chip described above. The die thickness is typically 280 μm ± 20 μm with the available pad size uncovered by a passivation film of 95 μm square. The material of the pads is TiW/Pt/Au and the backside is metalized by Ti/Au.

♦ *Assembling Condition*

SEI recommends the assembling process as shown below and affirms sufficient wire-pull and die-shear strength. The heating time of one minute at the temperature of 310 °C gave satisfactory results for die-bonding with AuSn performs. The heating and ultrasonic wire-bonding at the temperature of 150 °C by a ball-bonding machine is effective.

♦ *Quality Assurance*

For the F01 series products, there is only one technically inevitable drawback in terms of quality assurance which is to be impossible of the burn-in test for screening owing to die-shipment. SEI will not ship them if customers do not agree on this point. On the other hand, the lot assurance test is performed completely without any problems according to SEI's authorized rules. A microscope inspection is conducted in conformance with the MIL-STD-883C Method 2010.7.

♦ *Precautions*

Owing to their small dimensions, the GaAs FET's from which the F0100209B is designed are easily damaged or destroyed if subjected to large transient voltages. Such transients can be generated by power supplies when switched on if not properly decoupled. It is also possible to induce spikes from static-electricity-charged operations or ungrounded equipment.