Data Sheet June 14, 2004 FN7198.1

Quad 12MHz Rail-to-Rail Input-Output Buffer

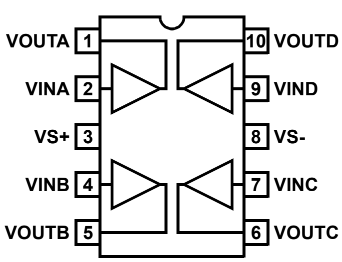
The EL5421 is a quad, low power, high voltage rail-to-rail input-output buffer. Operating on supplies ranging from 5V to 15V, while consuming only 500µA per channel, the EL5421 has a bandwidth of 12MHz (-3dB). The EL5421 also provides rail-to-rail input and output ability, giving the maximum dynamic range at any supply voltage.

The EL5421 also features fast slewing and settling times, as well as a high output drive capability of 30mA (sink and source). These features make the EL5421 ideal for use as voltage reference buffers in Thin Film Transistor Liquid Crystal Displays (TFT-LCD). Other applications include battery power, portable devices and anywhere low power consumption is important.

The EL5421 is available in a space saving 10-pin MSOP package and operates over a temperature range of -40°C to +85°C.

Pinout

EL 5421
(10-PIN MSOP)
TOP VIEW



Features

- 12MHz -3dB bandwidth
- Unity gain buffer
- Supply voltage = 4.5V to 16.5V
- Low supply current (per buffer) = 500µA
- High slew rate = 10V/µs
- Rail-to-rail operation
- “Mini” SO package (MSOP)
- Pb-free package available

Applications

- TFT-LCD drive circuits
- Electronics notebooks
- Electronics games
- Personal communication devices
- Personal digital assistants (PDA)
- Portable instrumentation
- Wireless LANs
- Office automation
- Active filters
- ADC/DAC buffers

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5421CY	10-Pin MSOP	-	MDP0043
EL5421CY-T7	10-Pin MSOP	7”	MDP0043
EL5421CY-T13	10-Pin MSOP	13”	MDP0043
EL5421CYZ (Note)	10-Pin MSOP (Pb-Free)	-	MDP0043
EL5421CYZ-T7 (Note)	10-Pin MSOP (Pb-Free)	7”	MDP0043
EL5421CYZ-T13 (Note)	10-Pin MSOP (Pb-Free)	13”	MDP0043

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . . +18V
Input Voltage . . . . V_S- -0.5V, V_S+ +0.5V
Maximum Continuous Output Current 30mA
Maximum Die Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C
Operating Temperature . . . . -40°C to +85°C
Power Dissipation . . . . See Curves

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = 25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	12	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	-4.5V ≤ V_{OUT} ≤ 4.5V	0.995		1.005	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.92	-4.85	V
V_{OH}	Output Swing High	I_L = 5mA	4.85	4.92		V
I_{SC}	Short Circuit Current	Short to GND (Note 2)	±80	±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current (Per Buffer)	No load		500	750	µA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%	7	10		V/µs
t_S	Settling to +0.1%	V_O = 2V step		500		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

1. Measured over the operating temperature range
2. Parameter is guaranteed (but not test) by design and characterization data
3. Slew rate is measured on rising and falling edges

Electrical Specifications

$V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 2.5V, $T_A = 25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		2	10	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	$0.5 \le V_{OUT} \le 4.5V$	0.995		1.005	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		80	150	mV
V_{OH}	Output Swing High	$I_L = 5mA$	4.85	4.92		V
I_{SC}	Short Circuit Current	Short to GND (Note 2)	±80	±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Buffer)	No load		500	750	µA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUT} \le 4V$, 20% to 80%	7	10		V/µs
t_S	Settling to +0.1%	$V_O = 2V$ step		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

1. Measured over the operating temperature range
2. Parameter is guaranteed (but not test) by design and characterization data
3. Slew rate is measured on rising and falling edges

Electrical Specifications

V_S+ = +15V, V_S- = 0V, R_L = 10kΩ and C_L = 10pF to 7.5V, T_A = 25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		2	14	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	$0.5 \le V_{OUT} \le 14.5V$	0.995		1.005	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		80	150	mV
V_{OH}	Output Swing High	I_L = 5mA	14.85	14.92		V
I_{SC}	Short Circuit Current	Short to GND (Note 2)	±80	±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Buffer)	No load		500	750	µA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUT} \le 14V$, 20% to 80%	7	10		V/µs
t_S	Settling to +0.1%	V_O = 2V step		500		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

NOTES:

1. Measured over the operating temperature range
2. Parameter is guaranteed (but not test) by design and characterization data
3. Slew rate is measured on rising and falling edges

Typical Performance Curves

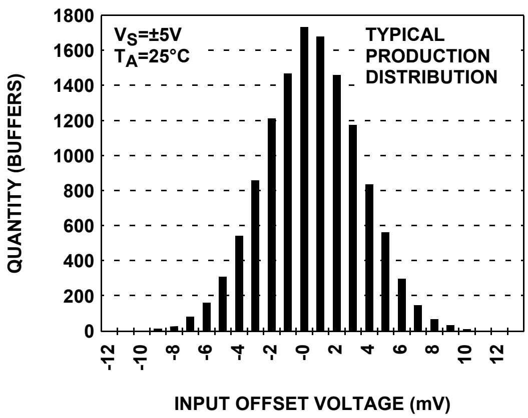


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

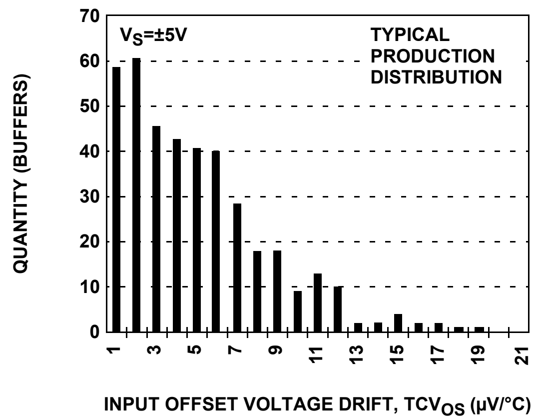


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT

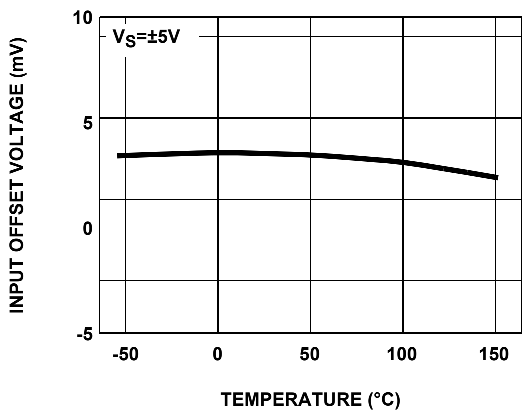


FIGURE 3. INPUT OFFSET VOLTAGE vs TEMPERATURE

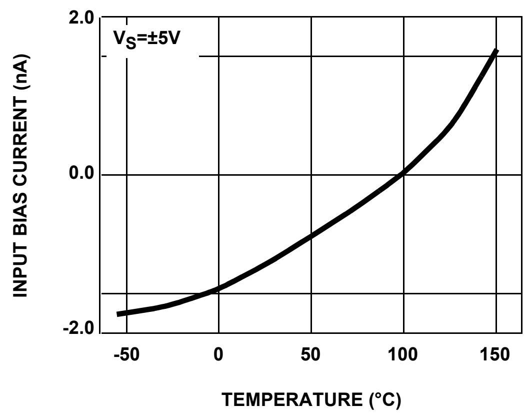


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

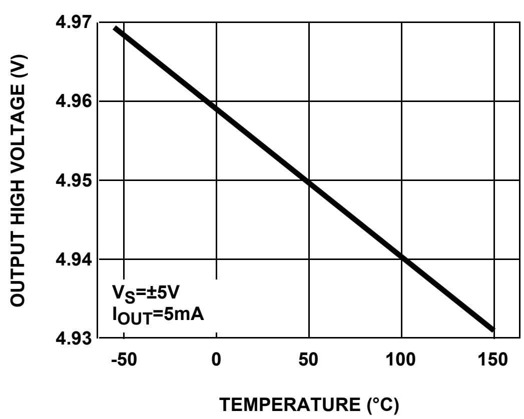


FIGURE 5. OUTPUT HIGH VOLTGE vs TEMPERATURE

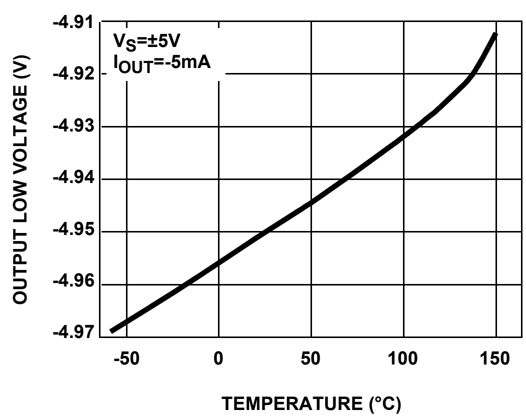


FIGURE 6. OUTPUT LOW VOLTAGE vs TEMPERATURE

Typical Performance Curves

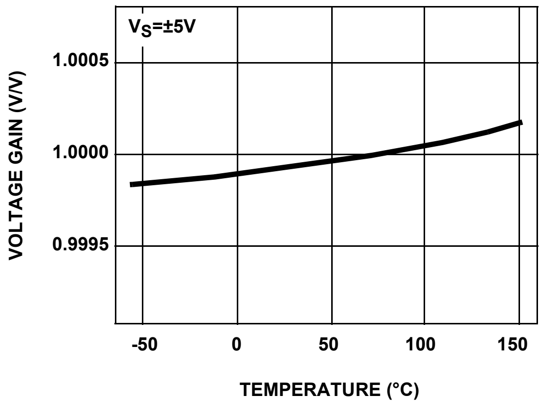


FIGURE 7. VOLTAGE GAIN vs TEMPERATURE

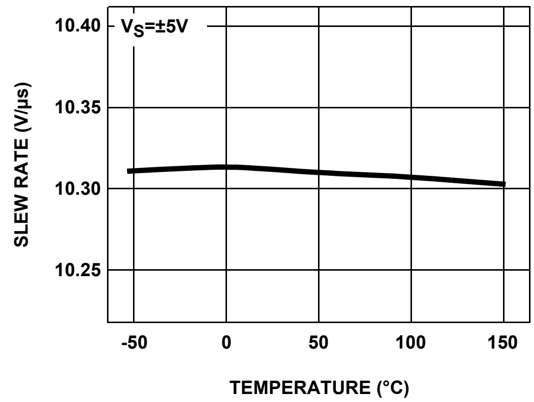


FIGURE 8. SLEW RATE vs TEMPERATURE

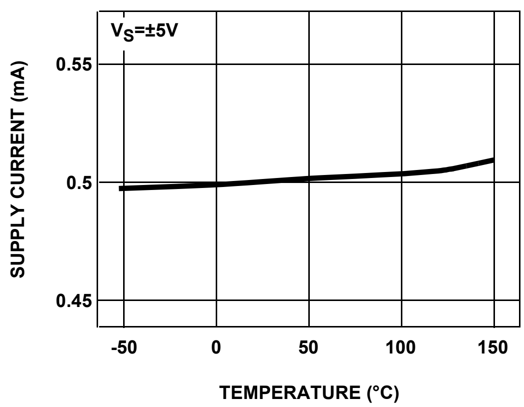


FIGURE 9. SUPPLY CURRENT PER CHANNEL vs TEMPERATURE

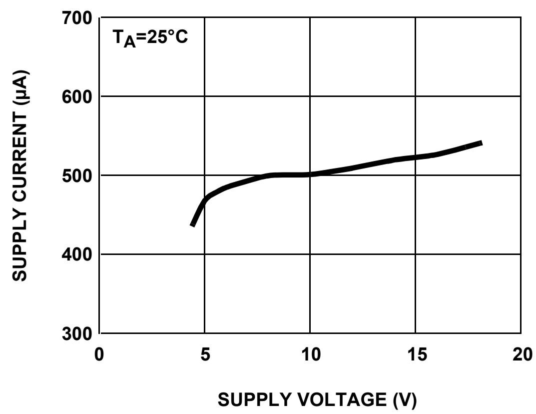


FIGURE 10. SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE

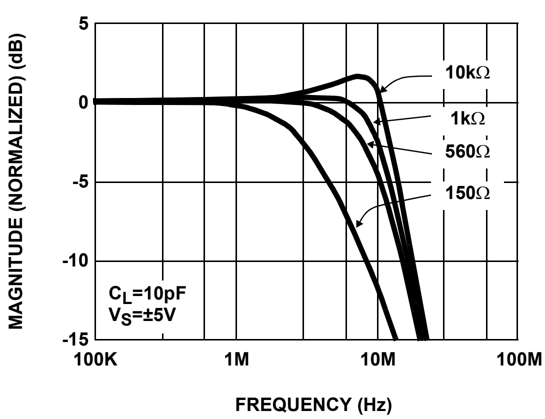


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS R_L

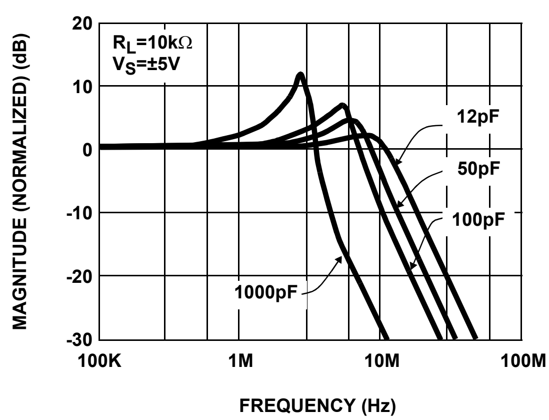


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS C_L

Typical Performance Curves

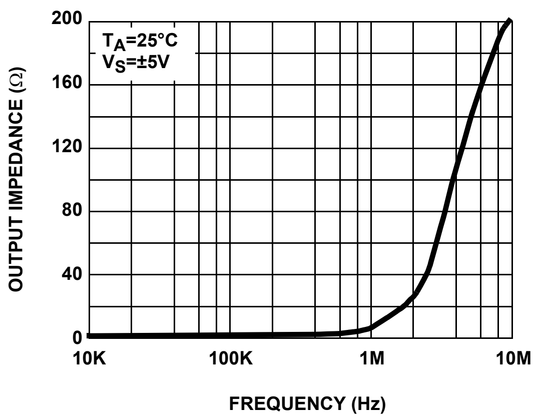


FIGURE 13. OUT PUT IMPEDANCE vs FREQUENCY

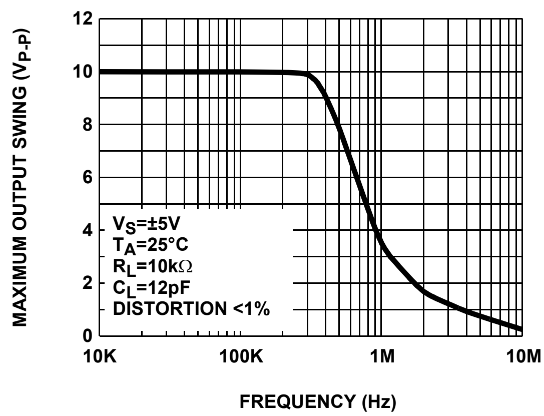


FIGURE 14. MAXIMUM OUTPUT SWING vs FREQUENCY

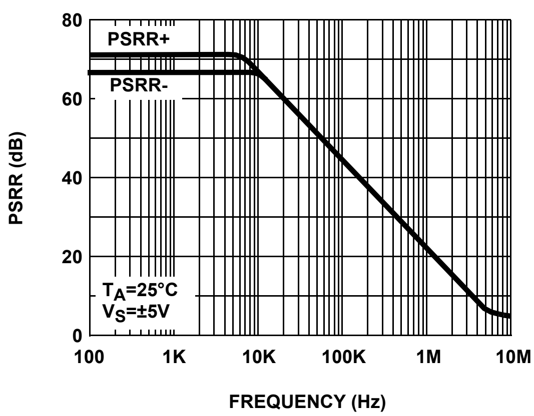


FIGURE 15. PSRR vs FREQUENCY

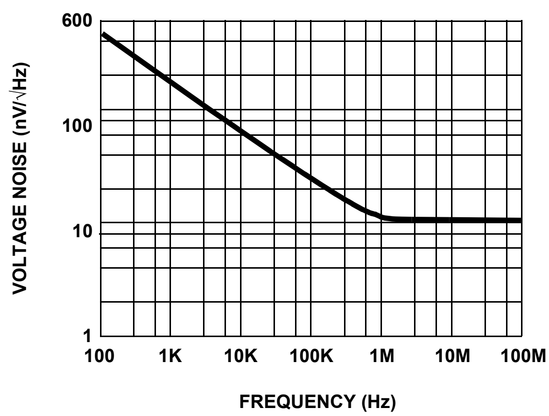


FIGURE 16. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

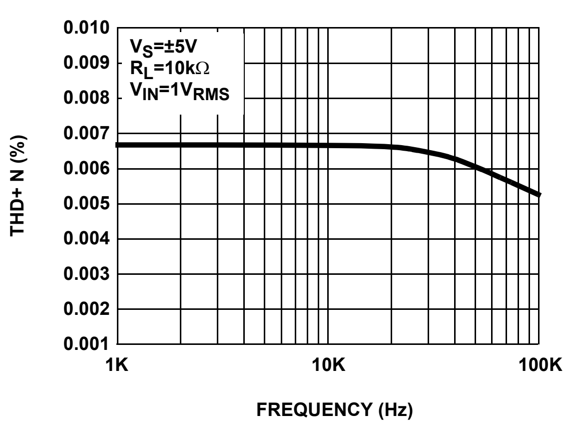


FIGURE 17. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

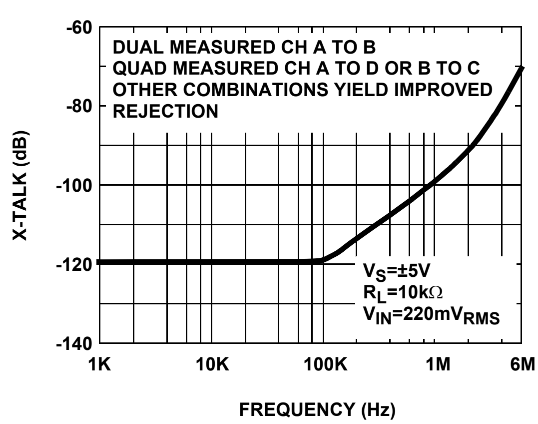


FIGURE 18. CHANNEL SEPARATION vs FREQUENCY RESPONSE

Typical Performance Curves

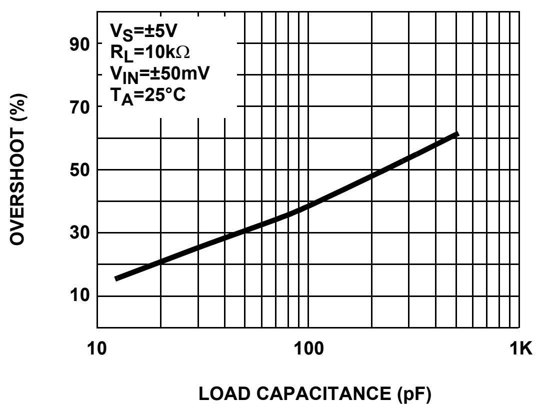


FIGURE 19. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

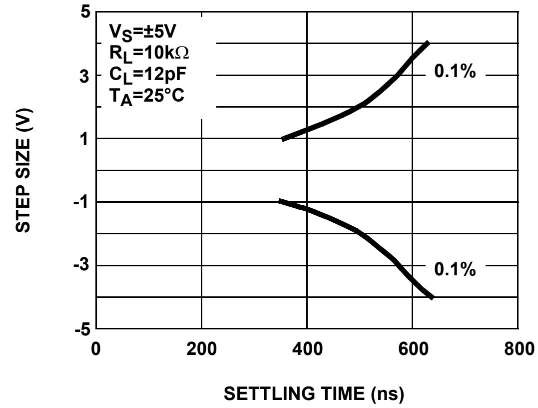


FIGURE 20. SETTLING TIME vs STEP SIZE

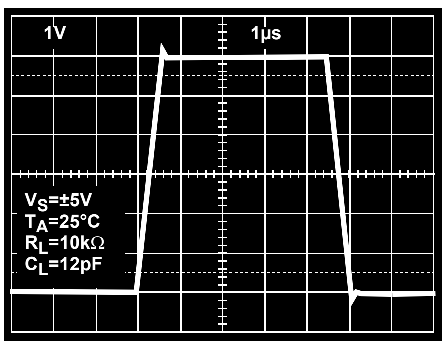


FIGURE 21. LARGE SIGNAL TRANSIENT RESPONSE

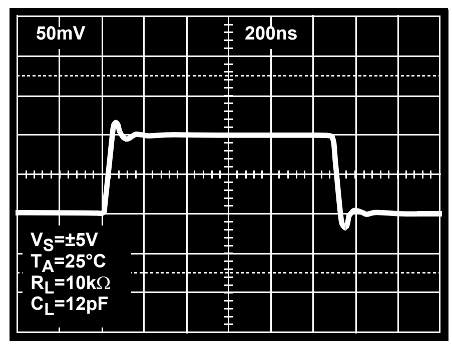
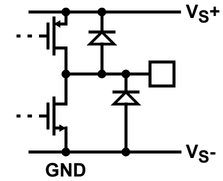
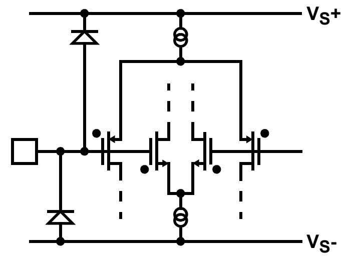


FIGURE 22. SMALL SIGNAL TRANSIENT REPOSNE

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUTA	Buffer A Output	 CIRCUIT 1
2	VINA	Buffer A Input	 CIRCUIT 2
3	VS+	Positive Power Supply	
4	VINB	Buffer B Input	(Reference Circuit 1)
5	VOUTB	Buffer B Output	(Reference Circuit 2)
6	VOUTC	Buffer C Output	(Reference Circuit 2)
7	VINC	Buffer C Input	(Reference Circuit 1)
8	VS-	Negative Power Supply	
9	VIND	Buffer D Input	(Reference Circuit 2)
10	VOUTD	Buffer D Output	(Reference Circuit 1)

Applications Information

Product Description

The EL5421 unity gain buffer is fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability, and has low power consumption (500µA per buffer). These features make the EL5421 ideal for a wide range of general-purpose applications. When driving a load of 10kΩ and 12pF, the EL5421 has a -3dB bandwidth of 12MHz and exhibits 10V/µs slew rate.

Operating Voltage, Input, and Output

The EL5421 is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5421 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The output swings of the EL5421 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 23 shows the input and output waveforms for the device. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.985V_{P-P}$.

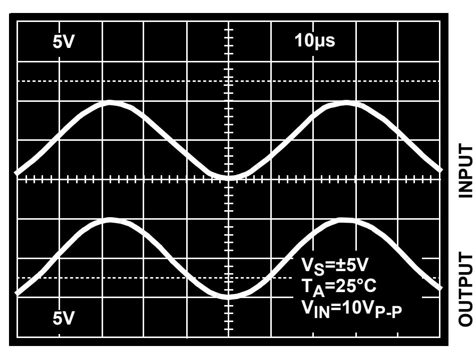


FIGURE 23. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5421 will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5421 is immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 24 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

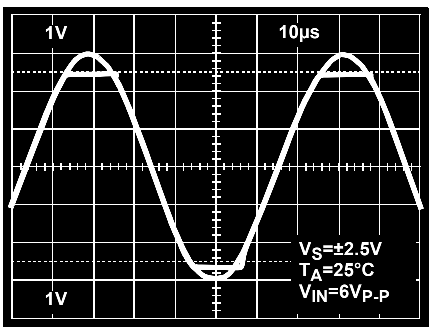


FIGURE 24. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5421 buffer, it is possible to exceed the 125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT} i) \times I_{LOAD} i]$$

when sourcing, and:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT} i - V_S -) \times I_{LOAD} i]$$

when sinking.

Where:

i = 1 to 4 for quad

V_S = Total supply voltage

I_{SMAX} = Maximum supply current per channel

$V_{OUT}i$ = Maximum output voltage of the application

$I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figures 25 and 26 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figures 25 and 26.

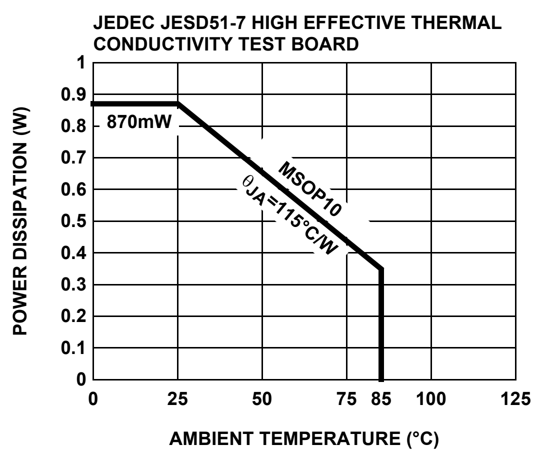


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

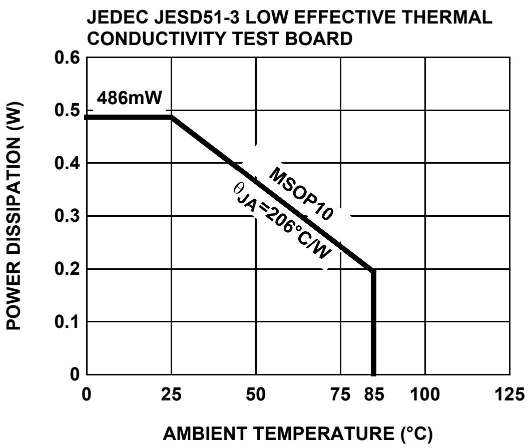


FIGURE 26. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

Unused Buffers

It is recommended that any unused buffer have the input tied to the ground plane.

Driving Capacitive Loads

The EL5421 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The buffers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain

Power Supply Bypassing and Printed Circuit Board Layout

The EL5421 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ to pin to V_S- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the buffer. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.