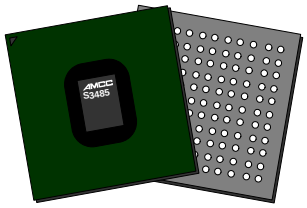


S3485

SONET/SDH/FEC/FC/GE/HDTV/DTV/D1/ESCON Multirate 4-bit Transceiver

Features

- Operational from 2.00 Gbps to 3.00 Gbps
- Supports:
  - OC-48 with or w/o FEC
  - OC-24 with or w/o FEC
  - OC-12 with or w/o FEC
  - OC-3 with or w/o FEC
  - HDTV (1.485 Gbps)
  - D1 (1.38 Gbps)
  - Fibre Channel (1062 Mbps)
  - 2 x Fibre Channel (2.124 Gbps)
  - Gigabit Ethernet (1.25 Gbps)
  - DTV (143.18 Mbps)
  - ESCON (200 Mbps)
- Low Power (300 mW Typical)
- Built-In Self Test (BIST) Feature
- 121 pin PBGA package with Green/RoHS compliant lead free option
- On-chip High-Frequency PLL for Clock Generation and Clock Recovery
- 4-bit LVDS Parallel Data Path
- TX and RX Lock Detect Indication
- Serial Loop Timing Mode
- Line and Diagnostic Loopback Mode for Faulty Node Identification
- Operational Temperature Range Up to 85°C
- Dual 1.2 V and 1.8 V supply
- Complies with OIF SFI-4/Telecordia/ITU-T Specifications

Transmitter Features

- Reference frequency of 155.52 MHz (or equivalent rate)
- 155.52 MHz (or equivalent rate) clock output
- Internal, self-initializing FIFO to decouple transmit clocks

Receiver Features

- Recovers clock from 2.00 to 3.00 Gbps
- Low-jitter CML differential or single-ended serial interface
- Reference frequency of 155.52 MHz (or equivalent rate)

Applications

- SONET/SDH-based transmission systems
- SONET/SDH modules
- Wavelength Division Multiplexing (WDM)
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber Optic Terminators
- Fiber Optic Test Equipment

Description

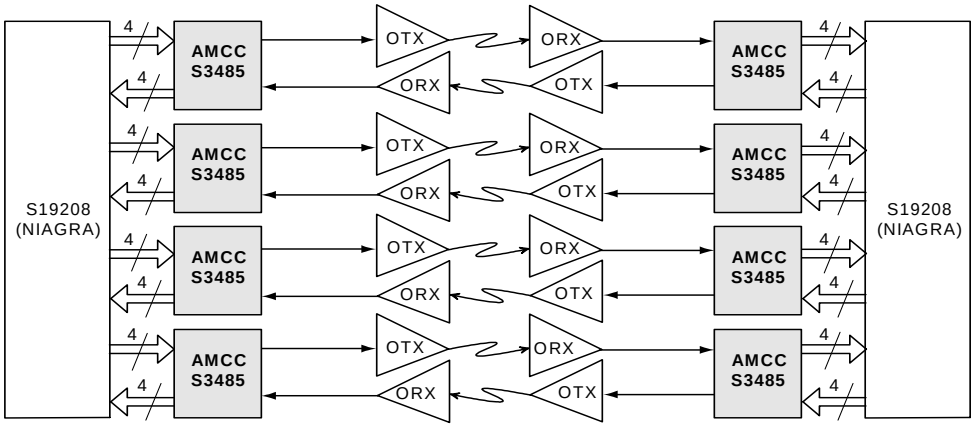
The S3485 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET multi-rate interface device. The S3485 receives a scrambled Non-Return-to-Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with the SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 transmission standards. The device is suitable for SONET-based WDM applications. The diagram in Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase-Lock Loop (PLL) on the S3485 transceiver chip, allowing the use of a slower external transmit clock reference. The chip can be used with a divide by 16 reference clock in support of existing system clocking schemes.

The low-jitter parallel LVDS interface is compliant with the bit-error rate requirements of the Telecordia and ITU-T standards. The S3485 is packaged in a 121 PBGA offering designers a small package outline.

Overview

The S3485 transceiver implements SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 serialization/deserialization and transmission functions. This chip can be used to implement the front end of SONET/ SDH/ Gigabit Ethernet/ Fibre Channel/ HDTV/ ESCON/ DTV/ D1 equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of data stream management and clock distribution throughout the front end. Of the listed bit rates, only the associated SONET/SDH, Fibre Channel and Gigabit Ethernet protocols have been validated to their respective standards. AMCC has characterized the remaining bit rates with a PRBS 2^{31} pattern but has not validated their associated protocols against any known standard. It is the responsibility of the end user to evaluate and verify protocol/standards compliance for all other bits rates that are intend for use.



System Block Diagram with the S3485

S3485

AMCC Suggested Interface Devices

Ganges (S19202)	STS-192 POS/ATM SONET/SDH Mapper
Niagara (S19208)	STS-192/48/12/3 DW/FEC/PM and ASYNC Mapper Device
Danube (S4805)	SONET/SDH STS-48/STM-16 Framer/Pointer Processor
Ohio (S4806)	STS-48/STM-16 SONET/SDH Framer and ATM/POS Mapper

The sequence of operations is as follows:

Transmitter Operations

- 4-bit parallel input
- Parallel-to-serial conversion
- Serial data output

Receiver Operations

- Serial input
- Clock and Data recovery
- Serial-to-parallel conversion
- 4-bit parallel data and clock output

Internal clocking and control functions are transparent to the user.

AMCC
6290 Sequence Dr.
San Diego, CA 92121
P 858 450 9333
F 858 450 9885
www.amcc.com

S3485_PB0832_v2.02_20061031