C32025
Digital Signal Processor Megafunction

General Description

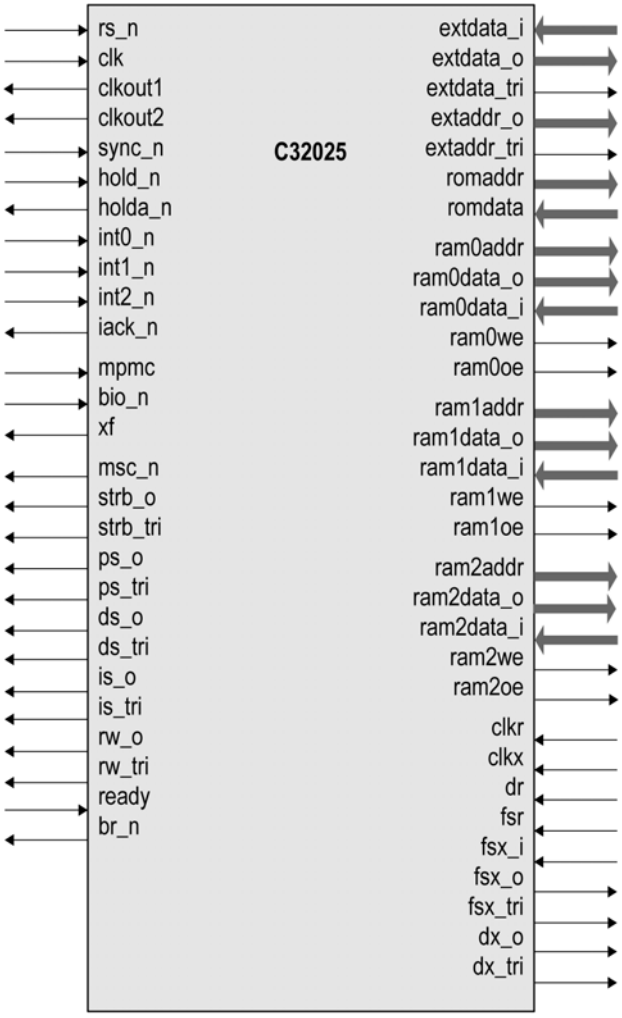
The C32025 is a 16-bit fixed-point digital signal processor core. It combines the flexibility of a high-speed controller with the numerical capability of an array processor. The C32025 has the same instruction set as the TMS320C25 and also provides the same interrupts, serial interface and timer.

Developed for easy reuse with ASICs or FPGAs, the core requires under 18000 ASIC gates.

Applications

- Digital sound processing (adaptive filtering, FFT, other special sound effects)
- Voice recognition
- Telecommunications (modems, codecs)
- Medical equipment (diagnostics tools)
- Computers peripherals
- Various embedded data-intensive systems

Symbol



Features

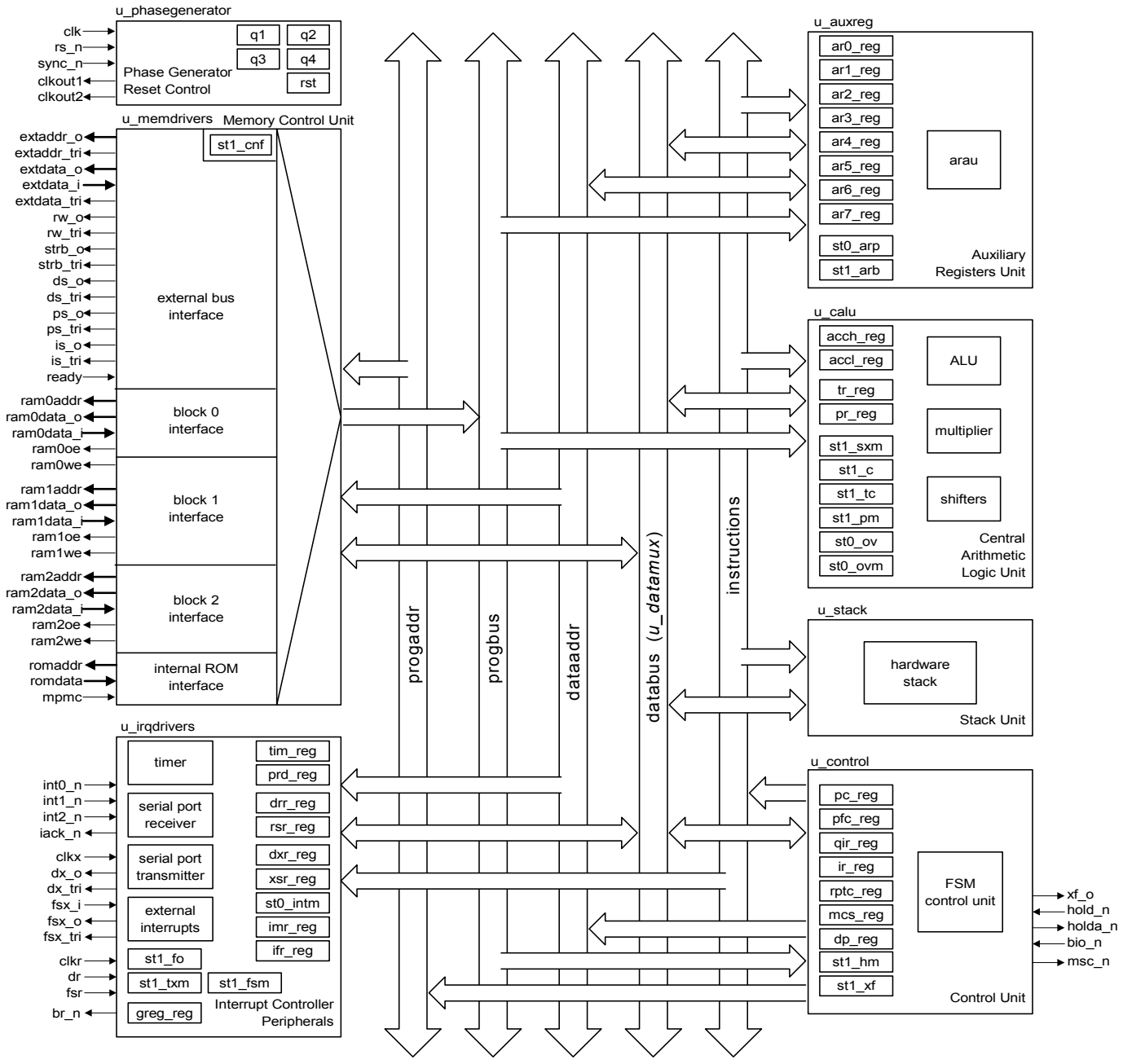
- Control Unit
  - 16-bit instruction decoding
  - Repeat instructions for efficient use of program space and enhanced execution
- Central Arithmetic-Logic Unit
  - 16-bit parallel shifter; 32-bit arithmetic and logical operations
  - 16 x 16 bit parallel multiplier with a 32-bit product
  - 32-bit accumulator with output shifter
  - Single-cycle Multiply-and-Accumulate instructions
- Auxiliary Registers
  - 8 16-bit registers for indirect addressing or temporary data storage
  - 16-bit Auxiliary Register Arithmetic Unit including operations with reversed-carry propagation
- Memory addressing modes
  - Direct - using a 9-bit Page Pointer and instruction word's lowest 7-bits
  - Indirect – using the Auxiliary Register File
  - Immediate – less than 16-bit via instruction word or full 16-bit long immediate following the instruction word
  - Block moves for data/program management
- 8-level Hardware Stack
- Interrupt Controller: 6 interrupt sources, excluding reset and a software interrupt
- Synchronous serial port for direct codec interface
- 16-bit reload timer
- Program Memory organization
  - 4K-words of internal ROM
  - Internal 256-word RAM block configurable either as program or data space
  - 64K-word external program space
- Data Memory organization
  - 2 Internal 256-word and one 32-word RAM blocks
  - 64K-words of external data space
  - 6 memory mapped registers
- 16 Input and 16 Output channels
- Wait states for interfacing slower off-chip devices
- Multiprocessing support
  - Global data memory interface
  - Synchronization input for synchronous multiprocessor configurations
- Concurrent DMA using an extended Hold operation
- Design is strictly synchronous with positive-edge clocking and synchronous reset, no internal tri-states.

Pin Description

Name	Type	Polarity/ Bus size	Description
clk	I	Rise	**Master clock input** All internal synchronous circuits clock
clkout1	O	-	**Master clock output** (fclk/4) When High it indicates internal quarter-phases Q3 and Q4
clkout2	O	-	**Second clock output** (fclk/4) When High it indicates internal quarter-phases Q2 and Q3
rs_n	I	Low	**Hardware reset input** Active for 2 cycles resets the device
mpmc	I	-	**Microprocessor/microcomputer mode** When Low the internal ROM is mapped into program space
sync_n	I	Fall	**Synchronization input** Forces the internal quarter-phase to Q1
hold_n	I	Low	**Hold input** Forces processor to place the data & address buses and control lines in the hi-Z state
holda_n	O	Low	**Hold acknowledge output** Indicates that processor is in the hold mode
int0_n int1_n int2_n	I I I	Low/Fall Low/Fall Low/Fall	**External interrupt input**s External interrupt 0 External interrupt 1 External interrupt 2
iack_n	I	Low	**Interrupt acknowledge** Indicates branching to the interrupt vector
ps_o ds_o is_o	O O O	Low Low Low	**Program, data and I/O space select signals**
ps_tri ds_tri is_tri	O O O	High High High	**Select signals tri-state control** Enables external tri-state buffers
rw_o	O	-	**Read/write output signal** Indicates external transfer direction. High means reading
rw_tri	O	H	**Read/write tri-state control** Enables external tri-state buffer
strb_o	O	Low	**Strobe signa**l Low indicates an external bus cycle
strb_tri	O	High	**Strobe tri-state control signal** Enables external tri-state buffer
ready	I	High	**Data ready input** Indicates that external device is prepared for transfer to be completed
bio_n	I	Low	**Branch control inpu**t When active the BIOZ branch occurs
br_n	O	Low	**Bus request output** Asserted when the processor requires access to external global data memory space

Name	Type	Polarity/ Bus size	Description
msc_n	O	Low	**Microstate complete output** Indicates a completion of a memory operation
xf	O	-	**External flag output** General purpose output pin
clkr	I	Fall	**Receive clock input**
clkx	I	Rise	**Transmit clock input**
dr	I	-	**Serial data receive input** Data clocked by clkr
dx_o	O	-	**Serial data transmit output**
dx_tri	O	High	**Serial transmit tri-state control** Active only while transmitting
fsr	I	Fall	**Frame synchronization pulse for receive input**
fsx_i	I	Fall	**Frame synchronization pulse for transmit input**
fsx_o	O	Fall	**Frame synchronization pulse for transmit output**
fsx_tri	O	High	**Frame synchronization pulse for transmit tri-state control**
			External Program/ Data/ IO interface
extaddr_o	O	16	Address bus output
extaddr_tri	O	High	Address tri-state control
extdata_i	I	16	Data bus input
extdata_o	O	16	Data bus output
extdata_tri	O	High	Data bus tri-state control
			Internal Program Memory interface
romdata	I	16	Data input
romaddr	O	12	Address output
			Internal RAM 0 interface
ram0data_i	I	16	Data bus input
ram0data_o	O	16	Data bus output
ram0addr	O	8	Data file address
ram0we	O	High	Data file write enable
ram0oe	O	High	Data file output enable
			Internal RAM 1 interface
ram1data_i	I	16	Data bus input
ram1data_o	O	16	Data bus output
ram1addr	O	8	Data file address
ram1we	O	High	Data file write enable
ram1oe	O	High	Data file output enable
			Internal RAM 2 interface
ram2data_i	I	16	Data bus input
ram2data_o	O	16	Data bus output
ram2addr	O	5	Data file address
ram2we	O	High	Data file write enable
ram2oe	O	High	Data file output enable

Block Diagram



C32025 Block Diagram

Functional Description

The C32025 core is partitioned into modules as described below.

Control Unit

Control unit consists of Program Counter (PC) and Prefetch Counter (PFC) used for program addressing and pipelining. Sequencer is responsible for data flow organization. Repeat Counter (RPTC) is used to repeat the execution of several instructions, especially data-intensive ones.

Memory Control Unit

It is an interface between the processor and all on-chip or off-chip memories. There are three internal RAM blocks interfaces, internal ROM interface and external address and data buses. External wait states are possible.

Central Arithmetic Logic Unit

Central Arithmetic-Logic Unit. (CALU) performs:

- Sign-extended shifting
- 32-bit arithmetic operations
- 32-bit logic operations
- 16-bit signed or unsigned multiplication

Auxiliary Registers Unit

Eight auxiliary registers are used for indirect data addressing or temporary data storage. Auxiliary Registers Arithmetic Unit performs operations on current auxiliary register after each indirect data memory read/write.

Stack Unit

Eight level hardware stack for PC storage during subroutine calls and interrupt service.

Peripherals

There is one 16-bit continuously operating timer with programmable period. Synchronous full-duplex serial interface can be used for interfacing serial AD/DA converters and codecs.

Interrupt Controller

There are three external interrupts, both edge and level triggered. Internal interrupt is generated at timer underflow or serial port transmit/receive completion. Those six interrupts are maskable using Interrupt Mask Register (IMR). There is also one non-maskable software interrupt.

Phase Generator

Internal clock cycle divider. Machine cycle consists of four main clock cycles.

Reset Control

Reset input is sampled once a machine cycle and distributed all over the core.

Device Utilization & Performance

Supported Family	Device Tested	Utilization			Performance F_{max}
		LEs	Memory	DSP	
Flex[2]	EPF10K100E-1	4532	M4Ks; 1 M512	1	24 MHz
Acex[2]	EP1K100E-1	4532	M4Ks; 1 M512	1	26 MHZ
Apex[1]	EP20K200E-1	4420	19 ESBs	-	37 MHz
Apex2[1]	EP2A15-7	4528	19 ESBs	-	65 MHz
Cyclone[1]	EP1C6-6	4066	37 ESBs	-	95 MHz
Stratix[1]	EP1S10-5	4370	7 EABs	-	101 MHz
Startix2[1]	EP2S15-3	3835	7 EABs	-	130 MHz

Notes:
1. Implemented with 544x16 bit RAM and 4096 x 16 bit ROM
2. Implemented with 544x16 bit RAM and 1048 x 16 bit ROM

Core Assumptions

The IACK_N and MSC_N lines are valid only during the quarter-phases Q1 and Q2 (when CLKOUT1 = 0). In other cases their behaviour is unpredictable in the original Texas Instruments TMS320C25 device. The C32025 sets them to 1s in Q3 and Q4, except in the hold mode when MSC_N remains 0.

The original Texas Instruments TMS320C25 serial port doesn't re-start properly when a frame sync pulse occurs in the middle of a transmission. The new transfer following a re-start is interrupted in a moment when previous transmission should be completed as if and there were no frame sync pulses, but the transferred data is re-loaded. The C32025 serial interface works properly as it is described in the specification document.

The CLKR and CLKX inputs are clock inputs in the original Texas Instruments TMS320C25 serial port registers. In C32025 they are not clock signals but are synchronously sampled at every positive edge of the main clock signal. The same applies to the external interrupts inputs INT0_N, INT1_N and INT2_N. They are connected to a negative edge flip-flop in the original device, but in C32025 they are sampled synchronously with main clock signal. These changes cause delays in the serial port operation and forces the minimum

length of an external interrupt pulse to at least one oscillator cycle.

Some registers are not reset by RS_N in the original Texas Instruments TMS320C25 device, but are reset in the C32025. They are:

ACC 00000000h

PR 00000000h

TR 0000h

ARP 000

ARB 000

DP 000000000

IMR 000000

DRR 0000h

DXR 0000h

Stack all levels are reset to 0000h

OVM 0

TC 0

AR0-AR7 all registers are reset to 0000h

Verification Methods

The C32025 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Texas Instruments TMS320C25 chip, and the results compared with the core's simulation outputs.

Development Environment

- VHDL source code for the C32025
- Synthesis support - Complete set of synthesis scripts for Synopsys
- Simulation support – A set of scripts and macros for Synopsys, MTI, and Aldec
- Example CHIP_C32025 – TMS320C25 compatible design
  This design uses the C32025 and illustrates how to build and connect memories and tri-state buffers
- Extensive HDL Test Bench that instantiates:
  - Example design CHIP_C32025
  - External RAM
  - External ROM
  - External I/O
  - Clock generator
  - Process that compares your simulation results with the expected results
- A collection of test assembler programs which are executed directly by the Test Bench
- A set of expected results
- Additional documentation
  - Architectural overview
  - Hardware description
  - User Guide
  - Design support including consulting

Deliverables

Netlist Licenses

- Post-synthesis EDIF netlist
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Place & Route script
- Simulation script
- Constraint file
- Instantiation templates
- User Documentation

HDL Source Licenses

- Synthesizable VHDL or Verilog RTL source code
- Testbench (self-checking)
- Vectors for testbenches
- Expected results
- Simulation script
- Synthesis script
- User Documentation

Related Information

Texas Instruments

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This megafunction developed by the processor experts at Evatronix SA