AKD4115-A
AK4115 Evaluation Board Rev.3

GENERAL DESCRIPTION

AKD4115 is the evaluation board for AK4115, 192kHz digital audio transceiver. This board has optical, cannon connector (XLR), and BNC connectors to interface with other digital audio equipment.

■ Ordering guide

AKD4115-A --- Evaluation board for AK4115
(A cable for connecting the printer port (parallel port) of IBM-AT compatible PC and control software are packed with this document. Please note that the control software does not operate on Windows NT)

FUNCTION

☐ Digital interface

-S/PDIF :
8 channel input (optical, BNC or XLR)
2 channel output (optical, BNC or XLR)
- Serial audio data I/F :
1 input (for DIT data input. 10-pin port)
1 output (for DIR data output. 10-pin port)
-B,C,U,V bit :
1 input/output port (10-pin port)
-Serial control data I/F
1 input/output port (10-pin port)

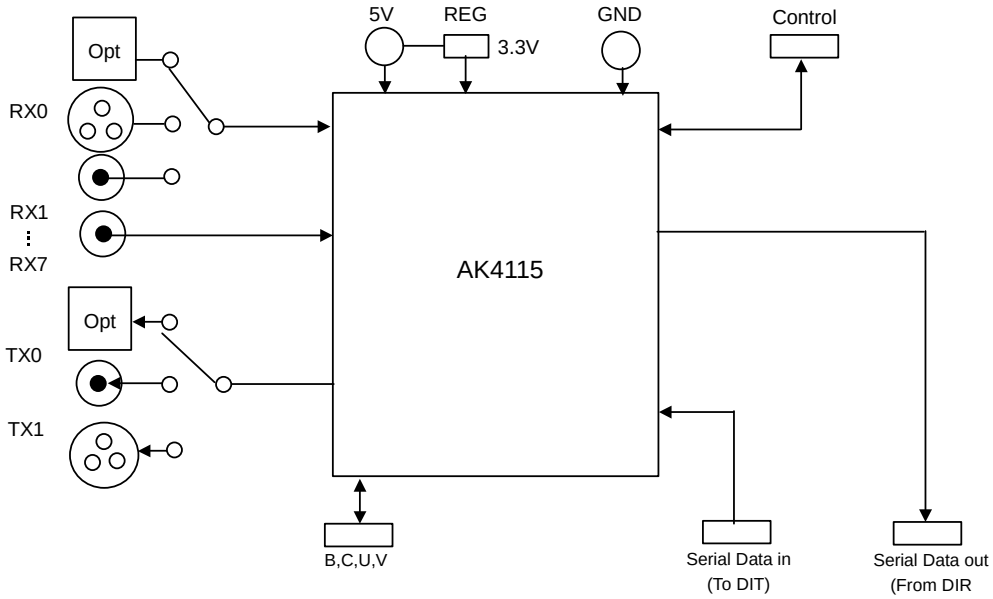


Figure 1. AKD4115-A Block Diagram
*Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operating sequence

(1) **Set up the power supply lines.**
[+ 5V] (Red) = 5V
[GND] (Black) = 0V

Each supply line should be distributed from the power supply unit.

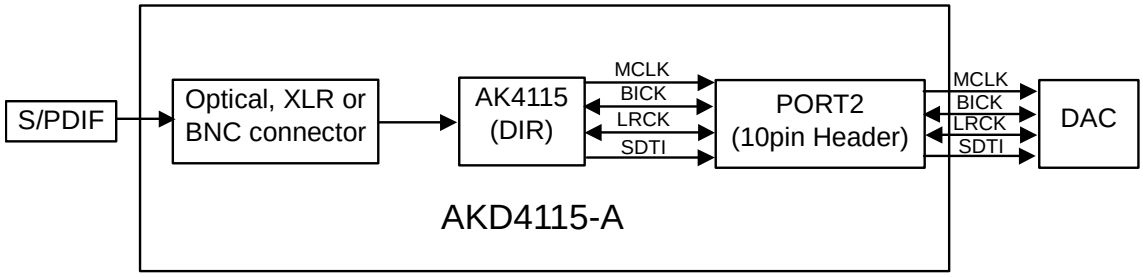
(2) **Set up the evaluation mode and jumper pins.** (Refer to the following item.)

(3) **Connect cables.** (Refer to the following item.)

(4) **Power on.**
The AK4115 should be reset once bringing PDN (SW2) "L" upon power-up.

■ Evaluation modes

(1) Evaluation for DIR



The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector(PORT1: TORX176), BNC connector or cannon connector(XLR). The AKD4115 can be connected with the AKM's DAC evaluation board via 10-pin cable.

a. Set-up of Bi-phase Input

RXP0/RXN0 and RX1-7 should not select BNC at the same time.

a-1. RXP0/RXN0

Connector	JP2(RXP0)	JP3(RXN0)
Optical (PORT1)	OPT	BNC
XLR (J1)	XLR	XLR
BNC (J2)	BNC	BNC

Table 1. Set-up of RXP0/RXN0

a-2. RX1, 2, 3, 4, 5, 6, and 7 can be inputted from a BNC (J2) connector only.
Only RX1, RX2 and RX 3 can be used in parallel mode. The jumper which selects the Rx channel should be Short.

Input	RX1	RX2	RX3	RX4	RX5	RX6	RX7
JP	JP4	JP5	JP6	JP7	JP8	JP9	JP10
	Short	Short	Short	RX4	RX5	RX6	RX7

Table 2. Set-up of RX1, 2, 3, 4, 5, 6 and 7

a-3. Set-up of AK4115 input path

In Parallel Mode you will need to use SW1_1 & SW1_5.
In Serial Mode you will need to use IPS2-0 bits.

-	IPS1 pin (SW1_5)	IPS0 pin (SW1_1)	INPUT Data	
IPS2 bit	IPS1 bit	IPS0 bit		
0	0	0	RX0	Default
0	0	1	RX1	
0	1	0	RX2	
0	1	1	RX3	
1	0	0	RX4	
1	0	1	RX5	
1	1	0	RX6	
1	1	1	RX7	

(In parallel mode, IPS2 is fixed to "0")
Table 3. Recovery Data Select

b. Set-up of clock input and output

The signal level outputted/inputted from PORT2 is 3.3V.

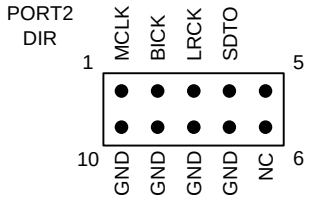


Figure 2. PORT2 pin layout

b-1. MCKO1/MCKO2

The output of MCKO1 pin or MCKO2 pin can be selected by JP12. The output frequency of MCKO1/MCKO2 is selected by OCKS 1-0.

Output signal	JP12	
MCKO1	MCKO1	Default
MCKO2	MCKO2	

Table 4. MCKO1/MCKO2 set-up

OCKS1 pin (SW3_2)	OCKS0 pin (SW3_3)	(X'tal)	MCKO1	MCKO2	fs (max)	
OCKS1 bit	OCKS0 bit					
0	0	256fs	256fs	256fs	96 kHz	Default
0	1	256fs	256fs	128fs	96 kHz	
1	0	512fs	512fs	256fs	48 kHz	
1	1	128fs	128fs	64fs	192 kHz	

Table 5. Master Clock Frequency Select

b-2. Set-up of BICK and LRCK input and output

Please select SW 3_7 (DIR_I/O) according to the setup of audio format of AK4115 (Refer to Table 7).

Audio format	SW3_7 (DIR_I/O)	
Slave mode	0	Default
Master mode	1	

Table 6. DIR_I/O set-up

c. Set-up of Audio format

It sets up by SW 1_2 and SW 1_3 in parallel mode. Please set up DIF2-0 bit and AES3 bit in serial mode.

Mode	-	-	DIF1 pin (SW1_3)	DIF0 pin (SW1_2)	DAUX	SDTO	LRCK		BICK		
	AES3 bit	DIF2 bit	DIF1 bit	DIF0 bit				I/O		I/O	
0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	0	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
5	0	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	0	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	Default
7	0	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	
8	1	x	x	x	24bit, Left justified	AES3 Mode	H/L	O	64fs	O	

Table 7. Audio format

d. Set-up of CM1 and CM0

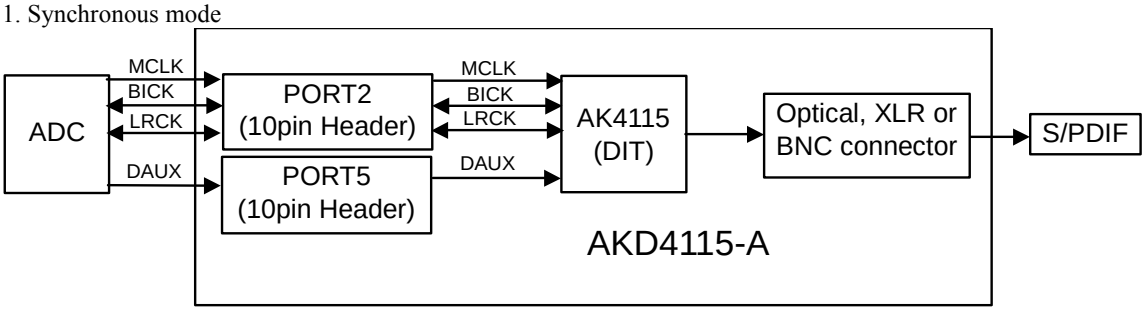
The operation mode of PLL is selected by CM1 and CM0. In parallel mode, it can be selected by SW3_4, SW3_1 and JP18. In serial mode, it can be selected by PSEL bit and CM1-0 bits.

PSEL pin (SW3_4) / PSEL bit	CM1 pin (SW3_1) / CM1 bit	CM0 pin (JP18) / CM0 bit	(UNLOCK)	PLL	X'tal	Clock source	SDTO source	
0	0	0	-	ON	ON(Note)	PLL(RX)	RX	Default
0	0	1	-	OFF	ON	X'tal	DAUX	
0	1	0	0	ON	ON	PLL(RX)	RX	
			1	ON	ON	X'tal	DAUX	
0	1	1	-	ON	ON	X'tal	DAUX	
1	0	0	-	ON	ON(Note)	PLL(ELRCK)	DAUX	
1	0	1	-	OFF	ON	X'tal	DAUX	
1	1	0	0	ON	ON	PLL(ELRCK)	DAUX	
			1	ON	ON	X'tal	DAUX	

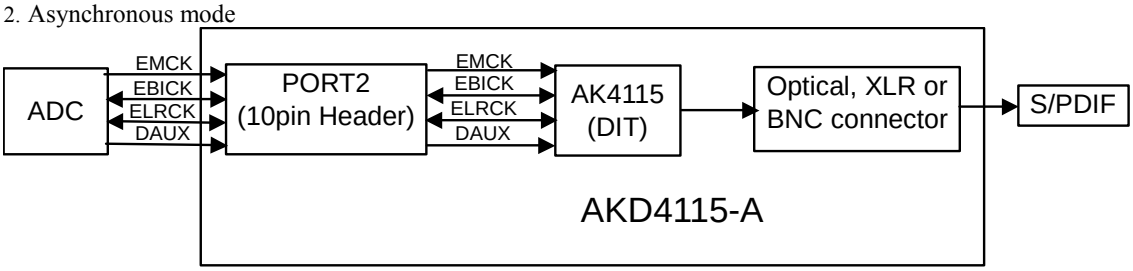
ON: Oscillation (Power-up), OFF: STOP (Power-Down)
Note: When the X'tal is not used as clock comparison for fs detection (XTL0, 1= "1,1"), the X'tal is OFF.
Table 8. Clock Operation Mode Select

(2) Evaluation for DIT

1. Synchronous mode



2. Asynchronous mode



MCLK, BICK, LRCK and DAUX are input the via 10pin header (PORT5: DIT). The AKD4115-A can be connected with the AKM's ADC evaluation board via 10-pin cable.

a. Set-up of a Bi-phase output signal

TX0 and TXP0/TXN0 should not select an optical connector or a BNC connector at the same time.

a-1. The data outputted from TXP1/TXN1 can be selected by OPS12-10 bit.

Connector	JP19 (TXP1)	JP14 (TXN1)
Optical (PORT4)	OPT	BNC
XLR (J3)	XLR	XLR
BNC (J4)	BNC	BNC

Table 9. Set-up of TXP1/TXN1

a-2. As for TX0, only the loop back mode of RX corresponds. This mode is fixed to RX0 in parallel mode. In serial mode, it can be selected by OPS02-00 bits.

Connector	JP13 (TX0)	JP19 (TXP1)	JP14 (TXN1)
Optical (PORT4)	OPT	Open	BNC
BNC (J4)	BNC	Open	BNC

Table 10. Set-up of TX0

b. Set-up of clock input and output

b-1. In the case of synchronous mode (ASYNC bit="0" or Parallel mode)

The used signals are MCKO1, MCKO2, LRCK, BICK, ELRCK and DAUX.
The signal level outputted and inputted from PORT2 and PORT5 is 3.3V.

Clock	PORT
MCLK	PORT2
BICK	PORT2
LRCK	PORT2
DAUX	PORT5
ELRCK	PORT5(LRCK)

Table 11. Clock input and output

b-1-1. MCKO1/MCKO2

The output of MCKO1 pin or MCKO2 pin can be selected by JP12. The output frequency of MCKO1/MCKO2 sets up by OCKS 1-0.

Output signal	JP12	JP15	JP11	
MCKO1	MCKO1	MCKO	MCKO1	Default
MCKO2	MCKO2	MCKO	MCKO2	

Table 12. Selection of MCKO1/MCKO2

OCKS1 pin (SW3_2)	OCKS0 pin (SW3_3)	(X'tal)	MCKO1	MCKO2	fs (max)	
OCKS1 bit	OCKS0 bit					
0	0	256fs	256fs	256fs	96 kHz	Default
0	1	256fs	256fs	128fs	96 kHz	
1	0	512fs	512fs	256fs	48 kHz	
1	1	128fs	128fs	64fs	192 kHz	

Table 13. Master Clock Frequency Select

b-1-2. Set-up of BICK and LRCK input and output

Please select SW 3_7 (DIR_I/O) according the setup of audio format of AK4115 (Refer to Table 7).

Audio format	SW3_7 (DIR_I/O)	
Slave mode	0	Default
Master mode	1	

Table 14. Set-up DIR_I/O

b-1-3. A set up of ELRCK

As a reference clock of PLL, when using ELRCK clock, it inputs from PORT5 (LRCK).

	JP16	JP17	
When inputting by AC coupling	AC	AC	
When inputting by CMOS level	DC	DC	Default

Table 15. Set-up of ELRCK input

b-2. In the case of the asynchronous mode (ASYNC bit= "1" , This mode is supported in serial mode.)

The used signals are EMCK, X'tal, EBICK, ELRCK, and DAUX. These signal levels outputted / inputted from PORT5 is 3.3V.

Clock	PORT
MCLK	PORT5
BICK	PORT5
LRCK	PORT5
DAUX	PORT5
ELRCK	PORT5

Table 16. Clock input and output

b-2-1. Set-up of Master clock

When EMCK is used

Output signal	MSEL bit	JP15
EMCK	1	EMCK

Table 17. Selection of EMCK

When X'tal is used as master clock

Output signal	JP12	JP15	JP11
MCKO1	MCKO1	MCKO	MCKO1
MCKO2	MCKO2	MCKO	MCKO2

Table 18. Selection of MCKO1/MCKO2

b-2-2. Setup of BICK and LRCK input and output

Please set up SW 3_8 (DIT_I/O) according to the setup of audio format of AK4115 (Refer to Table 20). JP16 and 17 are fixed to the "DC" side.

Audio format	SW3_8 (DIT_I/O)	
Slave mode	0	Default
Master mode	1	

Table 19. DIT_I/O set-up

c. Set-up of audio data format

c-1. In case of synchronous mode.

Please refer to Table 7.

c-2. In case of asynchronous mode

Mode	EDIF1 bit	EDIF0 bit	DAUX	ELRCK		EBICK		
					I/O		I/O	
4	0	0	24bit, Left justified	H/L	O	64fs	O	
5	0	1	24bit, I^2S	L/H	O	64fs	O	
6	1	0	24bit, Left justified	H/L	I	64-128fs	I	Default
7	1	1	24bit, I^2S	L/H	I	64-128fs	I	

Table 20. Audio data format in asynchronous mode

d. Set-up of PSEL, CM1 and CM0

d-1. In case of synchronous mode.

Please refer to Table 8.

d-2. In case of asynchronous mode

CM1 bit	CM0 bit	(UNLOCK)	PLL	X'tal	RX					
					Clock source	Clock I/O	SDTO	Clock source	Clock I/O	
0	0	-	ON	ON(Note 2)	PLL (RX)	Note 3	RX	X'tal or EMCK (Note 5)	Note 4	Default
0	1	-	OFF	ON	X'tal	Note 3	"L"	X'tal or EMCK	Note 4	
1	0	0	ON	ON	PLL (RX)	Note 3	RX	X'tal or EMCK	Note 4	
		1	ON	ON	X'tal	Note 3	"L"	X'tal or EMCK	Note 4	
1	1	-	ON	ON	X'tal	Note 3	"L"	X'tal or EMCK	Note 4	

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Note 2: When the X'tal is not used as clock comparison for sampling frequency detection (i.e. XTL1, 0 = "1, 1"), the X'tal is OFF.

Note 3: MCKO1/2, BICK, LRCK

Note 4: EMCK OR X'tal, EBICK, ELRCK, DAUX

Note 5: When X'tal is OFF, the clock source supports EMCK only.

Table 21. Clock Operation Mode Select

■ B, C, U, V Inputs and output

B(block start), C(channel status), U(user data) and V(validity) are inputted via 10pin header (PORT3: BCUV). When BCU_IO bit is set to "1", they are input signals. And when BCU_IO bit is set to "0", they are output signals. In parallel mode, they are fixed to output signals. Pin arrangement of PORT3 has become like Figure 3.

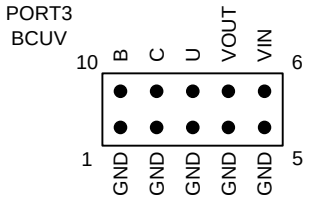


Figure 3. PORT3 pin layout

■ Serial control

The AK4115 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect the included 10pin cable to PORT6 (uP-I/F) of the AKD4115-A. Take care of the direction of connector. There is a mark at pin#1. And the pin layout of PORT6 is as Figure 4 shows.

Mode	SW1_5	JP18
4 wire Serial	L	CDTO/CM0="H" (Short)
IIC	H	SDA (Short) CM0="L" (Short) (Note)

Note: In IIC mode, the chip address is fixed to "01".
Table 22. Set-up of Parallel mode and Serial mode

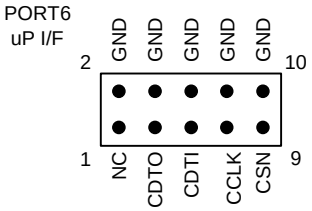


Figure 4. PORT6 pin layout

The evaluation board also includes control software and a software operation procedure is included in the evaluation board manual.

■ **Toggle switch set-up**

SW2	PDN	Reset switch for AK4115. Set to "H" during normal operation. Bring to "L" once after the power is supplied.

■ **LED indication**

LE1	INT0	Bright when INT0 pin goes to "H".
LE2	INT1	Bright when INT1 pin goes to "H".

■ **DIP switch (SW1) set-up: -off- means "L"**

No.	Switch Name	Function	Default
1	IPS0	Set-up of IPS0 pin. (in parallel mode)	OFF
2	DIF0	Set-up of DIF0 pin. (in parallel mode)	OFF
3	DIF1	Set-up of DIF1 pin. (in parallel mode)	OFF
4	XSEL	Set-up of XSEL pin. (in parallel mode) "L": X'tal 1, "H": X'tal 2	OFF
5	IPS1/IIC	Set-up of IPS1 pin. (in parallel mode) Set-up of IIC pin. (in serial mode) "L": 4 wire Serial, "H": IIC	OFF
6	P/SN	Set-up of P/SN pin. "L": Serial mode, "H": parallel mode	OFF
7	TEST	Set-up of TEST pin. (always "OFF")	OFF
8	ACKS	Set-up of ACKS pin. (in parallel mode) "L": Manual Setting, "H": Auto Setting	OFF

Table 23

■ **DIP switch (SW3) set-up: -off- means "L"**

No.	Switch Name	Function	Default
1	CM1	Set-up of CM1 pin. (in parallel mode)	OFF
2	OCKS1	Set-up of OCKS1 pin. (in parallel mode)	OFF
3	OCKS0	Set-up of OCKS0 pin. (in parallel mode)	OFF
4	PSEL	Set-up of PSEL pin. (in parallel mode) "L": S/PDIF Input, "H": ELRCK Input Clock	OFF
5	XTL0	Set-up of XTL0 pin.	OFF
6	XTL1	Set-up of XTL1 pin.	OFF
7	DIR_I/O	Set-up of the transmission direction of 74AC245 "L": When inputting from PORT2, "H": When outputting from PORT2	ON
8	DIT_I/O	Set-up of the transmission direction of 74AC245 "L": When inputting from PORT5, "H": When outputting from PORT5.	OFF

Table 24

■ **Set-up of XSEL, XTL1 and XTL0**

SW1_4	Status	
XSEL	X'tal #1	X'tal #2
0	Power-Up	Power-Down
1	Power-Down	Power-Up

Table 25. Setting of X'tal oscillator

SW3_6	SW3_5	X'tal Frequency		
XTL1	XTL0	X'tal #1	X'tal #2	
0	0	11.2896MHz	12.288MHz	Default
0	1	12.288MHz	11.2896MHz	
1	0	24.576MHz	22.5792MHz	
1	1	(Use channel status)		

Table 26. Reference X'tal frequency

■ **Jumper set up.**

No.	Jumper Name	Function
1	D3V/VD	Set-up of Power supply source for 74AC245. D3V : D3V (default) VD : VD
2	RXP0	Set-up of RXP0 input circuit. OPT : Optical (default) XLR : XLR BNC : BNC
3	RXN0	Set-up of RXP0 input circuit. OPT : Optical (default) BNC : BNC
4,5,6	RX1-3	Set-up of RX1-3 input circuit.
7,8,9,10	RX4-7	RX4-7 set-up depending serial/parallel mode RX4-7 : Serial mode (default) DIF2-0,IPS0 : Parallel mode
11,12	DIR MCLK , DIT MCLK	MCKO set-up for PORT5(DIT) and PORT2(DIR) MCKO1 : MCKO1 of AK4115 (default) MCKO2 : MCKO2 of AK4115
13	TX0	Set-up of TX0 output circuit. OPT : Optical BNC : BNC (default)
14	TXN1	Set-up of TXN1 output circuit. XLR : XLR BNC : BNC (default)
15	MCLK	MCLK input output selection of PORT5(DIT). MCKO : MCKO (default) EMCK : EMCK
16,17	ELRCK	Set-up of ELRCK input signal. AC : AC DC : DC (default)
18	SDA/CDTO	Set-up of SDA/CDTO pin. 4 wire Serial : CDTO/CM0=“H” (default) IIC : SDA
19	TXP1	Set-up of TXP1 input circuit. OPT : Optical (default) XLR : XLR BNC : BNC

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4115-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4115-A by 10-line type flat cable (packed with AKD4115-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4115-A Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4115-a.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

[Port Reset] :	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4115.
[All Write] :	Write all registers that is currently displayed.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0".

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to the AK4115, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to the AK4115, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate volume

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to the AK4115 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to the AK4115, click [OK] button. If not, click [Cancel] button.

4. [SAVE] and [OPEN]

4-1. [SAVE]

All of current register setting values displayed on the main window are saved to the file. The extension of file name is "akr".

<Operation flow>
(1) Click [SAVE] Button.
(2) Set the file name and click [SAVE] Button. The extension of file name is "akr".

4-2. [OPEN]

The register setting values saved by [SAVE] are written to the AK4115. The file type is the same as [SAVE].

<Operation flow>
(1) Click [OPEN] Button.
(2) Select the file (*.akr) and Click [OPEN] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [START] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [SAVE] and [OPEN] button on the Function3 window. The extension of file name is "aks".

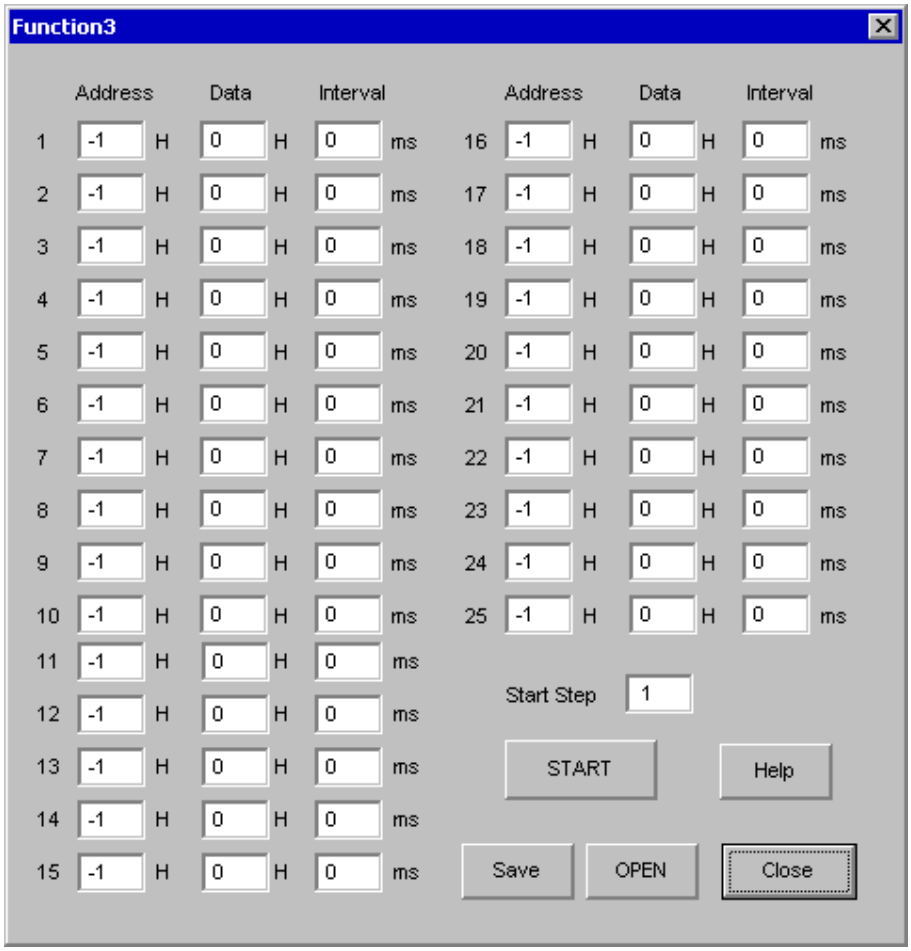


Figure 5. Window of [F3]

6. [Function4 Dialog]

The sequence file (*.aks) saved by [Function3] can be listed up to 10 files, assigned to buttons and then executed. When [F4] button is clicked, the window as shown in Figure 10 opens.

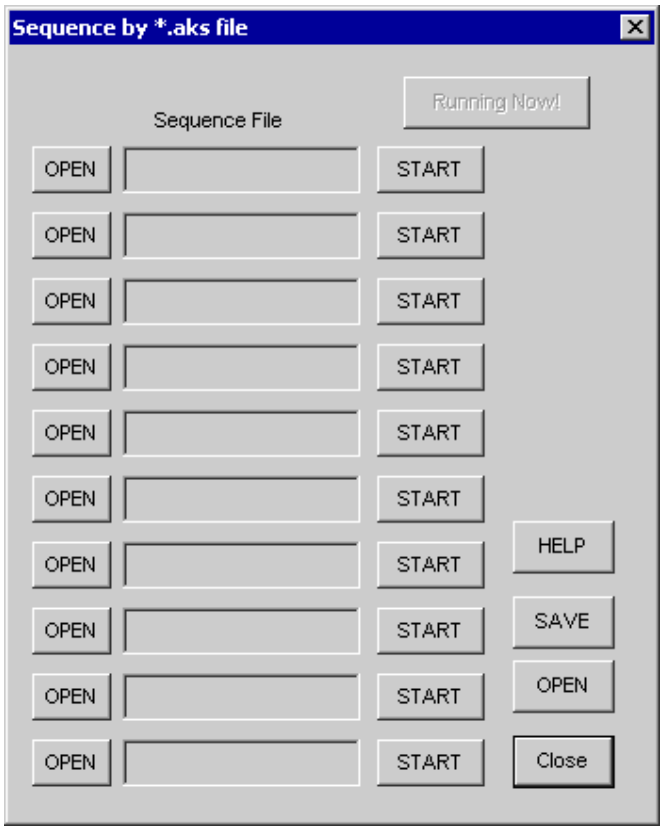


Figure 6. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks) saved by [Function3].

The sequence file name is displayed as shown in Figure 11. (In case that the selected sequence file name is "DAC_Stereo_ON.aks")

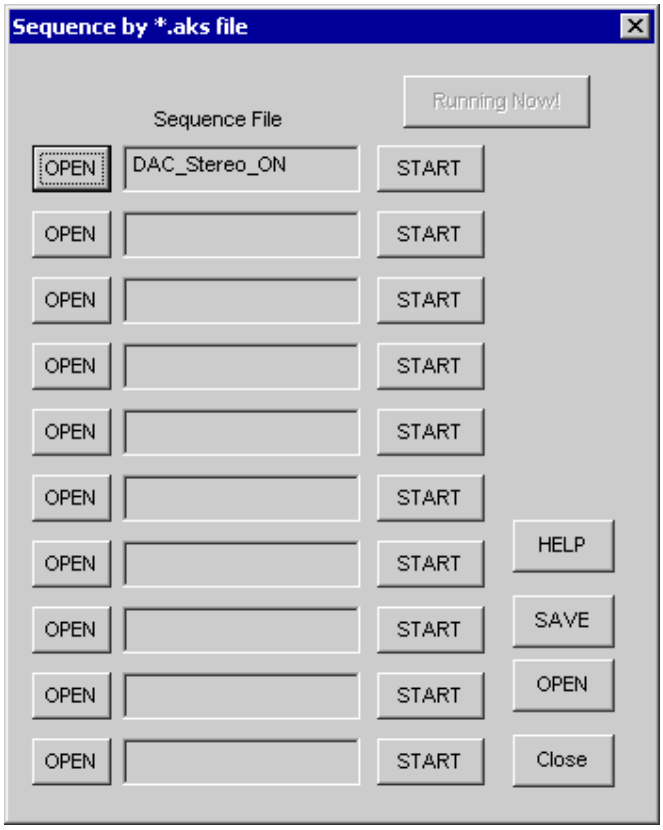


Figure 7. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of sequence file displayed on [Function4] window can be saved to the file. The extension of the file is "*.ak4".

[OPEN] : The name assign of sequence file(*.ak4) saved by [SAVE] is loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(3) When the sequence is changed in [Function3], the sequence file (*.aks) should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting file(*.akr) saved by [SAVE] function on main window can be listed up to 10 files, assigned to buttons and then executed. When [F5] button is clicked, the window as shown in Figure 12 opens.

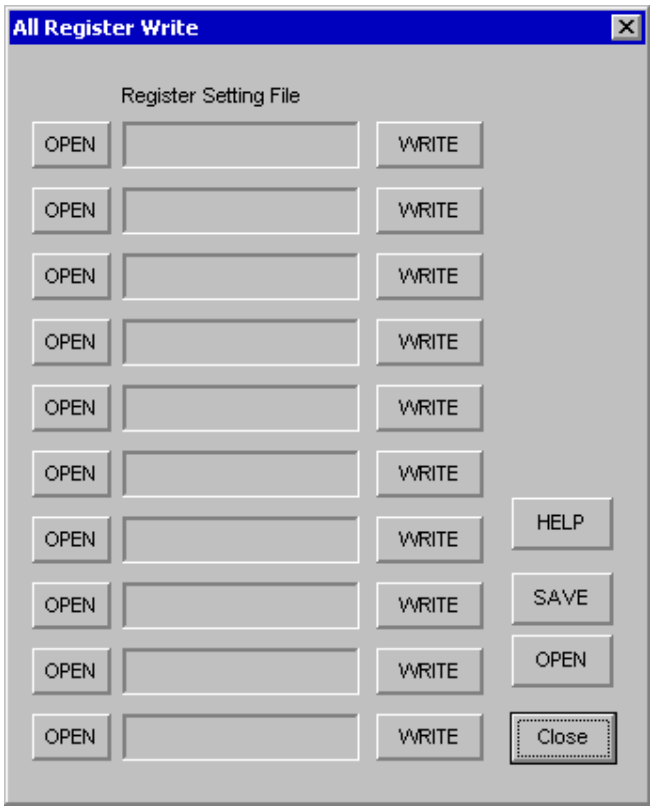


Figure 8. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 13. (In case that the selected file name is "DAC_Output.akr")

(2) Click [WRITE] button, then the register setting is executed.

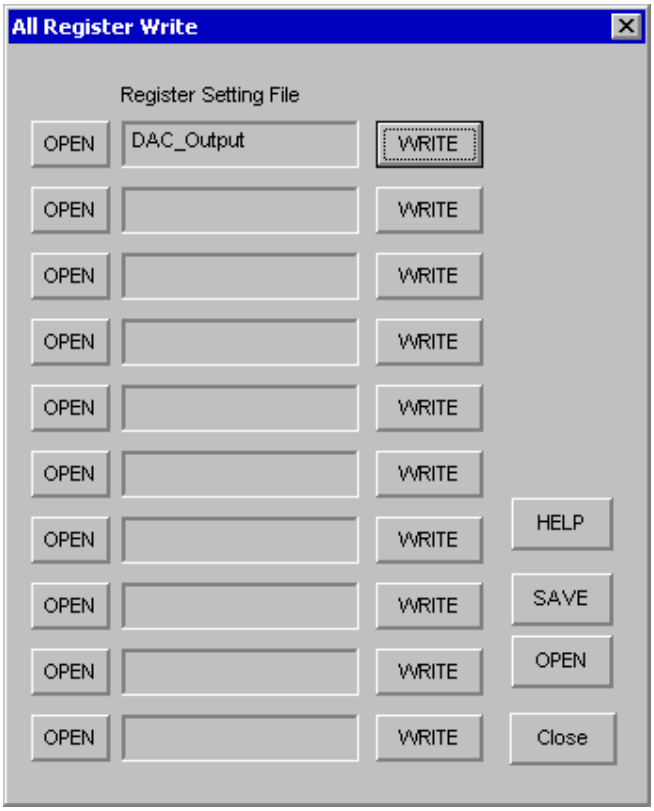


Figure 9. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The name assign of register setting file displayed on [Function5] window can be saved to the file. The file name is "*.ak5".
[OPEN] : The file extension assignment of the register setting file(*.ak5) saved by [SAVE] is loaded.

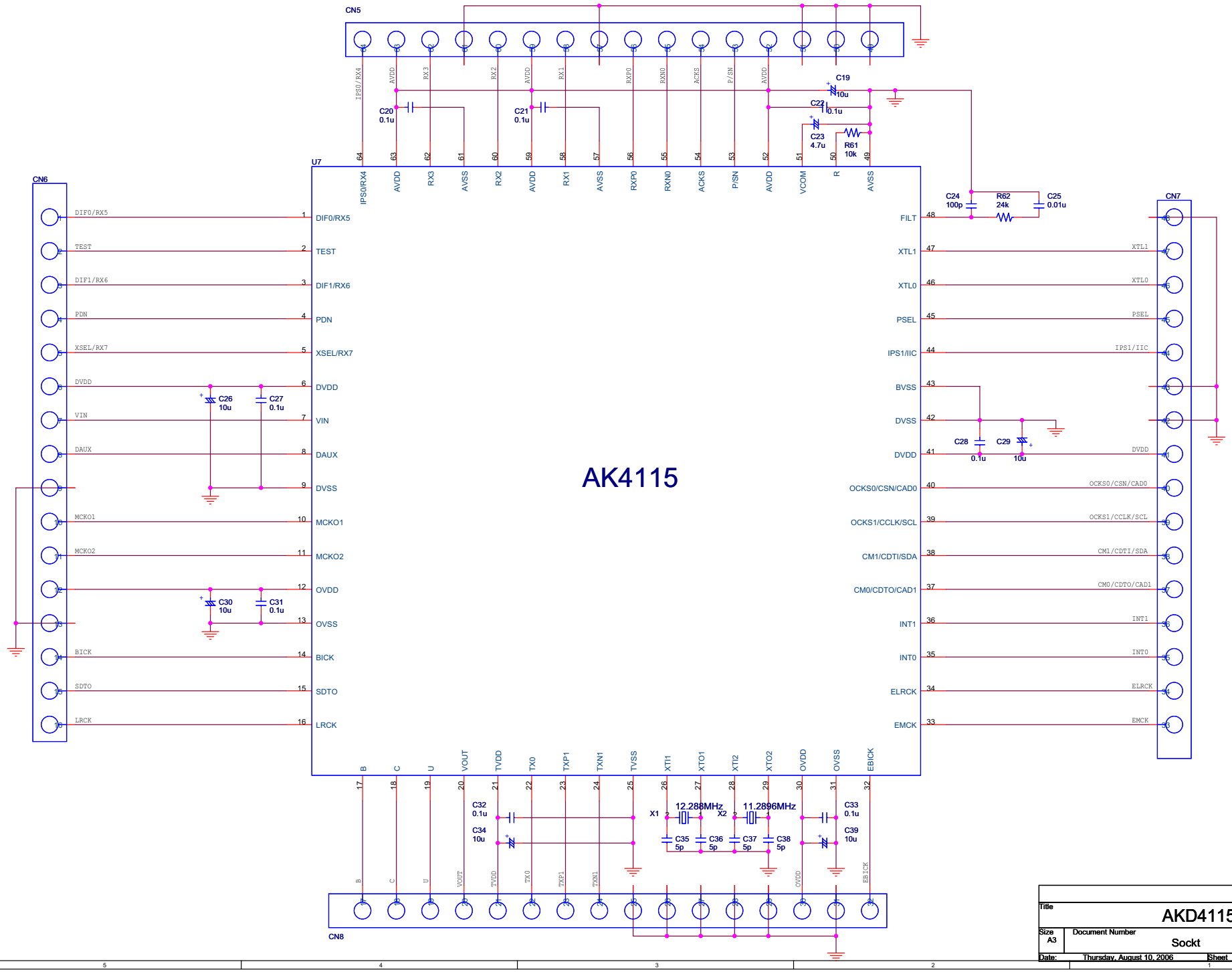
7-3. Note

(1) All files used by [SAVE] and [OPEN] function on right side need to be in the same folder.

(2) When the register setting is changed by [SAVE] Button on the main window, the register setting file (*.akr) should be loaded again in order to reflect the change.

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
04/12/08	KM076400	0	First edition	
06/02/15	KM076401	1	Modification	• Circuit diagram was changed (page 1/3). • The R61 changed from 15kΩ to 10kΩ.
06/06/15	KM076402	2	Add the explanation	P13 "Instruction for use" was added.
			Change control software	Control software was updated: 1.0 → 3.0 Control software manual was changed: P13-14 → P14-21
			Error Correct	P10 • SW_6 →SW_5 • CDTO/CM0="H" → CDTO/CM0="H" (Short) • SDA and CM0="L" → SDA (Short) CM0="L" (Short)
06/08/10	KM076403	3	Change device Revision	AK4115: Rev. C → Rev. D
			Delete the explanation	P13 "Instruction for use" was deleted.
			Change control software	Control software was updated: 3.0 → 4.0



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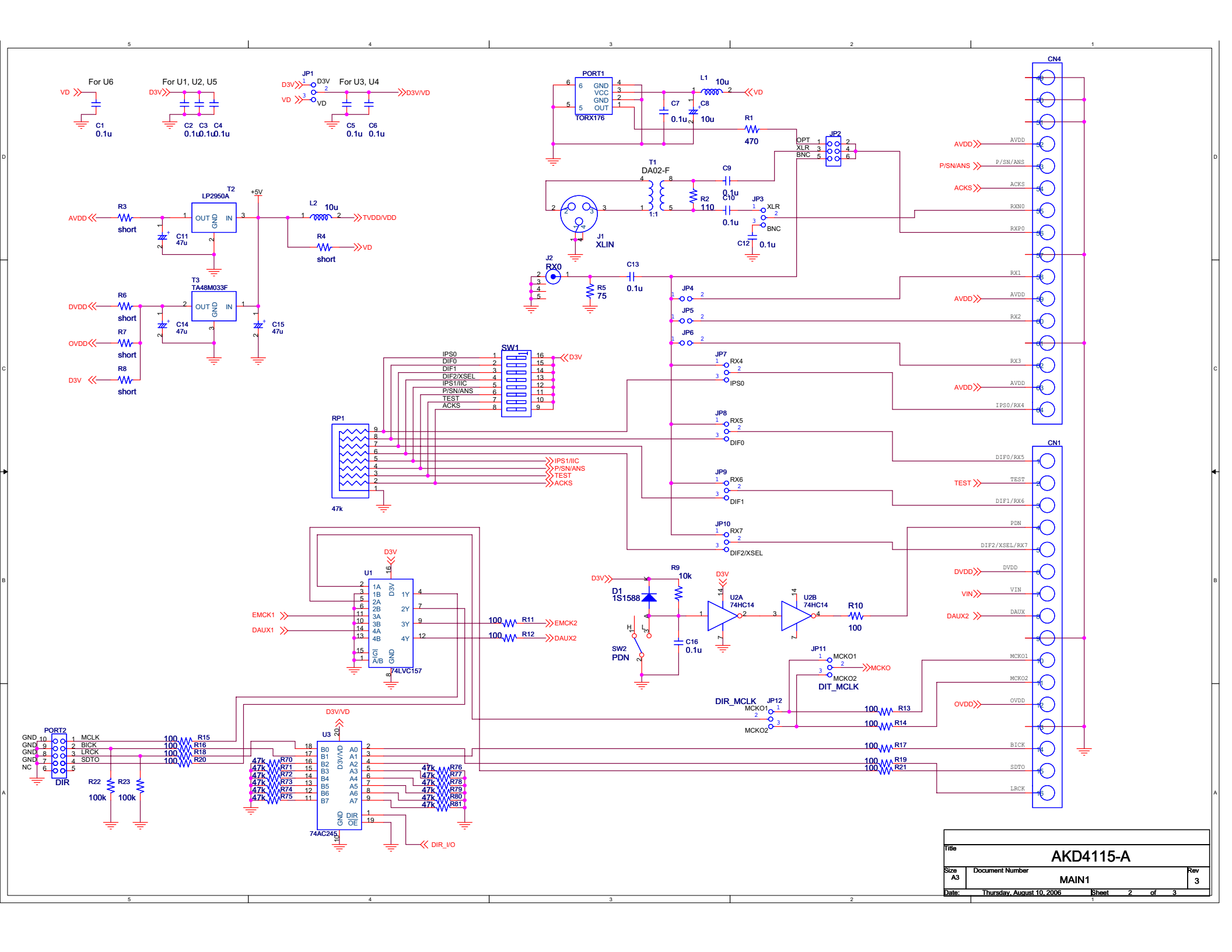
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For U1, U2, U5
For U3, U4
C1 0.1u
C2 0.1u C3 0.1u C4 0.1u
C5 0.1u C6 0.1u
PORT1
TORX176
L1 10u
C7 0.1u
C8 10u
R1 470
T1 DA02-F
1:1
C9 0.1u
C10 0.1u
R2 110
J1 XLIN
JP3 XLR BNC
C12 0.1u
J2 RX0
R5 75
C13 0.1u
JP2
CN4
LP2950A
T2
T3 TA48M033F
R3 short
R4 short
R6 short
R7 short
R8 short
C11 47u
C14 47u
C15 47u
L2 10u
SW1
RP1 47k
JP4
JP5
JP6
JP7 RX4 IPS0
JP8 RX5 DIF0
JP9 RX6 DIF1
JP10 RX7 DIF2/XSEL
U1 74LVC157
R11 100
R12 100
D1 1S1588
R9 10k
SW2 PDN
C16 0.1u
U2A 74HC14
U2B 74HC14
R10 100
JP11 MCKO1 MCKO2 DIT_MCLK
JP12 DIR_MCLK
R13 100
R14 100
CN1
PORT2 DIR
R15 100
R16 100
R17 100
R18 100
R19 100
R20 100
R21 100
R22 100k
R23 100k
U3 74AC245
R70 47k
R71 47k
R72 47k
R73 47k
R74 47k
R75 47k
R76 47k
R77 47k
R78 47k
R79 47k
R80 47k
R81 47k
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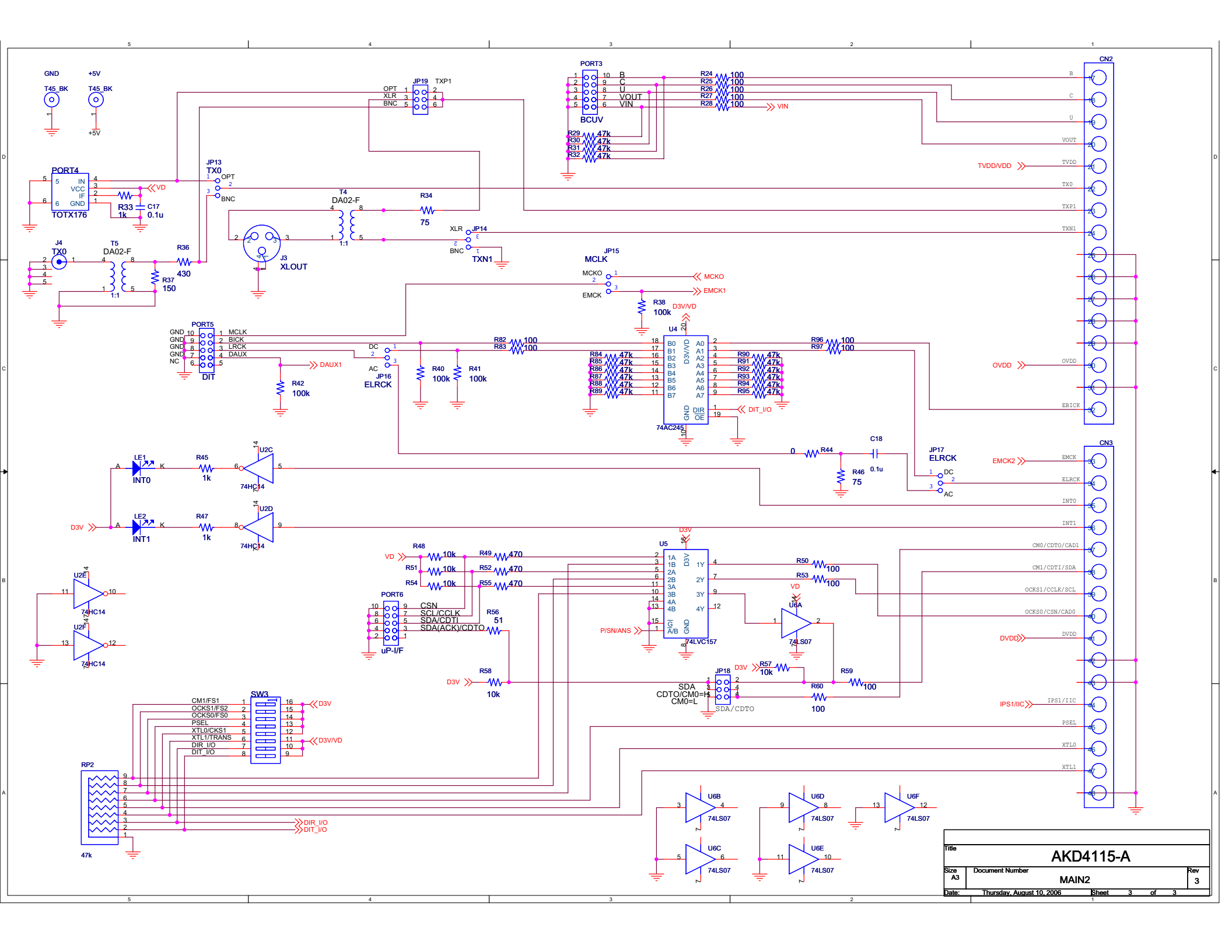
GND
+5V
T45_BK
T45_BK
PORT4
TOTX176
R33 1k
C17 0.1u
VD
JP13 TX0
OPT
BNC
JP19 TXP1
OPT
XLR
BNC
T4 DA02-F
1:1
R34 75
J3 XLOUT
XLR
JP14
BNC
TXN1
J4 TX0
T5 DA02-F
1:1
R36 430
R37 150
PORT3
BCUV
B
C
U
VOUT
VIN
R24 100
R25 100
R26 100
R27 100
R28 100
VIN
R29 47k
R30 47k
R31 47k
R32 47k
CN2
TVDD/VDD
TX0
TXP1
TXN1
OVDD
EBICK
JP15 MCLK
MCKO
EMCK
MCKO
EMCK1
R38 100k
D3V/VD
PORT5
DIT
MCLK
BICK
LRCK
DAUX
DAUX1
R42 100k
DC
AC
JP16 ELRCK
R40 100k
R41 100k
U4
74AC245
R82 100
R83 100
R84 47k
R85 47k
R86 47k
R87 47k
R88 47k
R89 47k
R90 47k
R91 47k
R92 47k
R93 47k
R94 47k
R95 47k
R96 100
R97 100
DIT_I/O
R44 0
C18 0.1u
R46 75
JP17 ELRCK
DC
AC
CN3
EMCK2
ELRCK
INT0
INT1
CM0/CDTO/CAD1
CM1/CDTI/SDA
OCKS1/CCLK/SCL
OCKS0/CSN/CAD0
DVDD
IPS1/IIC
PSEL
XTL0
XTL1
LE1 INT0
LE2 INT1
R45 1k
R47 1k
U2C 74HC14
U2D 74HC14
U2E 74HC14
U2F 74HC14
D3V
R48 10k
R51 10k
R54 10k
R49 470
R52 470
R55 470
R56 51
R58 10k
PORT6
uP-I/F
CSN
SCL/CCLK
SDA/CDTI
SDA(ACK)/CDTO
U5
74LVC157
P/SN/ANS
R50 100
R53 100
U6A 74LS07
JP18
SDA
CDTO/CM0=H
CM0=L
SDA/CDTO
R57 10k
R60 100
R59 100
SW3
CM1/FS1
OCKS1/FS2
OCKS0/FS0
PSEL
XTL0/CKS1
XTL1/TRANS
DIR_I/O
DIT_I/O
D3V
D3V/VD
RP2
47k
DIR_I/O
DIT_I/O
U6B 74LS07
U6C 74LS07
U6D 74LS07
U6E 74LS07
U6F 74LS07
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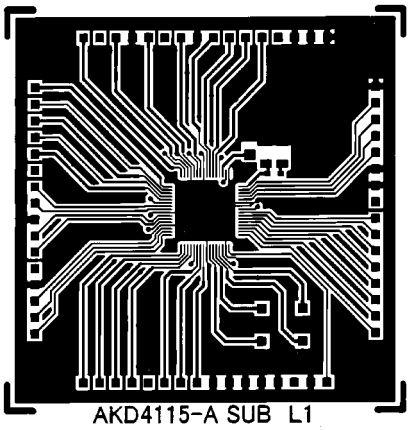

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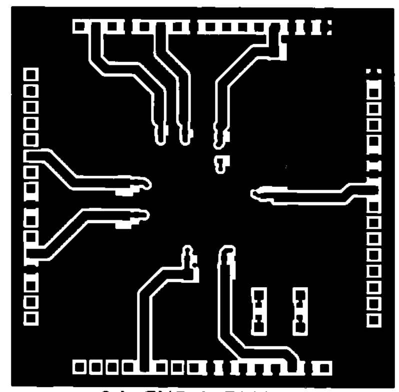
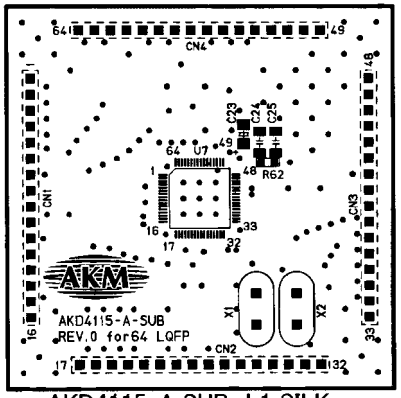
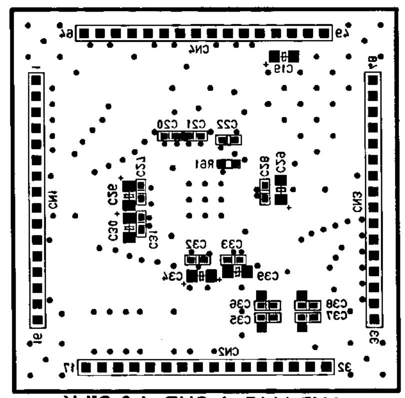


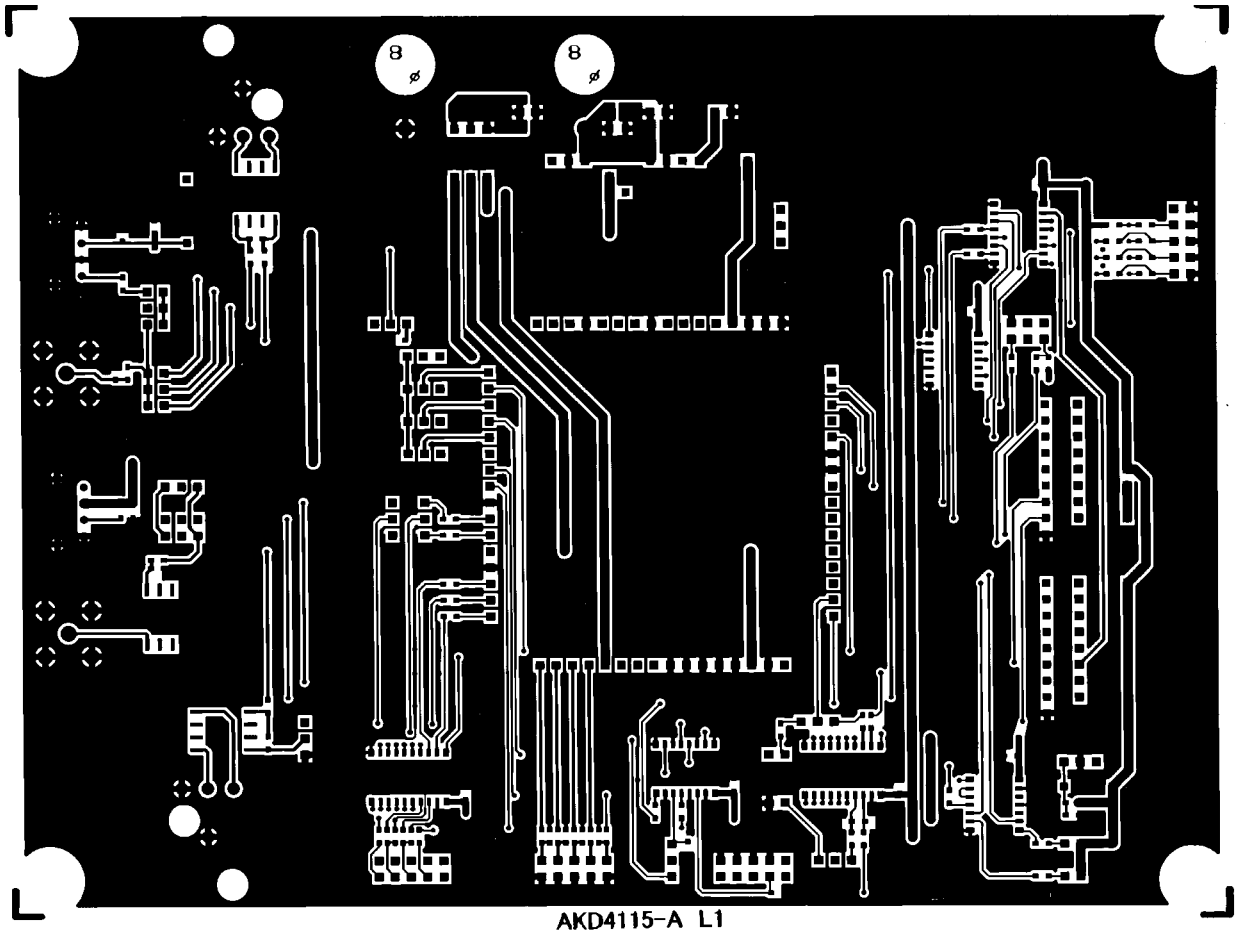
AKD4115-A SUB L2



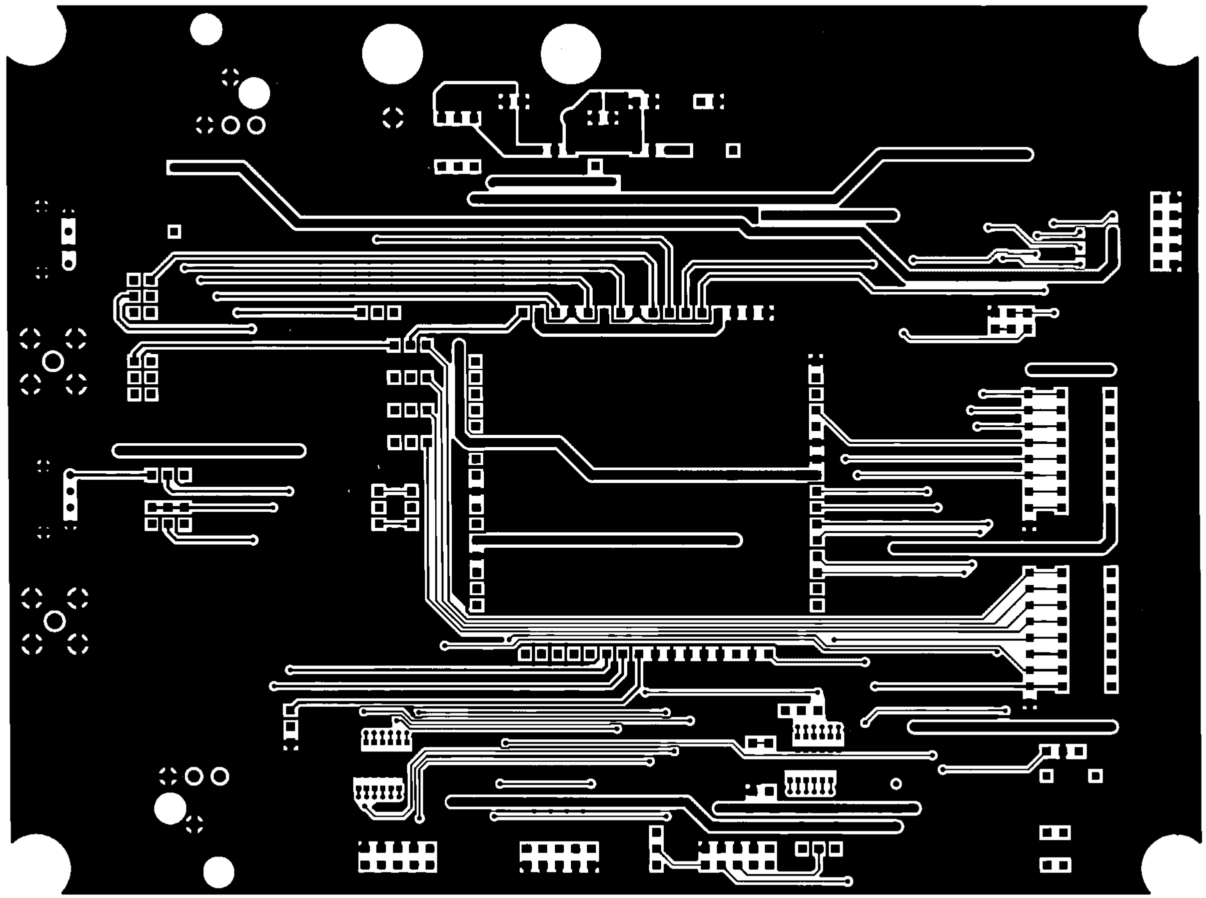
AKD4115-A SUB L1_SILK



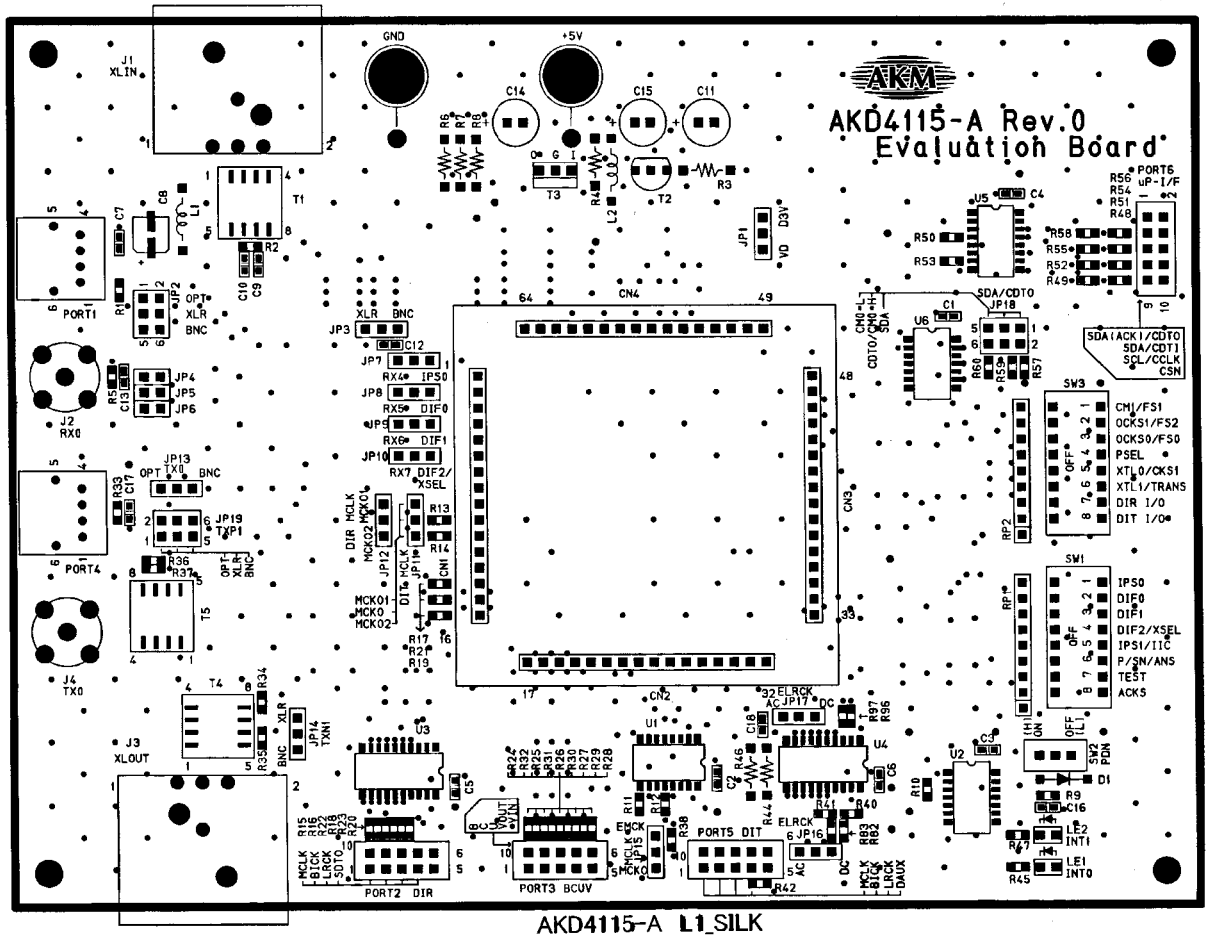
AKD4115-A SUB L2_SILK



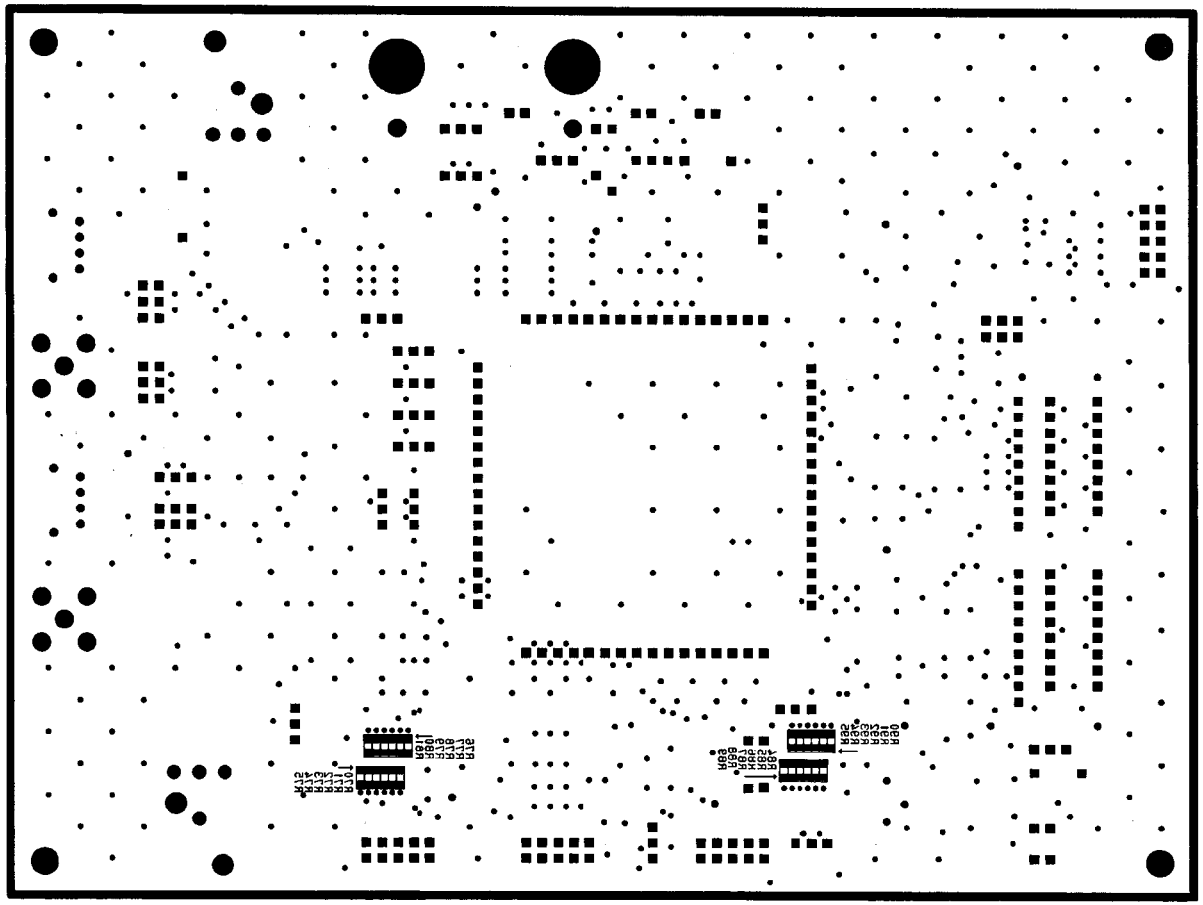
AKD4115-A L1



AKD4115-A L2



AKD4115-A L1_SILK



AKD4115-A L2_SILK