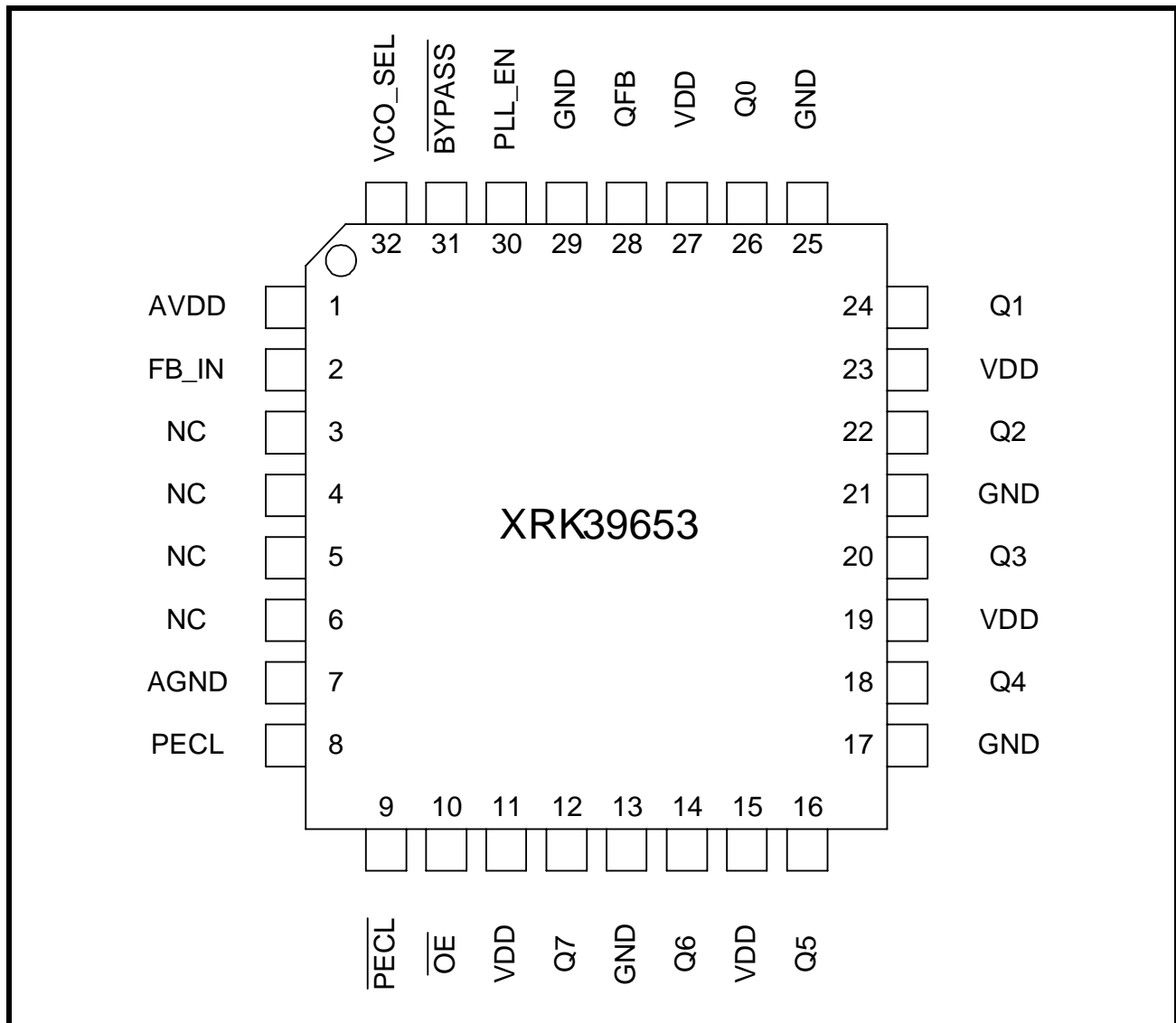


PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK39653CQ	32-Lead TQFP	0°C to +70°C
XRK39653IQ	32-Lead TQFP	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRK39653



PIN DESCRIPTIONS

NUMBER	NAME	TYPE		DESCRIPTION
1	AVDD	Power		Power supply for PLL
2	FB_IN	Input	pull-up	External PLL feedback clock input
3, 4, 5, 6	NC			
7	AGND	Power		PLL ground
8	PECL	Input		LVPECL - pos differential reference clock
9	$\overline{\text{PECL}}$	Input		LVPECL - neg differential reference clock
10	$\overline{\text{OE}}$	Input	pull-down	Output enable/disable and device reset
11,15, 19, 23, 27,	VDD	Power		Power supply
12, 14, 16, 18, 20, 22, 24, 26	Q[7:0]	Output		Clock outputs
13, 17, 21, 25, 29	GND	Power		Ground
28	QFB	Output		Feedback output for PLL
30	PLL_EN	Input	pull-up	PLL enable/disable select
31	$\overline{\text{BYPASS}}$	Input	pull-up	PLL and output divider bypass select
32	VCO_SEL	Input	pull-up	VCO divider select

TABLE 1: CONTROL INPUT FUNCTION TABLE

Pin Name	0	1	Default
VCO_SEL	System Divide = 4 of VCO output	System Divide = 8 of VCO output	1
PLL_EN	PLL is bypassed and disabled. The PECL clock reference source drives the outputs through the divider blocks	PLL enabled. Normal operation. VCO output drives the outputs through the divider blocks	1
$\overline{\text{BYPASS}}$	Complete bypass of the PLL and divider blocks. PECL reference clocks the outputs.	Normal operation. Dividers selected.	1
$\overline{\text{OE}}$	Outputs enabled	Outputs tri-stated and device reset. VCO running at minimum frequency	0

DC CHARACTERISTICS ($V_{CC}= 3.3 \pm 5\%$, $T_A= -40^{\circ}\text{C}$ TO $+85^{\circ}\text{C}$)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V_{CMR}^a	PECL Clock inputs common mode range	1.0		$V_{DD}-0.6$	V	LVPECL
V_{PP}	PECL Clock peak-to-peak input voltage	300		1000	mV	LVPECL
V_{IH}	Input voltage high	2.0		$V_{DD}+0.3$	V	LVC MOS
V_{IL}	Input voltage low			0.8	V	LVC MOS
V_{OH}	Output High Voltage ^a	2.4			V	$I_{OH}=-24\text{mA}$
V_{OL}	Output Low Voltage ^a			0.55 0.30	V	$I_{OL}=24\text{mA}$ $I_{OL}=12\text{mA}$
Z_{OUT}	Output Impedance		14-17		Ω	
I_{IN}	Input leakage current			± 200	μA	$V_{IN}=V_{DD}$ or $V_{IN}=\text{GND}$
I_{CC_PLL}	Maximum PLL supply current		5.0	10.0	mA	\overline{AV}_{DD} pin
I_{CCQ}	Maximum Quiescent supply current			10.0	mA	All V_{DD} pins, $\overline{OE}=1$
V_{TT}	Output Termination Voltage		$V_{CC}\pm 2$		V	

a. V_{CMR} is the cross point of the differential input signal.

AC CHARACTERISTICS ($V_{CC}= 3.3 \pm 5\%$, $T_A= -40^{\circ}\text{C}$ TO $+85^{\circ}\text{C}$)^a

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
f_{VCO}	VCO Frequency	200		500	MHz	
f_{ref}	Input Reference Frequency	$\div 4$ feedback $\div 8$ feedback PLL Bypass	50 25 0	125 62.5 200	MHz	PLL locked PLL locked bypass mode
f_{MAX}	Max Output Frequency	$\div 4$ feedback $\div 8$ feedback	50 25	125 62.5	MHz	PLL locked PLL locked
V_{PP}	PECL Clock peak-to-peak input voltage	450		1000	mV	LVPECL
V_{CMR}	PECL input Common Mode range	1.2		$V_{DD}-0.75$	V	LVPECL
$t_{PW\ Min}$	Input Reference Clock Minimum Pulse Width	2			ns	
t_{SPO}	Propagation Delay - Static Phase Offset (PECL to FB_IN)	-75		125	ps	PLL locked
t_{PD}	Propagation Delay - PLL Bypassed					
	Bypass mode 1 ($\overline{BYPASS} = 0$)	1.2		3.3	ns	
	Bypass mode 2, ($\overline{BYPASS} = 1$, $\overline{PLL_EN} = 0$)	3.0		7.0	ns	
$t_{skew(O)}$	Output-to-Output Skew			150	ps	
$t_{skew(PP)}$	Part to Part Skew (bypass PLL & divider)			1.5	ns	$\overline{BYPASS}=0$
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter			100	ps	

AC CHARACTERISTICS ($V_{CC} = 3.3 \pm 5\%$, $T_A = -40^\circ\text{C}$ TO $+85^\circ\text{C}$)^a

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
$t_{\text{JIT(PER)}}$	Period Jitter			100	ps	
$t_{\text{JIT(I/O)}}$	I/O Phase Jitter (RMS)			25	ps	
BW	PLL bandwidth ÷4 feedback ÷8 feedback			0.8 - 4 0.5 - 1.3	MHz MHz	
DC	Output duty cycle	45	50	55	%	PLL locked
t_{LOCK}	Maximum PLL Lock Time			10.0	ms	
$t_{\text{or}}/t_{\text{of}}$	Output Rise/Fall time	100		1000	ps	0.55 to 2.4V
$t_{\text{PLZ,HZ}}$	Output Disable Time			7	ns	
$t_{\text{PHZ,LZ}}$	Output Enable Time			6	ns	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT} .

MAXIMUM RATINGS^a

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT	CONDITION
V_{DD}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	$V_{\text{DD}}+0.3$	V	
V_{OUT}	DC Output Voltage	-0.3	$V_{\text{DD}}+0.3$	V	
I_{IN}	DC Input Current		± 20	mA	
I_{OUT}	DC Output Current		± 50	mA	
T_{S}	Storage Temperature	-65	125	$^\circ\text{C}$	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.

GENERAL SPECIFICATIONS

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V_{TT}	Output termination voltage		$V_{\text{CC}}\div 2$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs

FIGURE 3. OUTPUT-TO-OUTPUT SKEW $t_{SK(O)}$

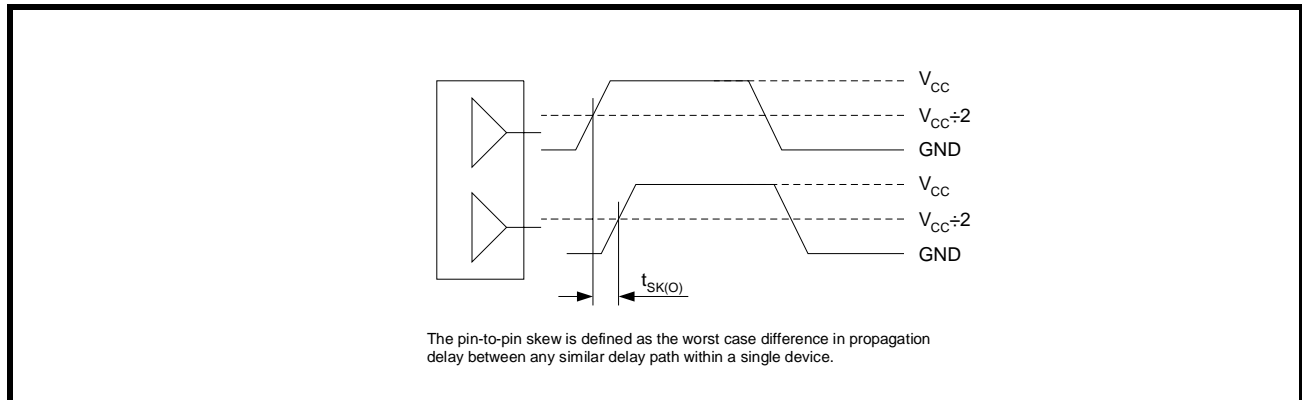


FIGURE 4. PROPOGATION DELAY (t_{ϕ}), STATIC PHASE OFFSET) TEST REFERENCE

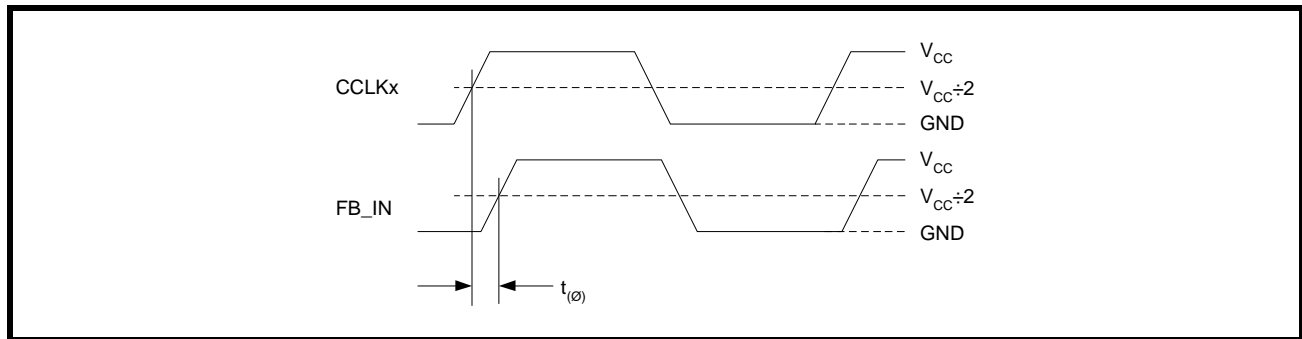


FIGURE 5. OUTPUT DUTY CYCLE (DC)

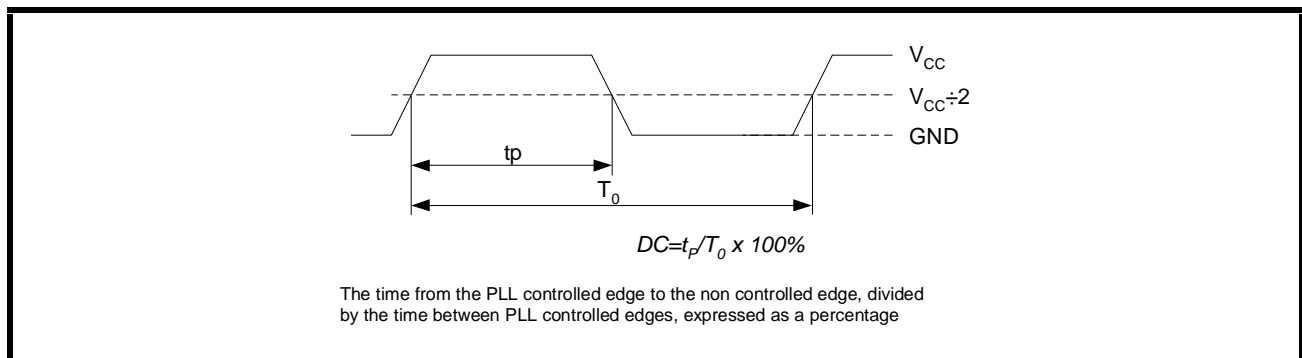


FIGURE 6. I/O JITTER

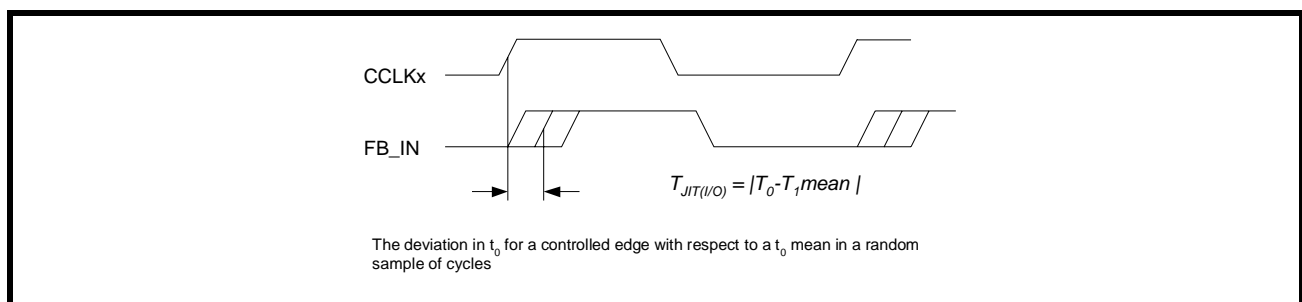


FIGURE 7. CYCLE-TO-CYCLE JITTER

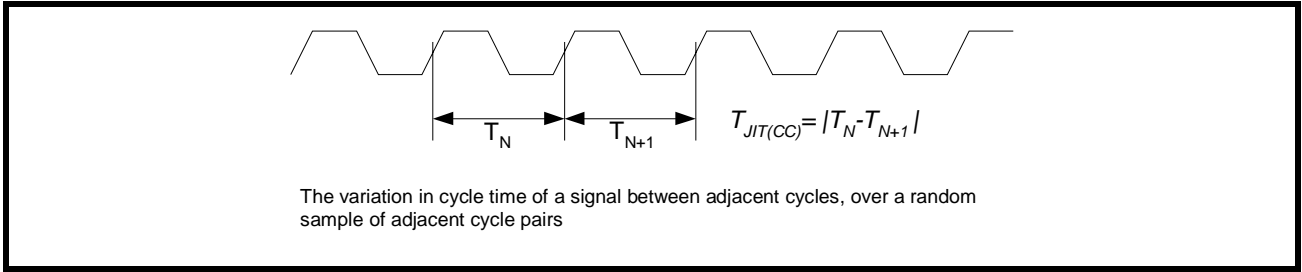


FIGURE 8. PERIOD JITTER

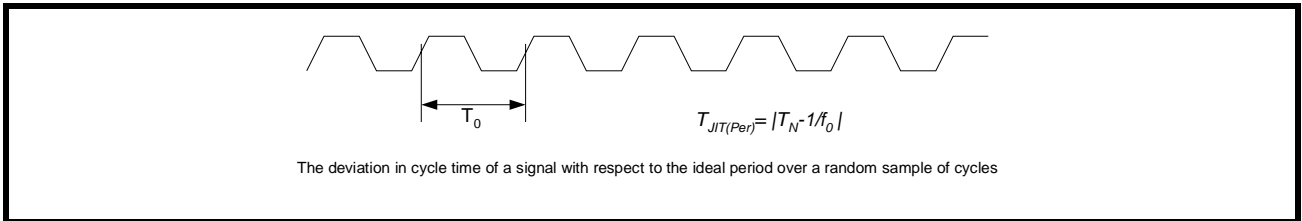
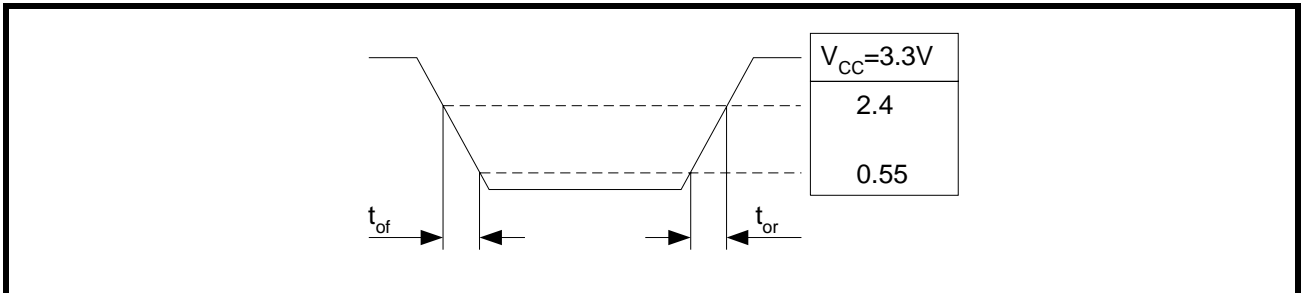
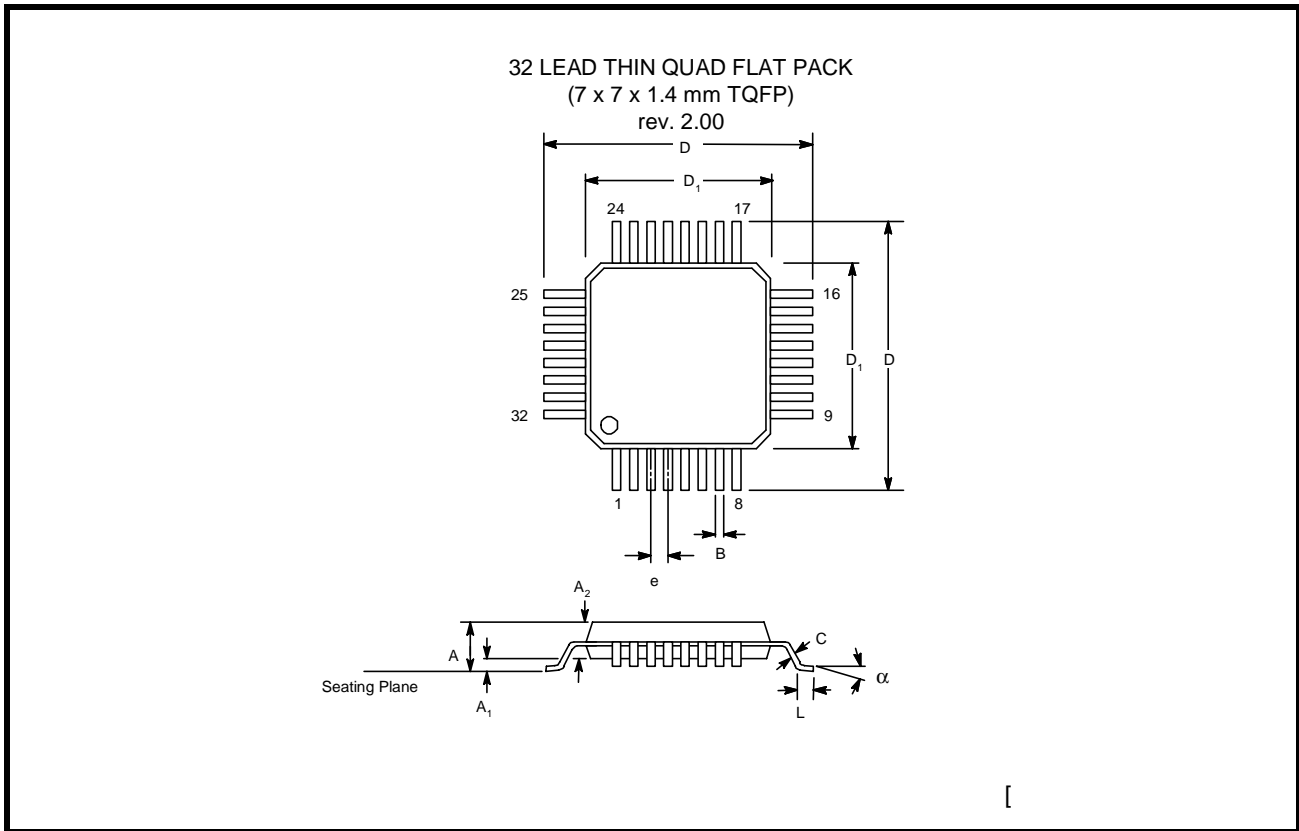


FIGURE 9. OUTPUT TRANSITION TIME TEST REFERENCE



PACKAGE DIMENSIONS



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A ₁	0.002	0.006	0.05	0.15
A ₂	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D ₁	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	November 2006	Initial <i>FINAL</i> release.

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2006 EXAR Corporation

Datasheet November 2006.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.