24-Lane 3-Port PCI Express® Switch

89PES24N3
Product Brief

Device Overview

The 89HPES24N3 is a member of IDT's PRECISE™ family of PCI Express® bridging and switching solutions offering the next-generation I/O interconnect standard. The PES24N3 is a 24-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides high-performance I/O connectivity and switching functions between a PCI Express upstream port and two downstream ports or peer-to-peer switching between downstream ports.

Features

High Performance PCI Express Switch

- 24 PCI Express lanes (2.5Gbps), 3 switch ports
- 12 GBps (96 Gbps) aggregate switching throughput
- Low latency cut-through switch architecture
- Supports 128 to 2048 byte maximum payload size
- One virtual channel
- Fully compliant with PCI Express Base specification Revision 1.0a

Flexible Architecture with Numerous Configuration Options

- Automatic per port link width negotiation to x8, x4, x2 or x1
- Port arbitration schemes utilizing round robin or weighted round robin algorithms
- Static lane reversal on all ports
- Polarity inversion
- Ability to load device configuration from serial EEPROM

Legacy Support

- PCI compatible INTx emulation
- Bus locking

Highly Integrated Solution

- Integrates 24 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)
- Incorporates on-chip internal memory for packet buffering and queueing
- Requires no external components

Reliability, Availability, and Serviceability (RAS) Features

- Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
- ECRC passed through
- Supports PCI Express Native Hot-Plug
  - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
- Hot-Swap capable I/O

Block Diagram

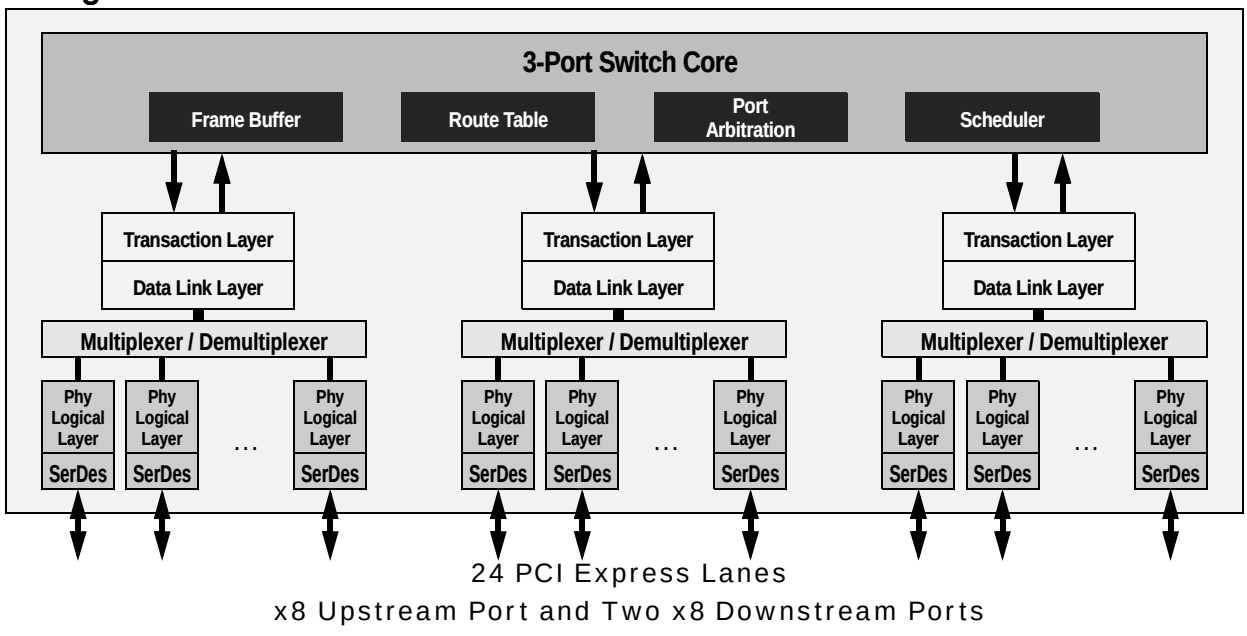

Figure 1 Internal Block Diagram

Power Management

- Utilizes advanced low-power design techniques to achieve low typical power consumption
- Support PCI Express Power Management Interface specification (PCI-PM 1.1)
- Unused SerDes are disabled.
- Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state

Testability and Debug Features

- Support IEEE 1149.6 JTAG which extends the capability of the IEEE 1149.1 standard to include AC-coupled and/or differential nets
- Built in Pseudo-Random Bit Stream (PRBS) generator
- Numerous SerDes test modes
- Ability to read and write any internal register via the SMBus
- Ability to bypass link training and force any link into any mode
- Provides statistics and performance counters

8 General Purpose Input/Output pins

- Each pin may be individually configured as an input or output
- Some pins have selectable alternate functions

Packaged in a 420-ball BGA

- 27x27 mm
- 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES24N3 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 12 GBps (96 Gbps) of aggregated, full-duplex switching capacity through 24 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES24N3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES24N3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes system selectable algorithms such as round robin, weighted round-robin, and strict priority schemes guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 10 Gigabit I/Os, SATA controllers, and Fibre Channel HBAs.

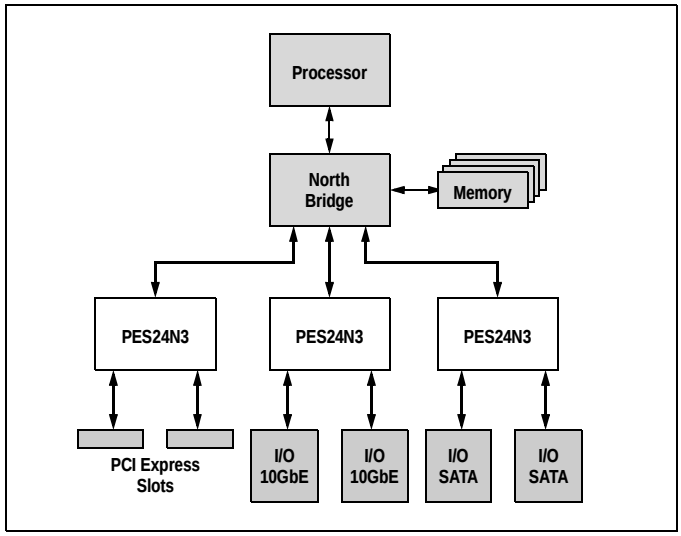

Figure 2 I/O Expansion Application

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