

FEATURES

- 10-bit, 20MHz sampling
- ± 1 LSB max. differential nonlinearity
- Internal calibration circuit
- Internal S/H amplifier
- 70MHz input bandwidth
- TTL/CMOS compatible in-out logic
- Latched three-state output data
- Single +5V supply
- Low 150mW power dissipation
- Small 48 pin LQFP package
- Low cost



INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|-----------------------------------|-----|---------------------------------|
| 1 | BIT 10 (LSB) | 48 | DIGITAL GROUND (DGND) |
| 2 | BIT 9 | 47 | NO CONNECTION |
| 3 | BIT 8 | 46 | NO CONNECTION |
| 4 | BIT 7 | 45 | +DV _S (Digital) |
| 5 | BIT 6 | 44 | ANALOG GROUND (AGND) |
| 6 | DIGITAL GROUND (DGND) | 43 | ANALOG GROUND (AGND) |
| 7 | +DV _S (Digital) | 42 | TEST SIGNAL IN |
| 8 | BIT 5 | 41 | CALIBRATION (CAL) |
| 9 | BIT 4 | 40 | NO CONNECTION |
| 10 | BIT 3 | 39 | ANALOG INPUT (V _{IN}) |
| 11 | BIT 2 | 38 | TEST SIGNAL OUT |
| 12 | BIT 1 (MSB) | 37 | TEST SIGNAL IN |
| 13 | TEST PIN | 36 | ANALOG GROUND (AGND) |
| 14 | TEST SIGNAL IN | 35 | REFERENCE BOTTOM (VRB) |
| 15 | RESET | 34 | REFERENCE BOTTOM (VRB) |
| 16 | DIGITAL GROUND (DGND) | 33 | NO CONNECTION |
| 17 | SELECT (SEL) | 32 | NO CONNECTION |
| 18 | +AV _S (Analog) | 31 | NO CONNECTION |
| 19 | TEST MODE | 30 | REFERENCE TOP (VRT) |
| 20 | LINV | 29 | REFERENCE TOP (VRT) |
| 21 | MINV | 28 | ANALOG GROUND (AGND) |
| 22 | A/D CLOCK | 27 | ANALOG GROUND (AGND) |
| 23 | OUTPUT ENABLE (\overline{OE}) | 26 | +AV _S (Analog) |
| 24 | CHIP ENABLE (\overline{CE}) | 25 | +AV _S (Analog) |

GENERAL DESCRIPTION

DATEL's ADS-325A is a low power, 10-bit, 20MHz, CMOS sampling A/D converter. Its small 48 pin plastic LQFP package contains a S/H amplifier, a 3-state output register, linearity calibration circuitry, and all necessary control logic. Only two external reference voltages, an A/D clock and a few digital inputs are required. The A/D clock may be applied with 50% duty cycle.

The excellent dynamic performance includes a spurious free dynamic range of 65dB and a signal-to-noise ratio with distortion of 54dB with a 3MHz input. ADS-325A is capable of operating from a single +5V power supply and typically consumes only 150mW. It can also operate from a +5V analog V_s with +3.3V digital V_s enabling an interface with 3.3V logic circuitry. The ADS-325A is ideally suited for high quality video/CCD imaging applications.

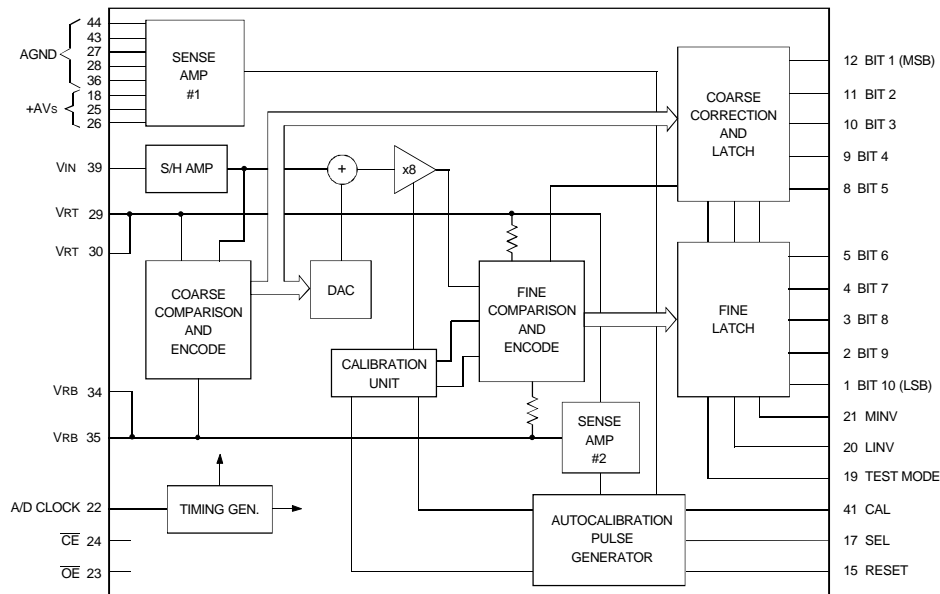


Figure 1. ADS-325A Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

| PARAMETERS | LIMITS | UNITS |
|----------------------------------------------------------------|-------------------------------|-------|
| Supply Voltages (+AV _S and +DV _S) | 0 to +7 | Volts |
| Reference Voltage (V _{RT} and V _{RB}) | -0.5 to +AV _S +0.5 | Volts |
| Input Voltage, Analog (V _{IN}) | -0.5 to +AV _S +0.5 | Volts |
| Input Voltage, Digital (V _{IH} and V _{IL}) | -0.5 to +AV _S +0.5 | Volts |
| Output Voltage, Digital (V _{OH} and V _{OL}) | -0.5 to +DV _S +0.5 | Volts |

FUNCTIONAL SPECIFICATIONS

(Typical at f_S = 20MHz, +AV_S = +5V, +DV_S = +3.3V, V_{RB} = +2.0V, V_{RT} = +4.0V, and T_A = +25°C unless otherwise specified.)

| ANALOG INPUTS | MIN. | TYP. | MAX. | UNITS |
|--------------------------------------|------|----------|------|-------|
| Input Voltage Range, V _{IN} | | +2 to +4 | | Volts |
| Input Current | | | | |
| V _{IN} = +4V | — | 40 | 50 | µA |
| V _{IN} = +2V | -50 | -40 | — | µA |
| Capacitance, C _{IN} | — | 9 | — | pF |
| Bandwidth (-1dB) | — | 70 | — | MHz |

REFERENCE

| | | | | |
|-------------------------------------------------|------|-----|------|-------|
| Reference Input Voltage | | | | |
| V _{RT} | — | +4 | +4.6 | Volts |
| V _{RB} | +1.8 | +2 | — | Volts |
| Input Current | | | | |
| I _{RT} | 5 | 7 | 11 | mA |
| I _{RB} | -11 | -7 | -5 | mA |
| Offset Voltage | | | | |
| V _{RT} | +40 | +90 | +140 | mV |
| V _{RB} | -120 | -70 | -20 | mV |
| Resistance (V _{RT} - V _{RB}) | 180 | 280 | 380 | Ω |

DIGITAL INPUTS

| | | | | |
|---------------------------------------|------|---|------|-------|
| Input Voltage | | | | |
| V _{IH} , Logic "1" | +2.3 | — | — | Volts |
| V _{IL} , Logic "0" | — | — | +0.8 | Volts |
| Input Current | | | | |
| I _{IH} , Logic Loading "1" ① | — | — | 5 | µA |
| I _{IL} , Logic Loading "0" ② | — | — | 5 | µA |
| A/D Clock Pulse Width | | | | |
| T _{PW1} | 25 | — | — | ns |
| T _{PW0} | 25 | — | — | ns |

DIGITAL OUTPUTS

| | | | | |
|-----------------------------------------------------|------|----|----|----|
| Output Logic Current | | | | |
| I _{OH} , Logic "1" ③ | -3.5 | — | — | mA |
| I _{OL} , Logic "0" ④ | 3.5 | — | — | mA |
| Leak Current at \overline{OE} = "1" ⑤ | — | — | 1 | µA |
| 3-State Enable Time, T _{PZE} ⑥ | 10 | 15 | 20 | ns |
| 3-State Disable Time, T _{PEZ} ⑦ | 20 | 25 | 30 | ns |
| Data Delay, T _{DL} (C _L = 20pF) | 8 | 13 | 18 | ns |

PERFORMANCE

| | | | | |
|---------------------------------|----|------|-----|---------|
| Resolution | 10 | — | — | Bits |
| Max. Throughput Rate ⑧ | 20 | — | — | MHz |
| Min. Throughput Rate ⑧ | — | — | 0.5 | MHz |
| Integral Linearity Error | — | ±1.3 | ±2 | LSB |
| Differential Linearity Error | — | ±0.5 | ±1 | LSB |
| Differential Gain Error ⑨ | — | 1.0 | — | % |
| Differential Phase Error ⑨ | — | 0.3 | — | Degrees |
| Aperture Delay, T _{sd} | 2 | 4 | 6 | ns |
| SNR & Distortion | | | | |
| f _{IN} = 100kHz | — | 53 | — | dB |
| f _{IN} = 500kHz | — | 52 | — | dB |
| f _{IN} = 1MHz | — | 53 | — | dB |
| f _{IN} = 3MHz | — | 54 | — | dB |
| f _{IN} = 7MHz | — | 47 | — | dB |
| f _{IN} = 10MHz | — | 45 | — | dB |

| PERFORMANCE (CONT.) | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|------|------|------|-------|
| Spurious Free Dynamic Range | | | | |
| f _{IN} = 100kHz | — | 60 | — | dB |
| f _{IN} = 500kHz | — | 59 | — | dB |
| f _{IN} = 1MHz | — | 60 | — | dB |
| f _{IN} = 3MHz | — | 65 | — | dB |
| f _{IN} = 7MHz | — | 50 | — | dB |
| f _{IN} = 10MHz | — | 49 | — | dB |

POWER REQUIREMENTS

| | | | | |
|------------------------------------------|-------|------|-------|-------|
| Power Supply Voltage | | | | |
| +AV _S | +4.75 | +5.0 | +5.25 | Volts |
| +DV _S | +3.0 | — | +5.25 | Volts |
| DGND - AGND | — | — | 100 | mV |
| Supply Current | | | | |
| Analog, +AIs | 20 | 27 | 34 | mA |
| Digital, +DIs | — | 3 | 5 | mA |
| Standby Current (\overline{CE} = "1") | | | | |
| Analog, +AIs | — | — | 1 | mA |
| Digital, +DIs | — | — | 1 | µA |
| Power Dissipation | — | 150 | — | mW |

PHYSICAL/ENVIRONMENTAL

| | | | | |
|-----------------------------|---------------------|---|------|----|
| Operating Temperature Range | -20 | — | +75 | °C |
| Storage Temperature Range | -55 | — | +150 | °C |
| Weight | 0.2 grams | | | |
| Package | 48-pin plastic LQFP | | | |

Footnotes:

- ① +DV_S = Max., V_{IH} = +DV_S
- ② +DV_S = Max., V_{IL} = 0V
- ③ \overline{OE} = AGND, +DV_S = Min., V_{OH} = +DV_S-0.5V
- ④ \overline{OE} = AGND, +DV_S = Min., V_{OL} = 0.4V
- ⑤ \overline{OE} = +AV_S, +DV_S = Max., V_{OH} = +DV_S, and V_{OL} = 0V
- ⑥ Hi-Z to Active, asynchronous with clock.
- ⑦ Active to Hi-Z, asynchronous with clock.
- ⑧ Fin = 1kHz
- ⑨ NTSC 401RE mod. ramp, fc = 14.3MHz

TECHNICAL NOTES

1. **Caution to ESD:** Since the ADS-325A is a CMOS device, precautions against static electricity should be taken.
2. **+AVs and +DV_S:** While the unit has separate pins for both the analog supply (+AV_S) and the digital supply (+DV_S), a time skew between supplying (or removing) both +AV_S and +DV_S may cause a latch-up problem. DATEL recommends using a common power supply for both +AV_S and +DV_S to avoid latch-up conditions. It is possible to use +3.3V for +DV_S along with +5V for +AV_S. Compared to the single +5V supply application, there will be no significant difference in performance. However, special care should be taken to minimize the time skew between +AV_S and +DV_S when turning on/off.
3. **PC board layout:** To obtain fully specified performance careful attention to PC board layout is required. Place large ground planes on the board and connect both analog and digital grounds at one point right beneath the converter. In the case where the grounds are tied at a location distant from the converter, the voltage difference between the grounds must be within 100mV. Tie all ground pins directly to the appropriate ground plane beneath the converter. Bypass +AV_S and +DV_S pins to ground using 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors at locations as close to the unit as possible.
4. **Reference Input:** Two external voltage references are required for the two reference inputs V_{RT} (pin 29, 30) and V_{RB} (pin 34, 35). Typically, these are +4V for V_{RT} and +2V

for VRB, which give an analog input range of +2V to +4V. The reference voltages must be within the following limitations:

$$+AVS - 0.4V \geq VRT > VRB \geq +1.8V, \text{ and} \\ VRT - VRB > = 1.8V$$

Stability of the reference will directly affect the accuracy of the A/D conversion. In this sense, the reference sources must be capable of driving more than 10mA. Also, the VRT and VRB pins should be bypassed to analog ground with 0.1µF ceramic capacitors placed as close to the pins as possible.

5. **Analog Input:** ADS-325A has a broad input bandwidth of 70MHz (@-1dB) with only 9pF of input capacitance at its analog input. The analog input should be driven by a high speed buffer amplifier with sufficient current drive.
6. **Digital Inputs:** All digital input pins including A/D clock input are CMOS compatible. Each of these pins has an internal overvoltage protection circuit with diodes as shown in Figure 2 (Equivalent circuit diagrams).
7. **Control Logic Inputs:** ADS-325A has several control logic input pins. Functions of these pins are described in the following:

TEST MODE (pin 19), MINV (pin 21), LINV (pin 20)
 These three pins select the output data format. With a combination of these input states the output data takes any form of binary, complementary binary, 2's compliment, or certain test pattern. Refer to Table 1 (Output coding) and Table 2 (Truth table).

CE (Chip Enable, pin 24)
 For normal operation the input to this pin should be logic low. Input high applied to the pin puts the unit into standby mode. In standby mode the unit dissipates only a few milliwatts or less.

OE (Output Enable, pin 23)
 Input logic low applied to this pin enables the three-state output bits (Bit 1 to Bit 10). Input high disables the outputs.

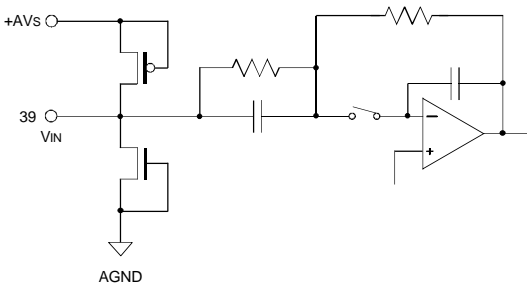
RESET (pin 15)
 This pin can be used to re-initiate start-up calibration. Normally connect this pin to logic high. See Calibration Function for more details.

CAL (Calibration Input, pin 41)
 This pin is the input for an external calibration pulse. See Calibration Function for more details.

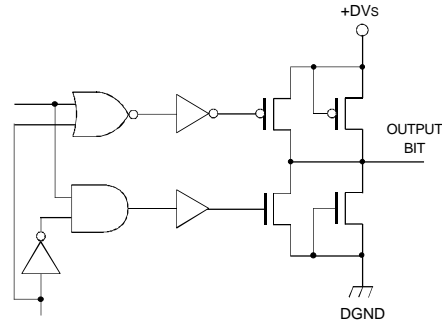
SEL (Select, pin 17)
 Applying logic high to this pin allows use of the internal auto calibration function and blocks out the external pulse from the CAL input. Inputting logic low to the pin disables the internal cal function and allows usage of the external cal pulses.

8. **Test IN/OUT pins:** Test signal input/output pins are used in the production process. The test signal output pins (pin 13, 38) should normally be left open. Tie the test signal input pin 42 to +AVs and the pins 14 and 37 to +AVs or AGND.

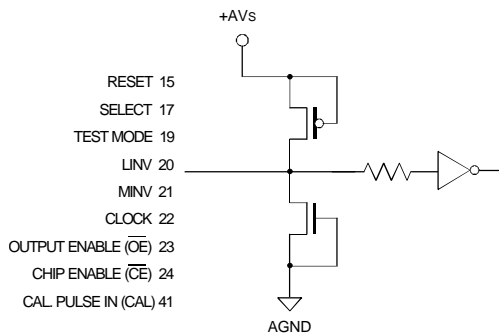
9. **Three-state output buffer:** A/D output buffer (BIT 1 to BIT 10) is a three-state register controlled by the OE pin. The output logic high level is dependent on +DVs.



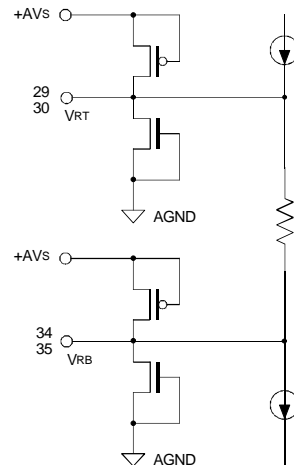
Analog Signal Input



Digital Data Outputs



SEL, CLK, CAL, RESET, OE, CE, Test Mode, LINV and MINV Inputs



Reference Input

Figure 2. Equivalent Circuits

CALIBRATION FUNCTION

To achieve its superior linearity ADS-325A has an internal calibration circuit with a built-in calibration pulse generation circuit and an input pin for an external calibration pulse. The calibration circuit consists of three D/A converters, a pattern generator and an averaging circuit. With either internal or external calibration pulses applied to the calibration circuit, the circuit senses an offset of the x8 gain amplifier and two reference biases supplied from the V_{RT} and the V_{RB} to a fine comparator/encoder block, and compensates them using the three DACs.

With a single negative going calibration pulse a unit cycle of calibration is completed. It is initiated with the negative going edge of the calibration pulse and takes seven A/D clock periods to be completed. Due to the fact that this calibration cycle occupies the lower comparator for four A/D clock periods the lower five bits of the output data remain constant through 4 clock cycles after the completion of the cycle. Figure 3 shows the timing for the calibration cycle.

A sequence of seven unit calibration cycles initiated by seven calibration pulses, completes a single calibration process. The number of calibration processes required depends on the condition of the device and on the stability of the references and the power. Even in worst case, 80 calibration processes done by 560 calibration pulses are enough to finish the whole calibration.

There are three modes of the calibration function. These are:
 a. Start-up calibration function
 b. Internal auto-calibration function
 c. External calibration function

For operation in modes a. and b. the ADS-325A has a built-in calibration pulse generation circuit. Figure 4a. illustrates a simplified block diagram of this circuit.

Start-up Calibration Function

At power-up of the unit the initial calibration process requires over 600 calibration pulses. The internal start-up calibration function automatically generates these pulses when power is first applied to the ADS-325A. To initiate the start-up calibration, the following five conditions must be met. See Figure 4b.

1. The supply voltage +AVs must be at least 2.5 Volts higher than AGND.
2. The voltage difference between V_{RT} and V_{RB} must be at least 1 Volt.
3. The \overline{RESET} pin (pin 15) must be set high.
4. The CE pin (pin 24) must be set low.
5. Condition 1 must be met before condition 2.

Once all of the above conditions have been met, the calibration pulses are generated by counting 16 A/D clock cycles on a 14-bit counter until closing the gate when the carry-out occurs. The time required for the start-up calibration is determined by the following formula:

$$\text{Start-up Calibration Time} = 1/f_{CLK} \times 16 \times 16,384$$

where f_{CLK} is the frequency of the A/D clock input. For example, a clock frequency of 14.3MHz requires a calibration time of 18.3ms.

Table 1. Digital Output Coding

TEST MODE = 1, LINV = 0, MINV = 0

| Analog Input Voltage | Step | Digital Output Code | | |
|----------------------|------|---------------------|------|------|
| | | MSB | MSB | LSB |
| 3.998V | 1023 | 11 | 1111 | 1111 |
| 3.996V | 1022 | 11 | 1111 | 1110 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 3.000V | 512 | 10 | 0000 | 0000 |
| 2.998V | 511 | 01 | 1111 | 1111 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 2.002V | 1 | 00 | 0000 | 0001 |
| 2.000V | 0 | 00 | 0000 | 0000 |

Table 2. Digital Output Truth Table

P = Positive True; N = Negative True (inverted)

| TEST MODE | LINV | MINV | Digital Output | | |
|-----------|------|------|----------------|------|------|
| | | | MSB | MSB | LSB |
| 1 | 0 | 0 | PP | PPPP | PPPP |
| 1 | 1 | 0 | PN | NNNN | NNNN |
| 1 | 0 | 1 | NP | PPPP | PPPP |
| 1 | 1 | 1 | NN | NNNN | NNNN |
| 0 | 1 | 1 | 10 | 1010 | 1010 |
| 0 | 0 | 1 | 11 | 0101 | 0101 |
| 0 | 1 | 0 | 00 | 1010 | 1010 |
| 0 | 0 | 0 | 01 | 0101 | 0101 |

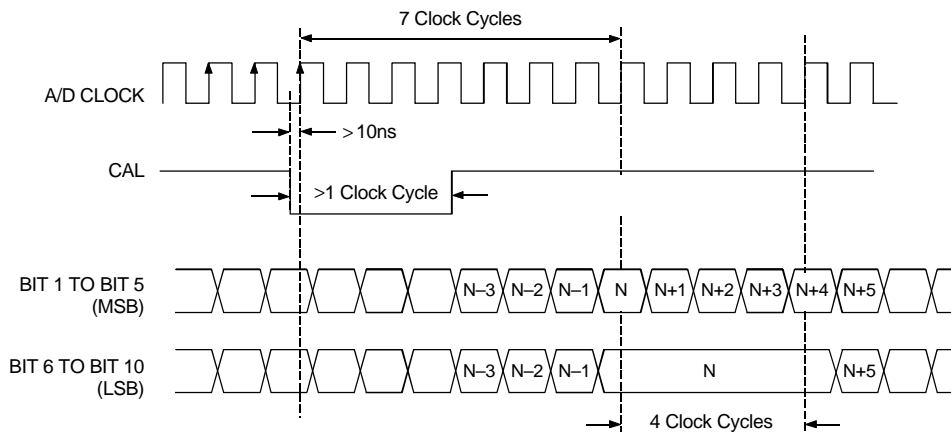


Figure 3. Calibration Timing Diagram

Re-initiating the Start-up Calibration

The start-up calibration function can be re-initiated at any time desired after the power and the references are supplied. Apply a positive pulse to \overline{CE} pin (pin 24) or a negative pulse to RESET pin (pin 15). The pulse width of these pulses must be equal to or wider than one A/D clock cycle. Also due to this feature, you can make sure of a proper start-up calibration at power-up by making a C-R delay connection with the RESET pin as shown in Figure 4c.

Using Start-up Calibration Function Only

Internal and external calibration functions need not be employed after start-up calibration. To use only the start-up calibration function, connect the SEL pin (pin 17) to AGND and the CAL pin (pin 14) to +AVs or AGND.

Auto Calibration Function

After the start up calibration is completed, the internal calibration function can periodically and automatically generate calibration pulses when the auto calibration mode is enabled. To enable this function connect the SEL pin (pin 17) and the CAL pin (pin 41) to +AVs. In this mode a 24-bit counter is counted with every 16 A/D clock cycles and the carry-out is used as the calibration pulse. The period of the calibration pulse generated is as follows:

$$\text{Period of Auto-calibration pulse} = 1/f_{\text{CLK}} \times 16 \times 16,777,216$$

For the case when the A/D clock frequency is 14.3MHz, the calibration pulse generation cycle is 18.8 seconds. Since a single calibration process is performed once every seven pulses, the total calibration cycle is approximately 132 seconds.

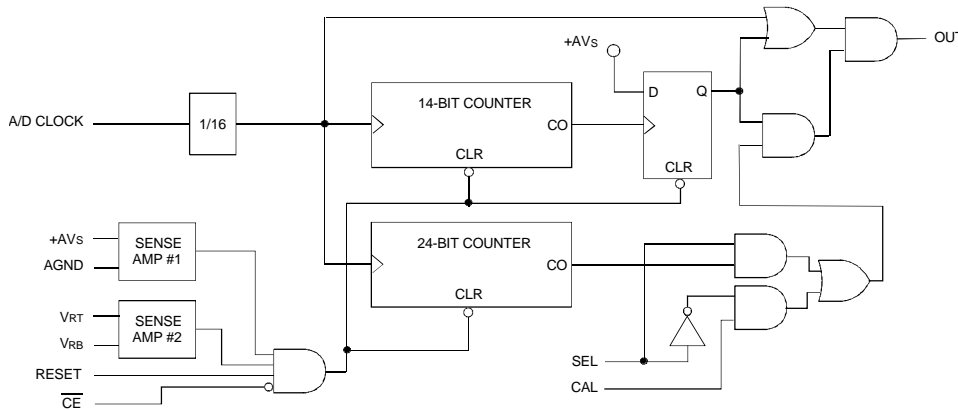


Figure 4a Internal Calibration Pulse Generation Circuit

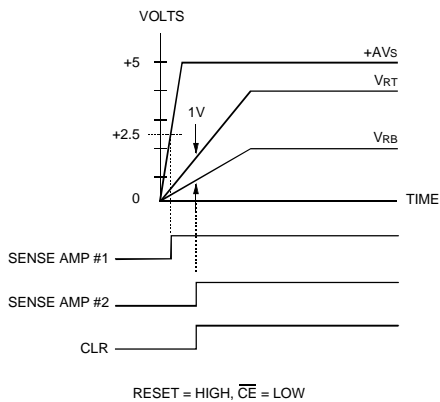


Figure 4b. Conditions for Start-Up Calibration

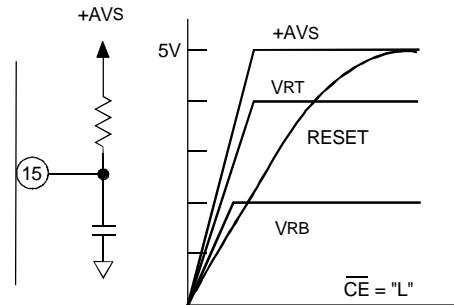


Figure 4c. Start-up Calibration using RESET

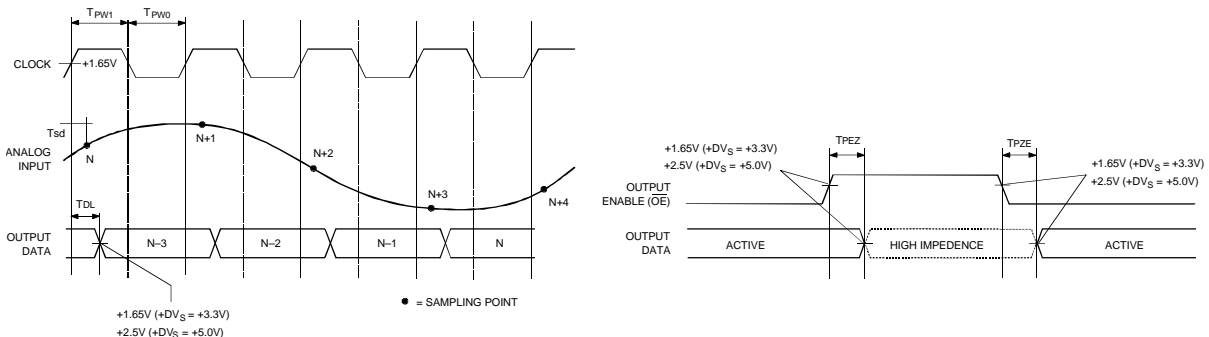


Figure 5. ADS-325A Timing Diagrams

As stated before, the five lower bits of the output data will remain constant for 4 clock cycles with every generation of the calibration pulse. Since the auto calibration pulses are generated asynchronously, this may create problems in certain applications.

External Calibration Function

To avoid the asynchronous data fixation due to the calibration

process, you can disable the internal auto calibration function and use an external calibration pulse which is synchronized with the analog input. Input the external calibration pulse to the CAL pin (pin 14) and tie the SEL pin (pin 17) to AGND. When digitizing a video signal, for example, you can synchronize the external calibration pulses with the V-sync or H-sync cycles of the video signal to avoid losing any data during the video signal cycles. See figure 6a. and 6b.

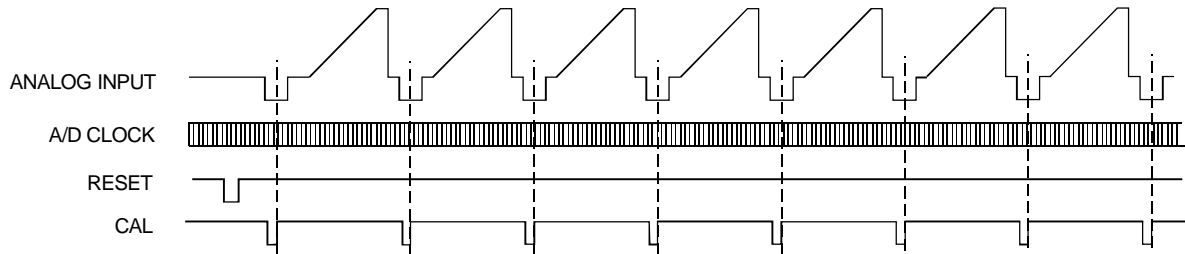


Figure 6a. Applying CAL Pulse Every H Sync.

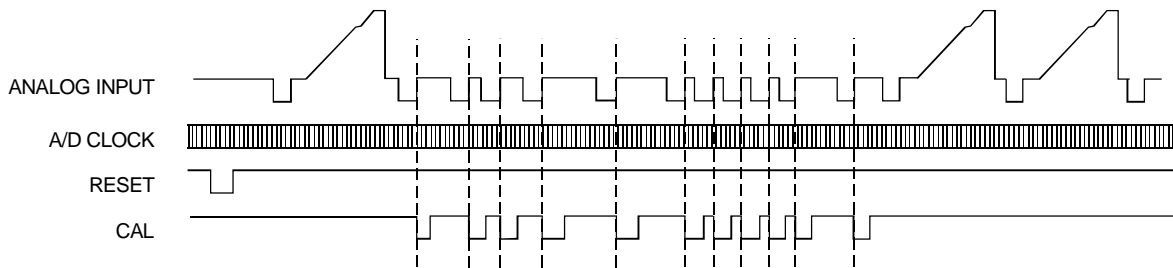
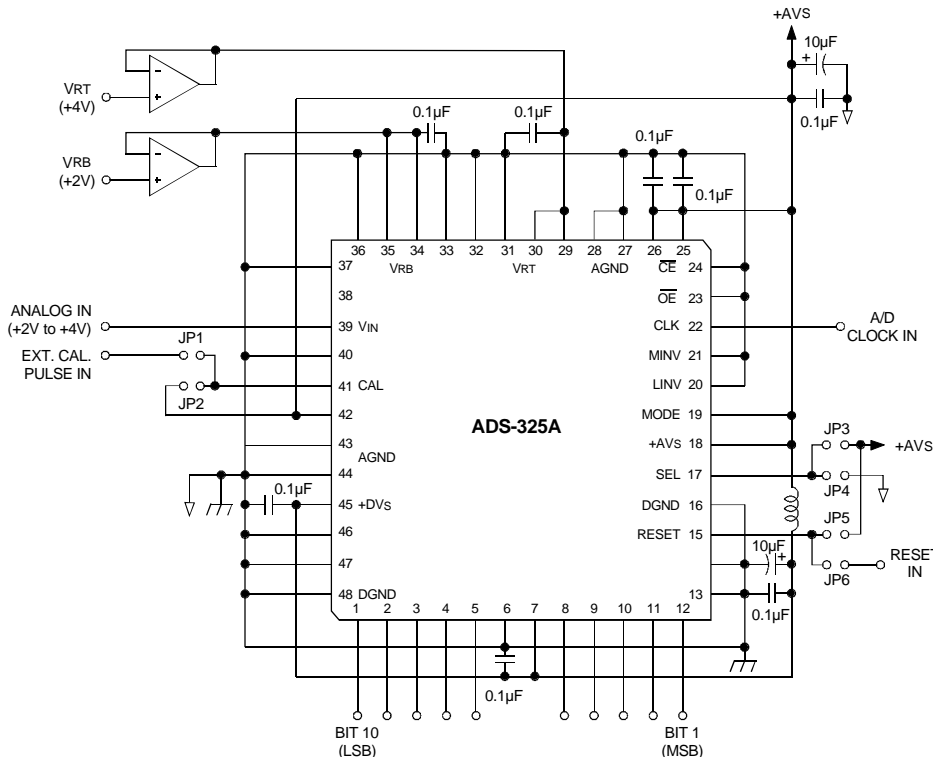


Figure 6b. Applying CAL Pulse Every V Sync.



NOTES:

1. For using Start-up calibration and External CAL Pulse Mode, close JP1 and JP4, and open JP2 and JP3.
2. For using Start-up calibration and Internal Auto-calibration Mode, close JP2 and JP3, and open JP1 and JP3.
3. For using Start-up calibration Mode only, close JP2 and JP4, and open JP1 and JP3.
4. RESET pin (Pin 15) should normally be connected to +AVS (close JP5). To re-initiate the start-up calibration after power-up, close JP6 to apply external RESET pulse.

Figure 7. Typical ADS-325A Connection Diagram

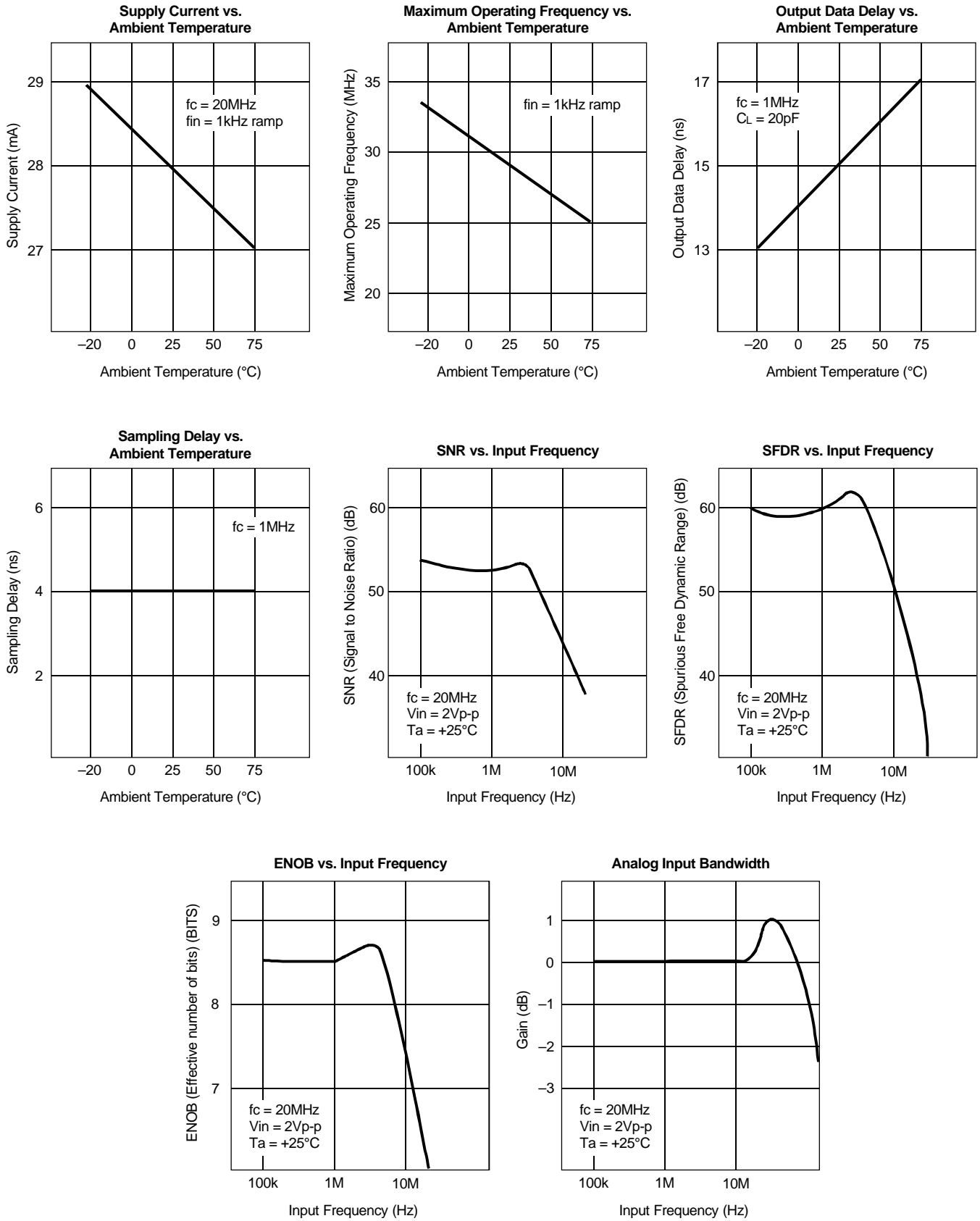
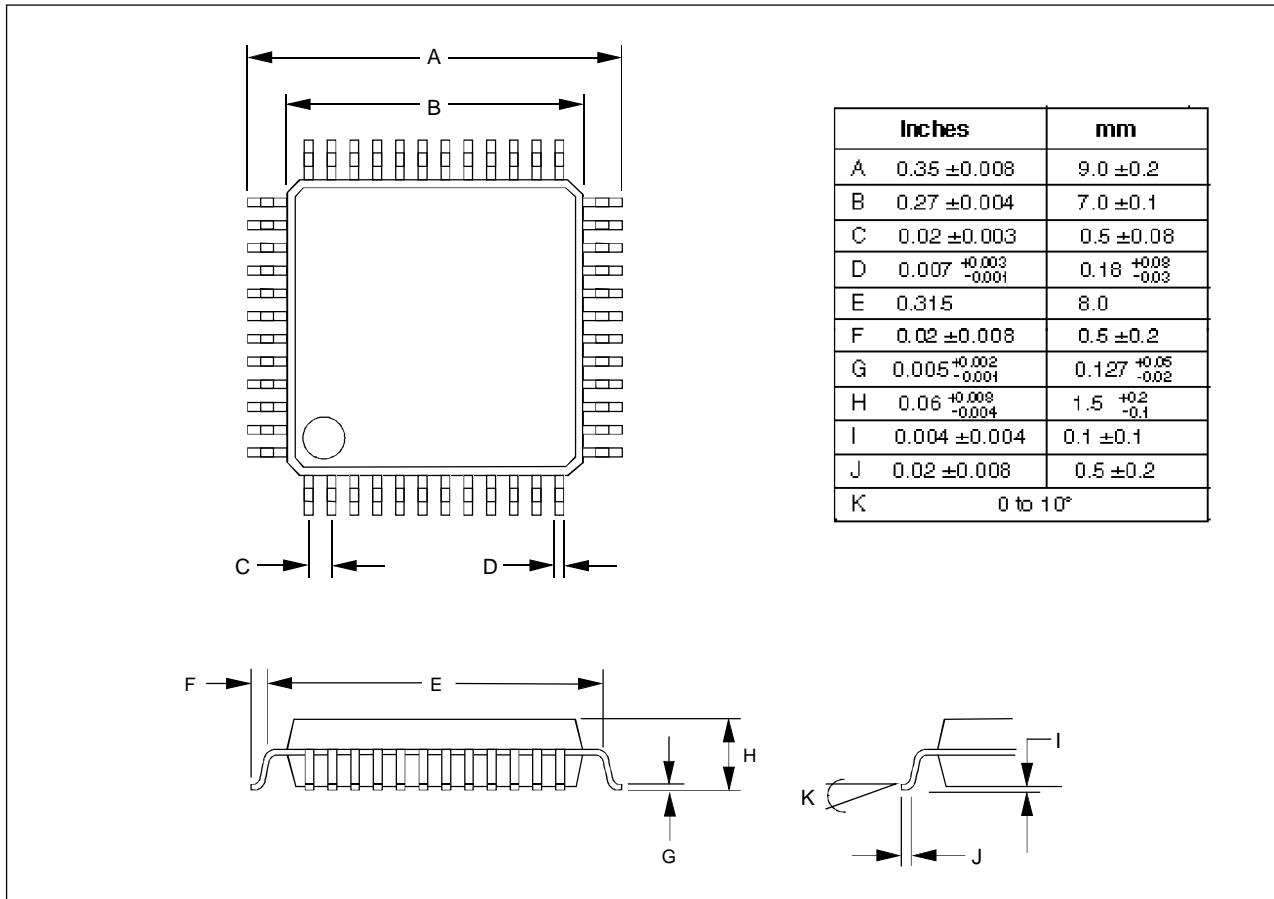


Figure 8. Typical Performance Curves

MECHANICAL DIMENSIONS



ORDERING INFORMATION

| Model Number | Bits/Throughput Rate | Package |
|--------------|----------------------|----------------------|
| ADS-325A | 10 Bits/20MHz | 48-pin, plastic LQFP |