



SANYO Semiconductors

# DATA SHEET

## LV4138W — Bi-CMOS LSI For LCD Panel Drive Single Chip IC

### Overview

The LV4138W is single chip IC for LCD panel drive.

### Functions

- Analog block RGB Decoder/Driver
- Digital block Timing Generator

### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC1 \text{ max}}$	Analog LOW type	6	V
	$V_{CC2 \text{ max}}$	Analog HIGH type	14	V
	$V_{DD \text{ max}}$	Digital type	4.5	V
Allowable power dissipation	$P_d \text{ max}$	$T_a \leq 75^\circ\text{C}$ * Mounted on a board.	350	mW
Operating temperature	$T_{opr}$		-15 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$
Input pin voltage	$V_{INA}$	Analog input pin	-0.3 to $V_{CC1}$	V
	$V_{IND}$	Digital input pin (Except pin 10, 11 and 12)	-0.3 to $V_{DD}+0.3$	V
	$V_{IND}$	Digital input pin (10, 11, 12pin)	-0.3 to +4.5	V

\* : Mounted on a board : 30×30×1.6mm<sup>3</sup>, glass epoxy board

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# LV4138W

## Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC1</sub>	Analog LOW type	3.0	V
	V <sub>CC2</sub>	Analog HIGH type	12.0	V
	V <sub>DD</sub>	Digital type	3.0	V
Operating voltage range	V <sub>CC1op</sub>	Analog LOW type	2.7 to 3.6	V
	V <sub>CC2op</sub>	Analog HIGH type	11 to 13.5	V
	V <sub>DDop</sub>	Digital type	2.7 to 3.6	V

## Input Signal Voltage

Parameter	Symbol	Conditions	Ratings	Unit	
Recommended input signal voltage	Y input signal	Yin	Sync chip - white	0.5	Vp-p
	Color difference input signal	B-Yin	75% Color bar signal	0.3	Vp-p
		R-Yin	75% Color bar signal	0.24	Vp-p

## Electrical DC Characteristics

Unless otherwise specified, settings 1 and 2 must be made.

Unless otherwise specified, V<sub>CC1</sub> = 3.0V, V<sub>CC2</sub> = V<sub>CCPCD</sub> = 12.0V, GND1 = GND2 = GNDPCD = 0, V<sub>DD1</sub> = V<sub>DD2</sub> = 3.0V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0, Ta = 25°C

### [Current Characteristics]

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Current dissipation V <sub>CC1</sub> , analog LOW	I <sub>CC1</sub>	Enter SIG4 to (A), (D) and (E). Measure the current value of I <sub>CC1</sub> .	TRAP OFF	18	26	33	mA
			TRAP ON	20	28	35	mA
Current dissipation V <sub>CC2</sub> , analog HIGH	I <sub>CC2</sub>	Enter SIG4 to (A) and SIG2 (0dB) to (B). Measure the current value of I <sub>CC1</sub> .	4.5	8	11	mA	
Current dissipation V <sub>DD</sub> , logic	I <sub>DD1</sub>	Enter SIG4 to (A) and SIG2 (0dB) to (B). Measure the current value of I <sub>DD11</sub> and I <sub>DD21</sub> . I <sub>DD1</sub> , I <sub>DD2</sub> , I <sub>DD3</sub> = I <sub>DD11</sub> +I <sub>DD21</sub>	L1, L2 mode	7	10	13	mA
	I <sub>DD2</sub>		H mode	8.5	12	15.5	mA

### [Digital block input/output characteristics]

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
L-level input voltage	V <sub>IL</sub>	Digital block input pin (Note 1)			0.3V <sub>DD</sub>	V
H-level input voltage	V <sub>IH</sub>	Digital block input pin (Note 1)	0.7V <sub>DD</sub>			V
H-level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -1.2mA (Note 2)	V <sub>DD</sub> - 0.2			V
L-level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 1.2mA (Note 2)			0.3	V
Output transition time	t <sub>TLH</sub>	Load 50pF (see Fig. 3)			30	ns
	t <sub>THL</sub>				30	ns
Cross point time difference	ΔT	Load 50pF CKH1/CKH2 and CKV1/CKV2 and CKH3/CKH4 (See Fig. 4)			10	ns
CHK duty	DTYHC	Load 50pF Measure the duty of CKH1, CKH2, CKH3 and CKH4.	47	50	53	%

(Note 1) Digital block input pins : LOAD, DATA, SCLK

(Note 2) Digital block output pins : Pins 15 to 31, 33, 34

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## Electrical AC Characteristics (1)

Unless otherwise specified, the setting 1 and 2 must be made.

Unless otherwise specified,  $V_{CC1} = 3.0V$ ,  $V_{CC2} = V_{CCPCD} = 12.0V$ ,  $GND1 = GND2 = GNDPCD = 0$ ,

$V_{DD1} = V_{DD2} = 3.0V$ ,  $V_{SS1} = V_{SS2} = 0$ ,  $T_a = 25^\circ C$

Unless otherwise specified, measure the non-inverted output of TP40, TP43, and TP45.

[Y signal system]

Parameter	Symbol	Conditions	min	typ	max	unit		
Contrast characteristics, TYP	GCNTTP	Enter SIG4 to (A) and measure the ratio between the output amplitude (white to black) and input amplitude of TP43.	14	16	18	dB		
Contrast characteristics, MIN	GCNTMN	Enter SIG4 to (A) and measure the ratio between the output amplitude (white to black) and input amplitude of TP43.	-2	1	4.5	dB		
Max. video gain	GV	Enter SIG4 to (A) and measure the ratio between the output amplitude (white to black) and input amplitude of TP43.	19	21	23	dB		
Y signal frequency characteristics	FTRPN0	Assume that the output amplitude of TP43 when SIG1 (0dB, no burst, 100kHz) is entered to (A) is 0dB. Change the input signal frequency to change and determine the frequency at which the output amplitude becomes -3dB. $C_L = 200pF$	TRAP OFF		6.0		MHz	
	FTRPNT		TRAP ON	NTSC	3.0			
	FTRPPL		PAL	3.5				
Picture quality adjustment variable amount 1 (TRAP OFF) H mode	GSHP1X	Assume that the output amplitude of TP43 when SIG7 (100kHz) is entered in (A) is 0dB. Determine the output amplitude ratio of the input SIG7 (2.5MHz).	MAX	11	14		dB	
	GSHP1N		MIN		-3	0		
Picture quality adjustment variable amount 2 (TRAP OFF) L1, L2 mode	GSHP2X	Assume that the output amplitude of TP43 when SIG7 (100kHz) is entered in (A) is 0dB. Determine the output amplitude ratio of the input SIG7 (1.8MHz).	MAX	11	14		dB	
	GSHP2N		MIN		-1	2		
Picture quality adjustment variable amount 3 (TRAP ON) L1, L2 mode	GSHP3X	Assume that the output amplitude of TP43 when SIG7 (100kHz) is entered in (A) is 0dB. Determine the output amplitude ratio of the input SIG7 (1.8MHz).	MAX	8	11		dB	
	GSHP3N		MIN		-5	-2		
Picture quality adjustment variable amount 4 (TRAP ON) H mode	GSHP4X	Assume that the output amplitude of TP43 when SIG7 (100kHz) is entered in (A) is 0dB. Determine the output amplitude ratio of the input SIG7 (2.0MHz).	MAX	6	9		dB	
	GSHP4N		MIN		-6	-3		
Y signal input/output delay rate	TDYTRN	Enter SIG9 to (A). Measure the delay time from the input signal 2T pulse peak to the peak of TP43 non-inverted output.	TRAP ON		200	300	400	ns
	TDYTRP		TRAP OFF		250	350	450	ns

[Color difference signal system]

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Color difference input color adjustment	GEXCMX	Input SIG5 ( $V_L = 0mV$ ) to (A) and SIG1 (0dB, 100kHz, no burst) to (D) and assume that the output amplitude (100kHz) of TP40 when COL = 128 is VCOCOL = 0 is VC2. Assume also that the output amplitude of TP40 when SIG1 is -10dB and COL=255 is VC1. Calculate as follows : GEXCMX = $20\log(V_{C1}/V_{C0})+10$ GEXCMN = $20\log(V_{C2}/V_{C0})$	+3	+5		dB
	GEXCMN			-20	-15	dB
Color difference balance	VEXCBL	Input SIG5 ( $V_L = 0mV$ ) to (A) and SIG1 (0dB, 100kHz, no burst) to (D) and (E). Assume that the output amplitude (100kHz) of TP40 is VB and that (100kHz) of TP45 is VR. Calculate as follows : VEXCBL = $VR/VB$	0.8	1.0	1.2	

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## [Color difference signal system]

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Color difference input balance adjustment R	GEXRMX	Input SIG5 ( $V_L = 0\text{mV}$ ) to (A) and SIG1 (-6dB, 100kHz, no burst) to (D) and (E). Assume that the output amplitude (100kHz) of TP45 and that of TP40 when TINT = 128 are VRO and VB0 respectively. The output amplitude of TP45 and that of TP40 when TINT = 255 are VR1 and VB1 respectively. Assume also that the output amplitude of TP45 and that of TP40 when TINT = 0 are VR2 and VB2 respectively. Then, calculate as follows : GEXRMX = $20\log(VR1/VRO)$ GEXRMN = $20\log(VR2/VRO)$ GEXBMX = $20\log(VB1/VB0)$ GEXBMN = $20\log(VB2/VB0)$		-5	-2	dB	
	GEXRMN		+2	+3		dB	
Color difference input balance adjustment B	GEXBMX	Input SIG5 ( $V_L = 0\text{mV}$ ) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume that the output amplitude (100kHz) of TP40 is VEXB and that of TP43 is VEXBG. Calculate as follows : EXGB = $VEXBG/VEXB$	+2	+3		dB	
	GEXBMN			-5	-2	dB	
G-Y matrix characteristics	VEXGBN	Input SIG5 ( $V_L = 0\text{mV}$ ) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume that the output amplitude (100kHz) of TP40 is VEXB and that of TP43 is VEXBG. Calculate as follows : EXGB = $VEXBG/VEXB$	NTSC	0.23	0.26	0.29	
	VEXGBP		PAL	0.17	0.20	0.23	
	VEXGR	Input SIG5 ( $V_L = 0\text{mV}$ ) to (A) and SIG1 (0dB, 100kHz, no burst) to (E). Assume that the output amplitude (100kHz) of TP45 is VEXR and that of TP43 is VEXRG. Calculate as follows : VEXGR = $VEXRG/VEXR$		0.46	0.51	0.56	

## [RGB signal system]

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RGB signal and PCD output DC voltage	VOUT	Enter SIG5 ( $V_L = 0\text{mV}$ ) to (A) and adjust BRIGHT and PCD-BRT of serial bus to set TP43 and TP38 output to 9Vp-p. Then, measure the DC voltage of TP38, TP40, TP43, and TP45.	5.8	6.0	6.2	V
RGB signal and PCD output DC voltage difference	$\Delta\text{VOUT}$	Determine the maximum value of difference of measured values of TP40, TP43, TP45, and TP38 of VOUT as described in the above item.		0	120	mV
SIGCENT variable range	VCNT	Confirm that setting V48 to 5.2V or 6.5V in the VOUT measurement conditions proves compliance with the above $\Delta\text{VOUT}$ and that $ V48 - \text{VOUT}  \leq 0.2\text{V}$ .	5.2	0	6.5	V
User brightness change rate	UBRTMX	Measure the change rate of the black level of TP40, TP43, and TP45 outputs when SIG3 is entered to (A) and U-BRT is changed from 128 to 255.	2.0	3.0		V
	UBRTMN	Measure the change rate of the white level of TP40, TP43, and TP45 outputs when SIG3 is entered to (A) and U-BRT is changed from 128 to 0.		-3	-2.0	V
Brightness change rate	BRTMX	Measure the change rate of the black level of TP40, TP43, and TP45 outputs when SIG3 is entered to (A) and BRT is changed from 128 to 255.	2.0	2.5		V
	BRTMN	Measure the change rate of the white level of TP40, TP43, and TP45 outputs when SIG3 is entered to (A) and BRT is changed from 128 to 0.		-2.5	-2.0	V
PCD output change rate	PCDMX	Enter SIG3 to (A), and measure the TP38 output amplitude when PCD-BRT = 255.	9.0			Vp-p
	PCDMN	Enter SIG3 to (A), and measure the TP38 output amplitude when PCD-BRT = 0.			1.5	Vp-p

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Sub-brightness R change rates	SBBRTR	Enter SIG5 ( $V_L = 0mV$ ) to (A) and measure the difference between the black level of TP45 output when R-BRT = 128 and the black level of output when R-BRT = 0 and R-BRT = 255.	$\pm 1.3$	$\pm 1.7$		V
Sub-brightness B change rates	SBBRTB	Enter SIG5 ( $V_L = 0mV$ ) to (A) and measure the difference between the black level of TP40 output when B-BRT = 128 and the black level of output when B-BRT = 0 and B-BRT = 255.	$\pm 1.3$	$\pm 1.7$		V
Gain difference between RGB signals	$\Delta GRGB$	Determine the level difference of non-inverted output amplitude (white to black) of TP40, TP43, and TP45 when SIG4 is entered to (A).	-0.6	0	0.6	dB
Sub-contrast R change rate	SBCNTR	Measure the non-inverted output (white to black) of TP45 for the non-inverted output (white to black) of TP43 when SIG4 is entered to (A) and when R-CNT = 0 and R-CNT = 255.	$\pm 2.0$			dB
Sub-contrast B change rate	SBCNTB	Input SIG4 to (A) and measure the difference of the level for B-CNT = 0 and 255 from the TP40 non-inverted output (white to black) when B-CNT = 128.	$\pm 2.0$			dB
RGB inverted/non-inverted gain difference	$\Delta GINV$	Determine the difference of inverted output amplitude for the non-inverted output amplitude (white to black) of TP40, TP43, and TP45 when SIG4 is entered to (A).	-0.5	0	0.5	dB
Black level potential difference between RGB signals	$\Delta VBL$	Determine the difference between highest and lowest black levels for inverted and non-inverted outputs of TP40, TP43, and TP45 when SIG4 is entered to (A).			300	mV
Gamma gain	$G_{\gamma L}$	Enter SIG8 to (A) and set the amplitude (black to white) of non-inverted output of TP43 to 3.5Vp-p with CONT and set the level to 1.5V through BRIGHT adjustment. Measure VG1, VG2, and VG3 and calculated as follows : $G_{\gamma L} = 20\log(VG1/0.0357)$ $G_{\gamma M} = 20\log(VG2/0.0357)$ $G_{\gamma H} = 20\log(VG3/0.0357)$ (See Fig. 5)	23.0	26.0	29.0	dB
	$G_{\gamma M}$		12.0	15.0	18.0	dB
	$G_{\gamma H}$		18.0	22.0	26.0	dB
$\gamma 1$ adjustment variable range	$V_{\gamma 1MN}$	Enter SIG8 to (A) and set the TP43 output (black to black) to 9Vp-p through BRIGHT adjustment. Read the $\gamma$ gain change point at $\gamma 1 = 0$ , $\gamma 1 = 255$ by referring to the IRE level of input signal : $V_{\gamma 1MN}$ for $\gamma 1 = 0$ $V_{\gamma 1MX}$ for $\gamma 1 = 255$			0	IRE
	$V_{\gamma 1MX}$		100			IRE
$\gamma 2$ adjustment variable range	$V_{\gamma 2MN}$	Enter SIG8 to (A) and set the TP43 output (black to black) to 9Vp-p through BRIGHT adjustment. Read the $\gamma$ gain change point at $\gamma 2 = 0$ , $\gamma 2 = 255$ by referring to the IRE level of input signal : $V_{\gamma 2MN}$ for $\gamma 2 = 0$ $V_{\gamma 2MX}$ for $\gamma 2 = 255$	100			IRE
	$V_{\gamma 2MX}$				0	IRE
PCD transition time	tPCDH	Enter SIG4 to (A) and set the output amplitude of TP38 to 9Vp-p. Measure tPCDH for rise and tPCDL for fall. Load : 20000pF		1.5	3	$\mu s$
	tPCDL			1.5	3	$\mu s$
RGB output whitelimiter level	VWL	Enter SIG3 to (A) and measure the amplitude of the white side limiter level of inverted/non-inverted TP43 output.	1.1	1.4	1.7	Vp-p
RGB output black limiter variable range	VBLIMX	Enter SIG3 to (A) and measure the amplitude of the black side limiter level of inverted/non-inverted TP43 output. VBLIMX for BLIM = 255 and VBLIMN for BLIM = 0	5.4	5.9	6.4	Vp-p
	VBLIMN		9.0			Vp-p
White limiter DC voltage	VW LIM	Enter SIG5 ( $V_L = 0mV$ ) to (A) and measure the DC voltage of TP40, TP43, and TP45.	5.8	6.0	6.2	V

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Black limiter DC voltage	VBLIM	Input SIG5 ( $V_L = 350\text{mV}$ ) to (A) and adjust BLIM to set the output of TP43 and TP40 to 9Vp-p. Measure the DC voltage of TP40, TP43, and TP45.	5.8	6.0	6.2	V

## [Filter characteristics]

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
TRAP attenuation amount	ATRAPH	Input SIG2 (0dB, 3.58MHz and 4.43MHz) in (A) and measure the TP43 output with a spectrum analyzer. Assuming that the TP43 amplitude in the TRAP ON mode is 0dB, determine the attenuation in the COMP input mode.		-15	-20	dB
	ATRAPP			-15	-20	dB
R-Y, B-Y LPF characteristics	DEMLPF	Input SIG5 ( $V_L = 150\text{mV}$ ) in (A) and SIG1 (100kHz) in (B). In this case, assume that the amplitude of 100kHz component of TP40, TP45 output is 0dB. Change the SIG1 frequency at which the output amplitude of TP40, TP45 becomes -3dB.	1.2	1.6	1.9	MHz

## [Sync separation, TG system]

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input sync signal width sensitivity	WSSEP	Enter SIG5 ( $V_L = 0\text{mV}$ , $V_S = 143\text{mV}$ , WS variable) to (A) and confirm synchronization with the TP24 HD output. Narrow WS of SIG5 from 4.7 $\mu\text{s}$ and determine WS at which synchronization between the input and TP24HD output is lost.	2.0			$\mu\text{s}$
Sync separation input sensitivity	VSSEP	Enter SIG5 ( $V_L = 0\text{mV}$ , WS = 4.7 $\mu\text{s}$ , VS variable) to (A) and confirm synchronization with the TP24 HD output. Reduce VS of SIG5 from 143mV and determine VS at which synchronization between the input and TP24HD output is lost.		40	60	mV
Sync separation output delay rate	TDSYL	(A) and measure the delay rate from TP6RPD output. Assume that TDSYL is for a period from fall of input HSYNC to fall of RPD output and that TDSYH is for the period up to rise of RPD output.	300	500	700	ns
	TDSYH		4.7	5.0	5.3	$\mu\text{s}$
Horizontal pull-in range	HPLLN	Enter SIG5 ( $V_L = 0\text{mV}$ , WS = 4.7 $\mu\text{s}$ , and $V_S = 143\text{mV}$ , horizontal frequency variable) to (A) and confirm synchronization with TP24 HD output. Change the horizontal frequency of SIG5 and determine the frequency $f_H$ at which synchronization is established from the condition in which input / output synchronization is lost. Calculate as follows : $HPLLN = f_H - 15734$ $HPLLP = f_H - 15625$	NTSC	$\pm 500$		Hz
	HPLLP		PAL	$\pm 500$		Hz



## Conditions of setting to measure the electric characteristics

Following settings must be made before measurement of electric characteristics.

### Setting 1. System reset

Turn ON SW58 and start V58 from GND in order to perform system reset for MOS block.

(See fig. 1-1.)

The default value is set for the serial bus.

### Setting 2. Horizontal AFC adjustment

Enter SIG5 ( $V_L = 0mV$ ) to (A) and adjust VCOADJ so that the width of WL and

WH becomes equal in the TP9 output waveform. (See fig. 1-2.)

(Note) In order to measure the 2MHz or more band for measurement items, such as the Y-system frequency characteristics or sharpness characteristics, it is necessary to pass through the sample hold circuit via serial bus.

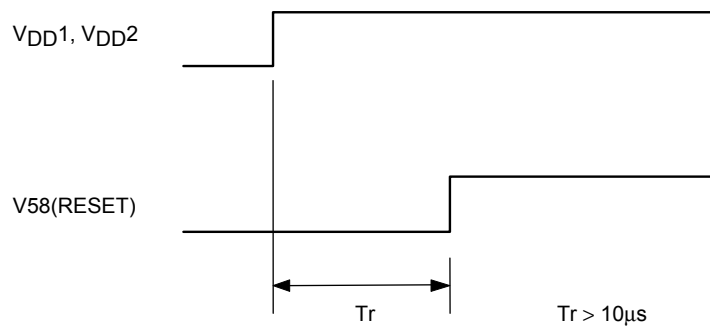


Fig.1-1 System reset

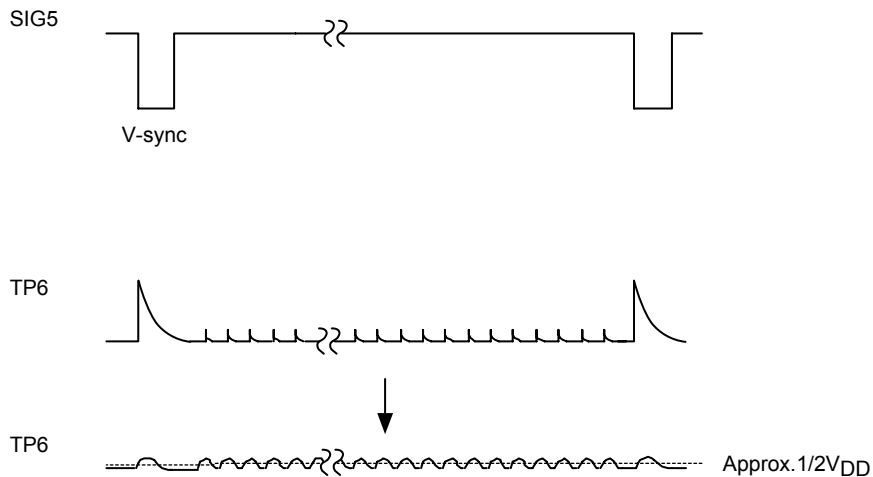


Fig.1-2 Horizontal AFC adjustment



Electric characteristics measurement method

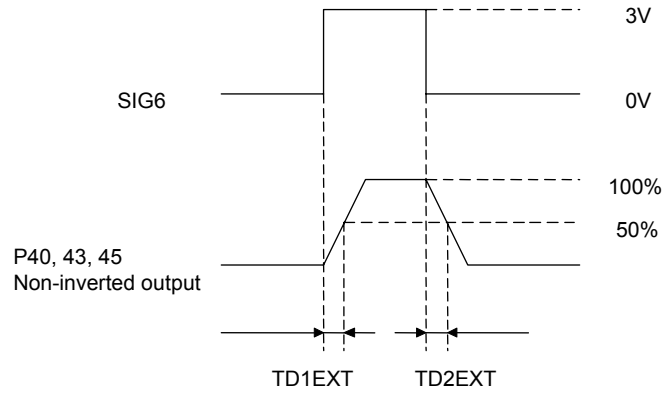


Fig.2 Delay between external RGB input/output

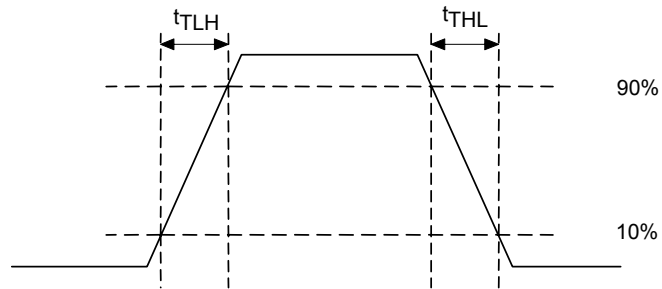


Fig.3 Output transition time measurement conditions

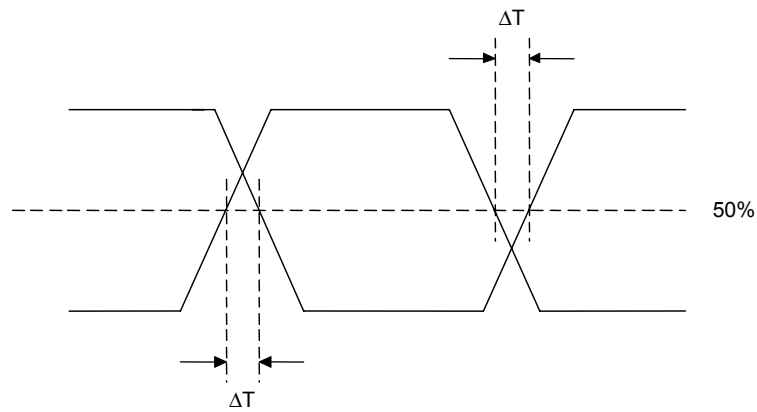


Fig.4 Cross point time difference measurement conditions

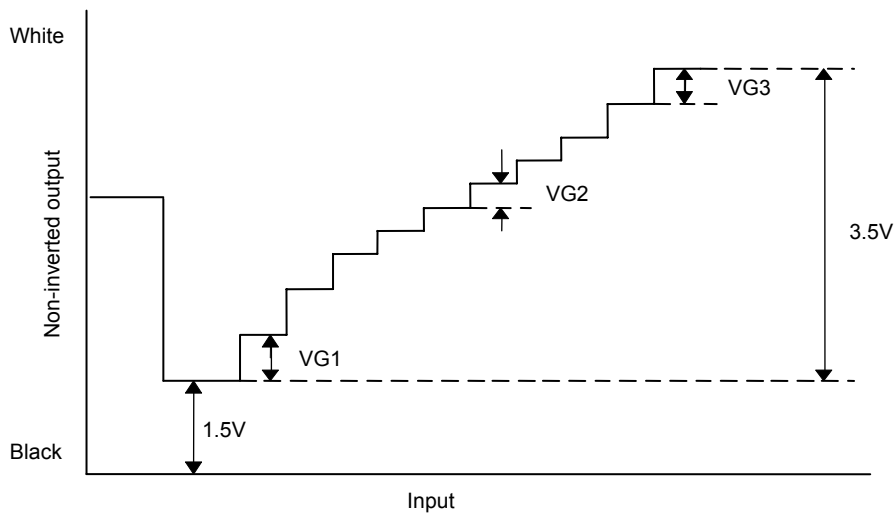
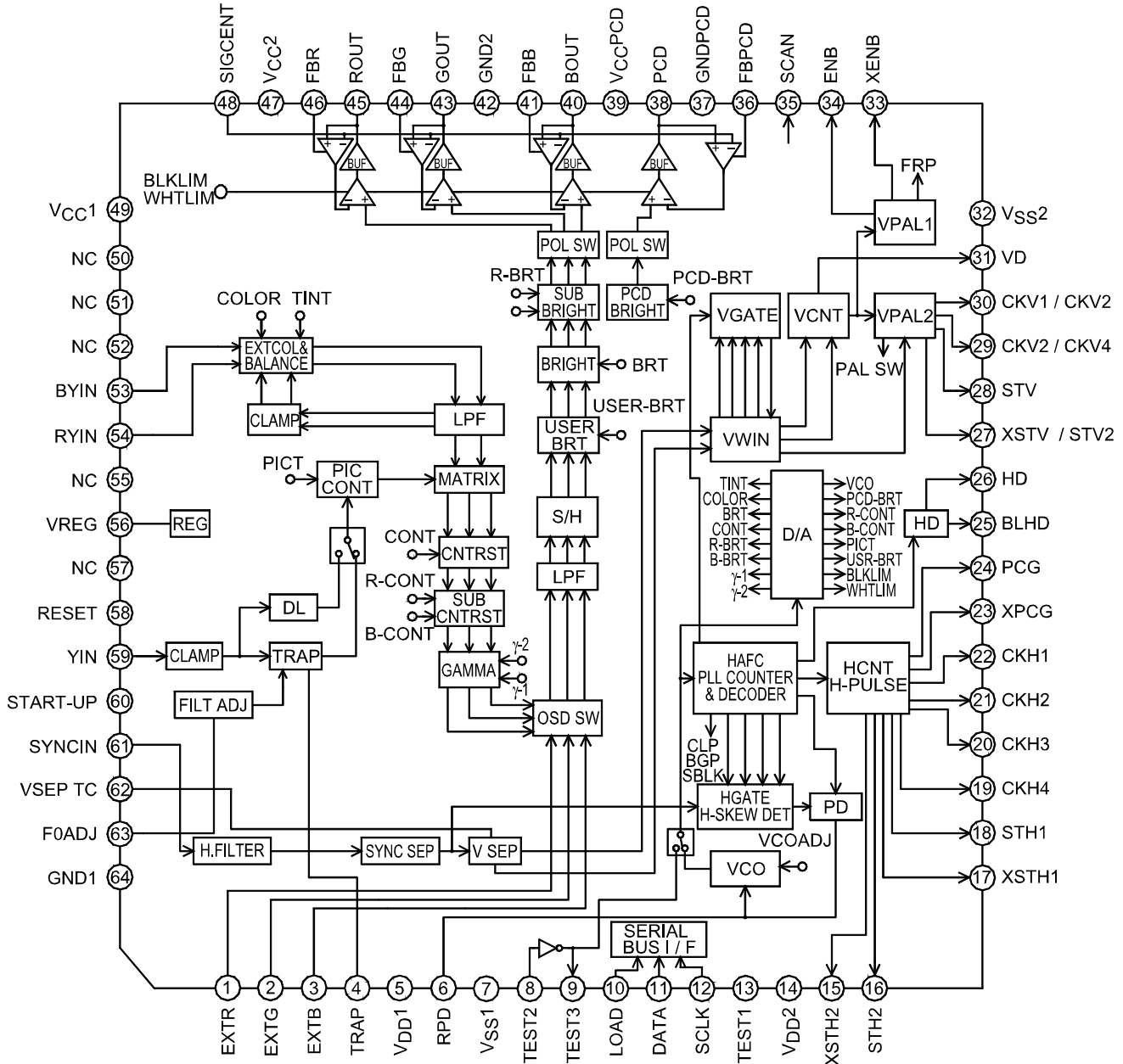


Fig.5  $\gamma$  characteristics measurement conditions

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## Block Diagram



## Pin Description

Pin No.	Pin Name	I/O	Pin Description	Common	For MONI only	For EVF only
1	EXTR	I	External digital R input (used also for the test)	○		
2	EXTG	I	External digital G input (used also for the test)	○		
3	EXTB	I	External digital B input (used also for the test)	○		
4	TRAP	O	External trap connection pin	○		
5	VDD1		Oscillator cell input (3V)	○		
6	RPD	O	Phase comparison output	○		
7	VSS1		Oscillator cell GND	○		
8	TEST2	I	Test pin 2	○		
9	TEST3	O	Test pin 3	○		
10	LOAD	I	Load input for serial bus	○		
11	DATA	I	Data input for serial bus	○		
12	SCLK	I	Clock input for serial bus	○		
13	TEST1	I	Test pin 1	○		
14	VDD2		Digital 1 system power supply (3V)	○		

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Pin No.	Pin Name	I/O	Pin Description	Common	For MONI only	For EVF only
15	XSTH2	O	EVF H-start reverse phase output			○
16	STH2	O	EVF H-start output			○
17	XSTH1	O	Monitor H-start reverse phase output		○	
18	STH1	O	Monitor H-start output		○	
19	CKH4	O	EVF H-clock 2 output			○
20	CKH3	O	EVF H-clock 1 output			○
21	CKH2	O	Monitor H-clock 2 output		○	
22	CKH1	O	Monitor H-clock 1 output		○	
23	XPCG	O	Precharge timing reverse phase output	○		
24	PCG	O	Precharge timing output	○		
25	BLHD	O	Backlight HD output	○		
26	HD	O	H drive output	○		
27	XSTV/STV2	O	V-start reverse phase output/EVF V start output	○		(○)
28	STV	O	V start output	○	(○)	
29	CKV2/CKV4	O	V clock 2 output/EVF CKV2	○		(○)
30	CKV1/CKV2	O	V clock 1 output/Monitor CKV2	○	(○)	
31	VD	O	V drive output	○		
32	VSS2		Digital 1 system GND	○		
33	XENB	O	Enable reverse-phase output	○		
34	ENB	O	Enable output	○		
35	SCAN	O	For scan selection (for monitor)		○	
36	FBPCD	I	Time constant pin for precharge output DC return	○		
37	GNDPCD		Ground for precharge output	○		
38	PCD	O	Precharge output	○		
39	VCCPCD		Precharge output power supply (12V)	○		
40	BOUT	O	B output	○		
41	FBB	I	Time constant pin for B-output DC return	○		
42	GND2		12V ground	○		
43	GOUT	O	G output	○		
44	FBG	I	Time constant pin for G-output DC return	○		
45	ROUT	O	R output	○		
46	FBR	I	Time constant pin for R-output DC return	○		
47	VCC2		12V power supply	○		
48	SIGCENT	I	Output DC level setting pin	○		
49	VCC1		Analog 3V power supply	○		
50	NC	-				
51	NC	-				
52	NC	-				
53	BYIN	I	B-Y input	○		
54	RYIN	I	R-Y input	○		
55	NC	-				
56	VREG	O	Reference voltage	○		
57	NC	-				
58	RESET	I	System reset	○		
59	YIN	I	Brightness signal input	○		
60	START-UP	I	Power-ON blanking time constant pin	○		
61	SYNCIN	I	Sync input	○		
62	VSEPTC		Time constant and external VD input for vertical sync separation	○		
63	F0ADJ	O	Filter F0 adjustment	○		
64	GND1		3V ground	○		

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## Analog pin function description

Pin No.	Pin Name	Pin Voltage	Pin Description	Equivalent Circuit
1 2 3	EXTR EXTG EXTB	-	The external digital signal is entered. All of RGB outputs become the black level when the threshold value is about 0.7V for Vth1 and about 1.8V for Vth2 and any one of RGB exceeds Vth1 and become the white level only for the output in which the input exceeds Vth2. Connect to the ground when not using.	
4	TRAP	1.0V	External trap pin. Trap can be inserted into Y-signal by connecting L and C in series to GND when TRAP ON is set.	
13	TEST1	-	Test pin. Connect this pin normally to GND for use.	
35	SCAN	-	Scan select control output pin. Output from the open collector	
36	FBPCD	1.5V	Feedback circuit smoothing capacitor pin for precharge output DC level control. Because of high impedance, a capacitor with small leakage is used.	
37	GNDPCD	0V	Precharge ground.	
38	PCD	VCC2/2	Precharge output.	
39	VCCPCD	12V	Power supply for precharge output.	

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Continued from preceding page.

Pin No.	Pin Name	Pin Voltage	Pin Description	Equivalent Circuit
40 43 45	BOUT GOUT ROUT	$V_{CC2}/2$	RGB primary color signal output.	
41 44 46	FBB FBG FBR	1.5V	Feedback circuit smoothing capacitor pin for RGB output DC level control. Because of high impedance, a capacitor with small leakage is used.	
42	GND2	0V	$V_{CC2}$ ground.	
47	$V_{CC2}$	12V	12V power supply.	
48	SIGCENT	$V_{CC2}/2$	Apply external voltage (5.2 to 6.5V) when the signal output DC voltage is to be used for those other than $1/2 V_{CC2}$ .	
49	$V_{CC1}$	3.0V	Analog 3V power supply.	
53 54	BYIN RYIN	1.7V	Enter the color difference of R-Y/B-Y. The clamp level in this case is about 1.7V.	
56	VREG	2.0V	Regulator output pin. Connect an external capacitor of 1µF or more.	

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Pin No.	Pin Name	Pin Voltage	Pin Description	Equivalent Circuit
58	RESET	-	C-MOS circuit reset pin. Normally, connect a capacitor between this pin and GND during use. (Threshold value = 2.0V)	
59	YIN	1.6V	Y signal input pin. The standard input signal level is 0.5Vp-p (from sync chip to 100% white).	
60	START-UP	-	Time constant connection pin to set the RGB output to the black level at power ON. Connect the pin to VDD2 when not using. (Threshold value = 2.0V)	
61	SYNCIN	1.6V	Input pin for sync separation.	
62	VSEPTC	1.7V	Time constant connection pin for vertical sync separation. (The pin is used also for external VD input.)	
63	f0ADJ	1.5V	Reference current generation pin for filter. 15 kΩ is connected between this pin and GND to generate the reference current. (Keep the pin open for trap OFF mode.)	
64	GND1	0V	3V ground.	

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## Digital pin function description

Pin No.	Pin Name	Pin Voltage	Equivalent Circuit	Pin Description
5	VDD1	-	Power supply dedicated for VCO.	
6	RPD	-	Phase comparator output.	
7	VSS1	0	Digital ground for VCO.	
8	TEST2	-	Test pin. Normally, connect the input side (TEST2) to GND during use.	
9	TEST3	-		
10	LOAD	-	Serial bus input pin.	
11	DATA	-		
12	SCLK	-		
14	VDD2	-	Digital output pin.	
15	XSTH2	-	Digital output pin.	
16	STH2	-		
17	XSTH1	-		
18	STH1	-		
19	CKH4	-		
20	CKH3	-		
21	CKH2	-		
22	CKH1	-		
23	XPCG	-		
24	PCG	-		
25	BLHD	-		
26	HD	-		
27	XSTV/STV2	-		
28	STV	-		
29	CKV2/CKV4	-		
30	CKV1/CKV2	-		
31	VD	-		
33	XENB	-		
34	ENB	-		
32	VSS2	0	Digital ground.	

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No.	Parameter	Symbol	Input signal, condition, etc.	SW set								Mode set			DAC set														
				1	2	3	48	53	54	58	System	Panel	TRAP	SH	TINT	COL	BRT	CNT	R-B	B-B	$\gamma_1$	$\gamma_2$	PLL	PIC	BLM1	UBRT	RCNT	BCNT	P-B
0	(Setting 2, horizontal AFC adjustment)		(A) = SIG5 (VL = 0mV)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
1	Current dissipation $V_{CC1}$	ICC1	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
2	Current dissipation $V_{CC2}$	ICC2	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
3	Current dissipation $V_{DD}(L1, L2, H mode)$	IDD1	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	L1	ON	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
	Current dissipation $V_{DD}(H mode)$	IDD2	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	H	ON	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
4	L-level input voltage	VIL	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
5	H-level input voltage	VIH	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
6	H-level output voltage	VOH1	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
7	L-level output voltage	VOL1	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
8	Output transition time	tTLH	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
		tTHL	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
9	Cross point time difference	$\Delta T$	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
10	CKH duty	DTYHC	(A) = SIG4, (B) = SIG2 (0dB)	A	A	A	OFF	B	B	ON	NT	-	-	1	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
11	Contrast characteristics, TYP	GCNTTP	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
12	Contrast characteristics, MIN	GCNTMN	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
13	Video max. gain	GV	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
14	Y signal frequency	FTRPNO	(A) = SIG1	A	A	A	OFF	B	B	ON	-	H	OFF	ALL	128	128	128	128	128	0	ADJ	180	0	0	ADJ	128	128	128	128
		FTRPNT	(A) = SIG1	A	A	A	OFF	B	B	ON	NT	H	ON	ALL	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
		FTRPPL	(A) = SIG1	A	A	A	OFF	B	B	ON	PAL	H	ON	ALL	128	128	128	128	128	0	ADJ	128	0	0	ADJ	128	128	128	128
15	Picture quality variable amount 1 (TRAP OFF) L1, L2 mode	GSH1X	(A) = SIG7	A	A	A	OFF	B	B	ON	-	H	OFF	ALL	128	128	128	128	128	0	ADJ	255	0	0	ADJ	128	128	128	128
		GSH1N	(A) = SIG7	A	A	A	OFF	B	B	ON	-	H	OFF	ALL	128	128	128	128	128	0	ADJ	0	0	0	ADJ	128	128	128	128
16	Picture quality adjustment variable amount 2 (TRAP OFF), H mode	GSH2X	(A) = SIG7	A	A	A	OFF	B	B	ON	-	L1	OFF	ALL	128	128	128	128	128	0	ADJ	255	0	0	ADJ	128	128	128	128
		GSH2N	(A) = SIG7	A	A	A	OFF	B	B	ON	-	L1	OFF	ALL	128	128	128	128	128	0	ADJ	0	0	0	ADJ	128	128	128	128
17	Picture quality adjustment variable amount 3 (TRAP ON), H mode	GSH3X	(A) = SIG7	A	A	A	OFF	B	B	ON	NT	L1	ON	ALL	128	128	128	128	128	0	ADJ	255	0	0	ADJ	128	128	128	128
		GSH3N	(A) = SIG7	A	A	A	OFF	B	B	ON	NT	L1	ON	ALL	128	128	128	128	128	0	ADJ	0	0	0	ADJ	128	128	128	128
18	Picture quality adjustment variable amount 4 (TRAP ON), H mode	GSH4X	(A) = SIG7	A	A	A	OFF	B	B	ON	NT	H	ON	ALL	128	128	128	128	128	0	ADJ	255	0	0	ADJ	128	128	128	128
		GSH4N	(A) = SIG7	A	A	A	OFF	B	B	ON	NT	H	ON	ALL	128	128	128	128	128	0	ADJ	0	0	0	ADJ	128	128	128	128

Note: PLL must be reset when the panel mode is changed.



No.	Parameter	Symbol	Input signal, condition, etc.	SW set										Mode set			DAC set												
				1	2	3	48	53	54	58	System	Panel	TRAP	SH	TINT	COL	BRT	CNT	R-B	B-B	$\gamma_1$	$\gamma_2$	PLL	PIC	BLM1	UBRT	RCNT	BCNT	P-B
				A	A	A	OFF	B	ON	NT	-	-	OFF	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128
19	Y signal input/output delay rate	TDYTRN	(A) = SIG9	A	A	A	OFF	B	B	ON	NT	-	OFF	ALL	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		TDYTRP	(A) = SIG9	A	A	A	OFF	B	B	ON	-	-	ON	ALL	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
20	Color difference input color adjustment	GEXCMX	(A) = SIG5, (D) = SIG1	A	A	A	OFF	A	B	ON	-	-	ALL	128	255	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		GEXCMN	(A) = SIG5, (D) = SIG1	A	A	A	OFF	A	B	ON	-	-	ALL	128	0	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
21	Color difference balance	VEXCBL	(A) = SIG5, (D) = (E) = SIG1	A	A	A	OFF	A	A	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
22	Color difference input balance adjustment R	GEXRMM	(A) = SIG5, (D) = (E) = SIG1	A	A	A	OFF	B	A	ON	-	-	ALL	255	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		GEXRMN	(A) = SIG5, (D) = (E) = SIG1	A	A	A	OFF	B	A	ON	-	-	ALL	0	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
23	Color difference input balance adjustment B	GEXBMX	(A) = SIG5, (D) = (E) = SIG1	A	A	A	OFF	A	B	ON	-	-	ALL	255	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		GEXBMN	(A) = SIG5, (D) = (E) = SIG1	A	A	A	OFF	A	B	ON	-	-	ALL	0	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
24	G-Y matrix characteristics	VEXGBN	(A) = SIG5, (D) = SIG1	A	A	A	OFF	A	B	ON	NT	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		VEXGBP	(A) = SIG5, (D) = SIG1	A	A	A	OFF	A	B	ON	PAL	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		VEXGR	(A) = SIG5, (D) = SIG1	A	A	A	OFF	B	A	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
25	RGB/PCD output DC voltage	VOUT	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	ADJ	128	128	128	0	0	ADJ	128	0	128	128	128	ADJ	
26	RGB/PCD output DC voltage difference	$\Delta$ VOUT	(Calculation)	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	ADJ	128	128	128	0	0	ADJ	128	0	128	128	128	ADJ	
27	SIGCNT variable range	VCNT	(A) = SIG5	A	A	A	ON	B	B	ON	-	-	ALL	128	128	ADJ	128	128	128	0	0	ADJ	128	0	128	128	128	ADJ	
28	User brightness change rate	UBRTMX	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	255	128	128	0	0	ADJ	128	0	255	128	128	128	
		UBRTMN	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	255	128	128	0	0	ADJ	128	0	255	128	128	128	
29	User brightness change rate	BRTMX	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	255	255	128	128	0	0	ADJ	128	0	128	128	128	128	
		BRTMN	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	0	255	128	128	0	0	ADJ	128	0	128	128	128	128	
30	Brightness change rate	PCDMX	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	255	
		PCDMN	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	0	
31	Sub-brightness R change rate	SBBRTR	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	160	128	SET	128	0	0	ADJ	128	0	128	128	128	128	
32	Sub-brightness B change rate	SBBRTB	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	160	128	SET	128	0	0	ADJ	128	0	128	128	128	128	
33	Gain difference between RGB signals	$\Delta$ GRGB	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
34	Sub-contrast R change rate	SBCNTR	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	70	128	128	0	0	ADJ	128	0	128	128	128	128	
35	Sub-contrast B change rate	SBCNTB	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	70	128	128	0	0	ADJ	128	0	128	128	128	128	
36	RGB inverted/non-inverted gain difference	$\Delta$ GINV	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
37	Black level potential difference between RGB signals	$\Delta$ VBL	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	ALL	128	128	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	

Note: PLL must be reset when the panel mode is changed.

No.	Parameter	Symbol	Input signal, condition, etc.	SW set								Mode set				DAC set												
				1	2	3	48	53	54	58	System	Panel	TRAP	S/H	TINT	COL	BRT	CNT	R-B	B-B	$\gamma 1$	$\gamma 2$	PLL	PIC	BIM1	UBRT	RCNT	BCNT
38	Gamma gain	G <sub>Y</sub> L	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	128	128	120	210	ADJ	128	0	128	128	128	128	128
		G <sub>Y</sub> M	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	128	128	120	210	ADJ	128	0	128	128	128	128	128
		G <sub>Y</sub> H	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	128	128	120	210	ADJ	128	0	128	128	128	128	128
39	$\gamma 1$ adjustment variable range	V <sub>Y1</sub> MIN	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	60	128	0	0	ADJ	128	0	128	128	128	128	128
		V <sub>Y1</sub> MX	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	60	128	255	0	ADJ	128	0	128	128	128	128	128
40	$\gamma 2$ adjustment variable range	V <sub>Y2</sub> MIN	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	60	128	0	0	ADJ	128	0	128	128	128	128	128
		V <sub>Y2</sub> MX	(A) = SIG8	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	ADJ	60	128	0	255	ADJ	128	0	128	128	128	128	128
41	PCD transition time	IPCD	(A) = SIG4	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
42	RGB output white limiter level	VWL	(A) = SIG3	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	255	ADJ	128	0	0	128	128	128	
43	RGB output black limiter variable range	VBLIMX	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	255	ADJ	128	255	0	128	128	128	
		VBLIMN	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	255	ADJ	128	0	0	128	128	128	
44	White limiter DC voltage	VWLIM	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		VBLIM	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	0	128	128	0	0	ADJ	128	ADJ	128	128	128	
46	TRAP attenuation amount	ATRAPN	(A) = SIG2	A	A	A	OFF	B	B	ON	NT	-	-	ON	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		ATRAPP	(A) = SIG2	A	A	A	OFF	B	B	ON	PAL	-	-	ON	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
47	R-Y, B-Y LPF characteristics	DEMLPF	(A) = SIG5, (D) = (E) = SIG1	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		WSSEP	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
49	Sync separation input sensitivity	VSSEP	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		TDSYL	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
51	Horizontal pull-in range	TDSYH	(A) = SIG5	A	A	A	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		HPLLN	(A) = SIG5	A	A	A	OFF	B	B	ON	NT	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
52	External RGB input threshold voltage	HPLLP	(A) = SIG5	A	A	A	OFF	B	B	ON	PAL	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		VTEXTB	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
53	Propagation delay time between external RGB outputs	VTEXTW	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		TD1EXT	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
54	External RGB output blanking level	TD2EXT	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		EXTBK	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
55	External RGB output white level	EXTWT	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
		TEXMIN	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	
56	External RGB input minimum pulse width	TEXMIN	(A) = SIG5, (C) = SIG6	B	B	B	OFF	B	B	ON	-	-	-	ALL	128	128	128	128	0	0	ADJ	128	0	128	128	128	128	

Note: PLL must be reset when the panel mode is changed.

# LV4138W

## Input sine wave (1)

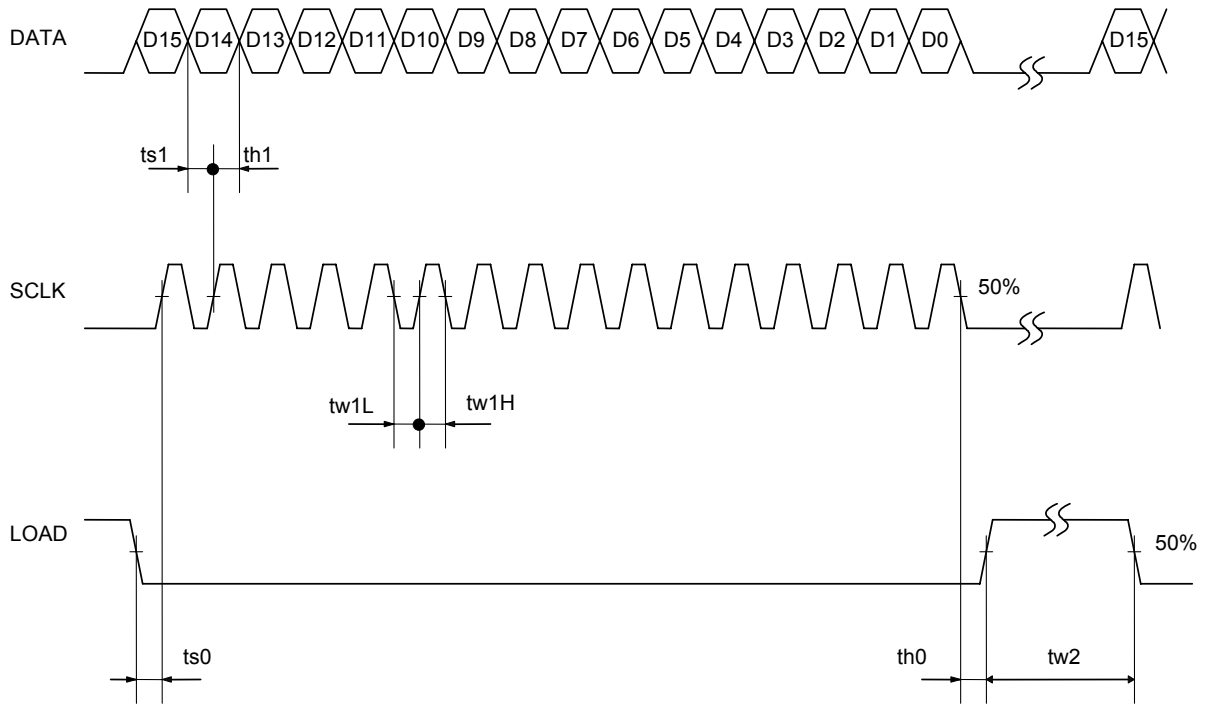
SG No.	Sine wave	
SIG1		With/ without sine wave video signal Burst/no burst (Amplitude, Frequency variable) ← Value shown in the left 0dB
SIG2		Chroma signal : burst, chroma frequency (3.579545MHz, 4.433619MHz), Chroma phase variable, burst frequency variable ← Value shown in the left 0dB
SIG3		
SIG4		5-step staircase wave
SIG5		$V_L$ amplitude variable $V_S$ variable : 143mV, unless otherwise specified. $W_S$ variable : 4.7 $\mu$ s, unless otherwise specified. $f_H$ variable : NTSC 15.734kHz PAL 15.625kHz, unless otherwise specified.

## Input sine wave (2)

SG No.	Sine wave	
SIG6		$V_L$ amplitude variable
SIG7		Frequency variable
SIG8		10-step staircase wave
SIG9		2T pulse

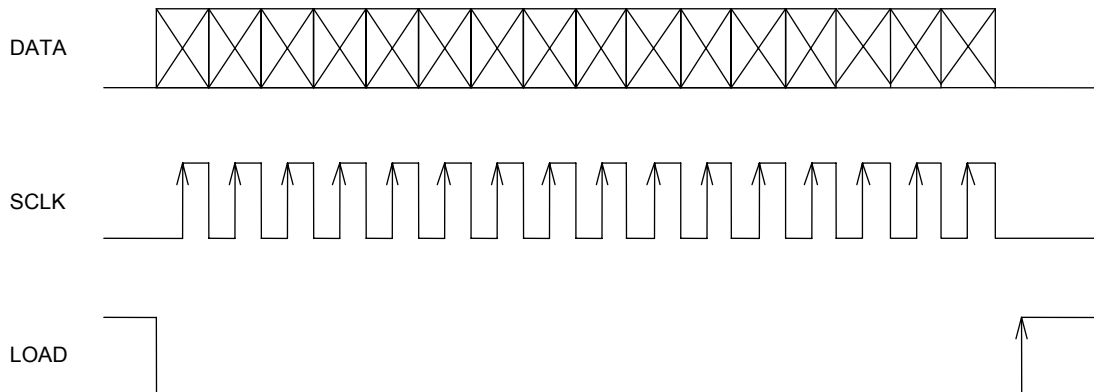
## Serial bus communication specifications

(1) Conditions for serial transfer



Parameter	Symbol	Conditions	min	typ	max	unit
<b>Serial transfer</b>						
Data setup time	$ts_0$	LOAD setup time to start SCLK.	150			ns
	$ts_1$	DATA setup time to start SCLK.	150			ns
Data holdup time	$th_0$	LOAD hold time to start SCLK	150			ns
	$th_1$	Data hold time to start SCLK.	150			ns
Pulse width	$tw_{1L}$	SCLK pulse width.	160			ns
	$tw_{1H}$	SCLK pulse width.	160			ns
	$tw_2$	LOAD pulse width.	1.0			$\mu$ s

## (2) 3-wave serial format



Data length : 16bit

Clock frequency : 3MHz or less

Only when SCLK is input in 16-bit clock while LOAD is in the L period, DATA is accepted at rise of LOAD.

Note : When SCLK is in 15-bit or 17-bit clock while LOAD is in the L period, DATA is not accepted.

## (3) Data output timing

### 1. Various mode settings

DATA accepted at rise of LOAD is set at fall of the vertical sync signal.

When the data is transmitted several times for the same item, the data immediately before the vertical sync signal becomes valid.

### 2. Setting of the electric volume

Concurrently with acceptance of DATA at rise of LOAD, the D/A output data is changed.

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## (4) Various mode settings 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Not used	○
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Not used	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TRAP ON	○
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	TRAP OFF	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Not used	○
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	Not used	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	System changeover NTSC	○
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	System changeover PAL	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	External VSYNC input OFF	○
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	External VSYNC input ON	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Y/color difference clamp position, pedestal	○
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	Y/color difference clamp position, SYNC	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Sample hold phase SHS1 (Note 1)	○
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	Sample hold phase SHS2 (Note 1)	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Sample hold phase SHS3 (Note 1)	
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	Sample hold phase ALL through (Note 1)	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	HD output polarity, positive	○
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	HD output polarity, negative	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	VD output polarity, positive	○
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	VD output polarity, negative	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	Panel selection 521×218: L1 mode (ALP202,ALP228,etc.) (ALP022,etc.)	○
0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	Panel selection 557×234: L2 mode (ALP210,ALP230,etc.)	
0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	Panel selection 881×228: H2 mode (ALP236,etc.)	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	Field overlap method, odd number on even number	○
0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	Field overlap method, even number on odd number	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	Normal mode (Note 6)	○
0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	521×218 (EVF) +557×234 (monitor) driving (Note 6-3)	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	BLHD output ON	○
0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	BLHD output Stop	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	Sync generator function, OFF	○
0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	Sync generator functionON (output other than HD, VD, BLHD, and SPCLK is turned OFF).	
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	Normal mode	○
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	Skipping OFF mode for PAL (Indication of no skipping)	
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	Not used	
0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	Not used	
0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	Not used	
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	Normal mode	○
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	Not used	
0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	For test. Do not set this bit to "1".	×
0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	For test. Do not set this bit to "1".	×

# LV4138W

## (4) Various mode settings 2

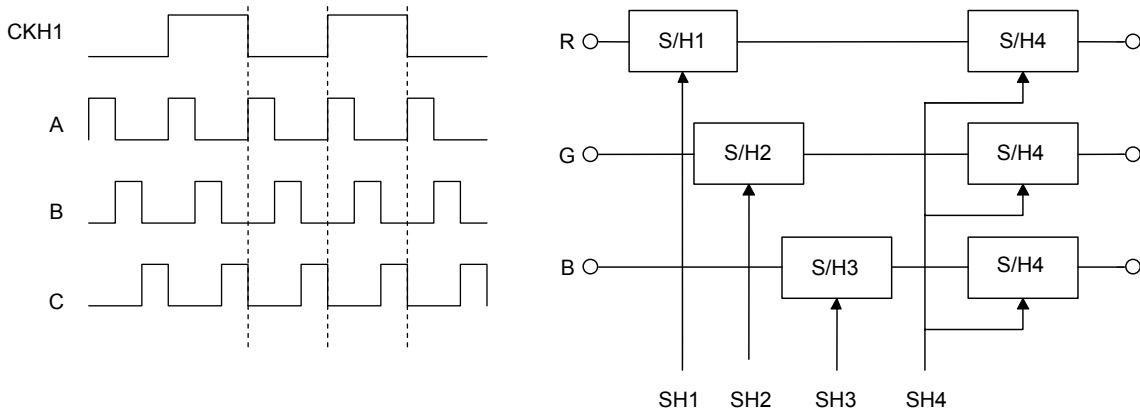
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default
0	0	0	0	0	1	0	0	x	x	x	HC5	HC4	HC3	HC2	HC1	H-position setting, 2/fh x 31 steps (Note 2)	10000
0	0	0	0	0	1	0	1	x	x	x	x	x	VP2	VP1	VP0	V-position setting, 1H x 4 steps (Note 3)	010
0	0	0	0	0	1	1	0	x	x	x	HD6	HD5	HD4	HD3	HD2	HD phase setting, 4/fh x 31 steps (Note 4)	00000
0	0	0	0	0	1	1	1	x	x	x	HW5	HW4	HW3	HW2	HW1	BLHD pulse setting, 2/fh x 31 steps (Note 5)	10000
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Monitor horizontal inversion, normal scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	Monitor horizontal inversion, reverse scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Monitor vertical inversion, normal scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	Monitor vertical inversion, reverse scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	EVF horizontal inversion, normal scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	EVF horizontal inversion, reverse scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	EVF vertical inversion, normal scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	EVF vertical inversion, reverse scan mode	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Scan changeover pin, normalSCAN pin : OPEN	○
0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	Scan changeover pin, reverse scanSCAN pin : OPEN	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Not used	○
0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	Not used	○
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	VCO sensitivity changeover 1	○
0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	VCO sensitivity changeover 2	○
0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	VCO sensitivity changeover 3	○
0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	VCO sensitivity changeover 4	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	Monitor scan stop mode (Note 6-4)	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	1	Monitor display mode	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	EVF scan stop mode (Note 6-4)	○
0	0	0	0	1	0	0	1	0	0	0	0	1	1	0	0	EVF display mode	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	blanking period CHK/STH stop OFF (NORMAL)	○
0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	blanking period CKH/STH stop ON (power save mode)	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	H blanking period CKH stop OFF (NORMAL)	○
0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	H blanking period CKH stop ON (power save mode)	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	Panel connection form MODE 1 (Note 6-1)	○
0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	Panel connection form MODE 2 (Note 6-2)	○
0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	Normal mode	○
0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	For test. Do not set this bit to "1".	x

## (4) Various mode settings 3 (DAC setting)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default
1	0	0	0	0	0	0	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	TINT adjustment	10000000
1	0	0	0	0	0	0	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	COLOR adjustment	10000000
1	0	0	0	0	0	1	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	BRIGHT adjustment	10010101
1	0	0	0	0	0	1	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	CONTRAST adjustment	10001100
1	0	0	0	0	1	0	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	R-BRIGHT adjustment	10000000
1	0	0	0	0	1	0	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	B-BRIGHT adjustment	10000000
1	0	0	0	0	1	1	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	γ-1 adjustment	01100100
1	0	0	0	0	1	1	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	γ-2 adjustment	00000000
1	0	0	0	1	0	0	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	PCD amplitude adjustment	01010000
1	0	0	0	1	0	0	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	R-CONT adjustment	10000000
1	0	0	0	1	0	1	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	B-CONT adjustment	10000000
1	0	0	0	1	0	1	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	BLKLIMIT adjustment	10101100
1	0	0	0	1	1	0	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Not used	00000000
1	0	0	0	1	1	0	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	PICTURE adjustment	10000000
1	0	0	0	1	1	1	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	USER-BRIGHT adjustment	10000000
1	0	0	0	1	1	1	1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	VCO adjustment	10000000
1	1	1	0	0	0	0	0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Test mode. Do not set this address.	

**(Note 1) Sample hold phase**

S/H pulse timing



	Horizontal inversion	Normal scan	
	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	through	through	through
SH3	A	C	B
SH4	C	B	A

	Horizontal inversion	Reverse scan	
	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	A	C	B
SH3	through	through	Through
SH4	C	B	A

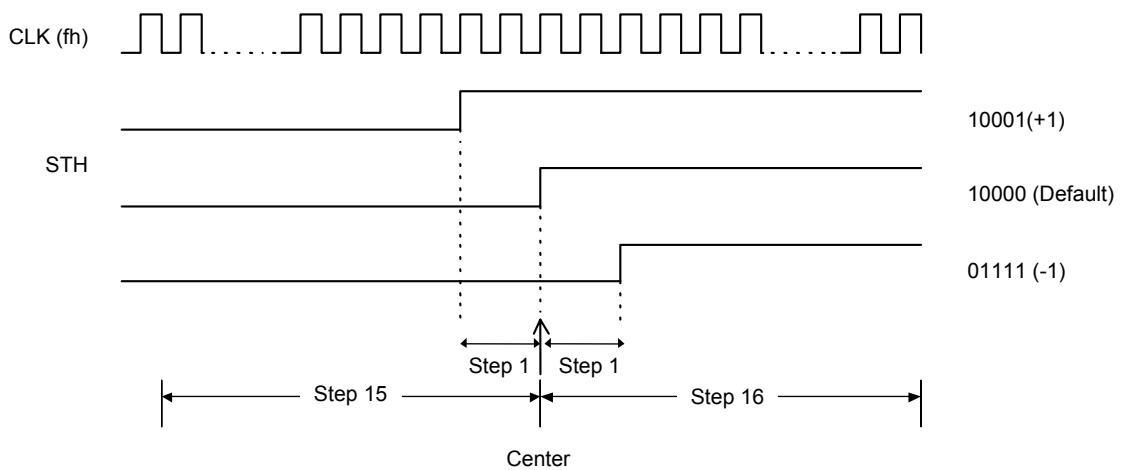
SH1 : SH pulse for R signal  
SH3 : SH pulse for B signal

SH2 : SH pulse for G signal  
SH4 : Common SH pulse for RGB signal

**(Note 2) H-Position set**

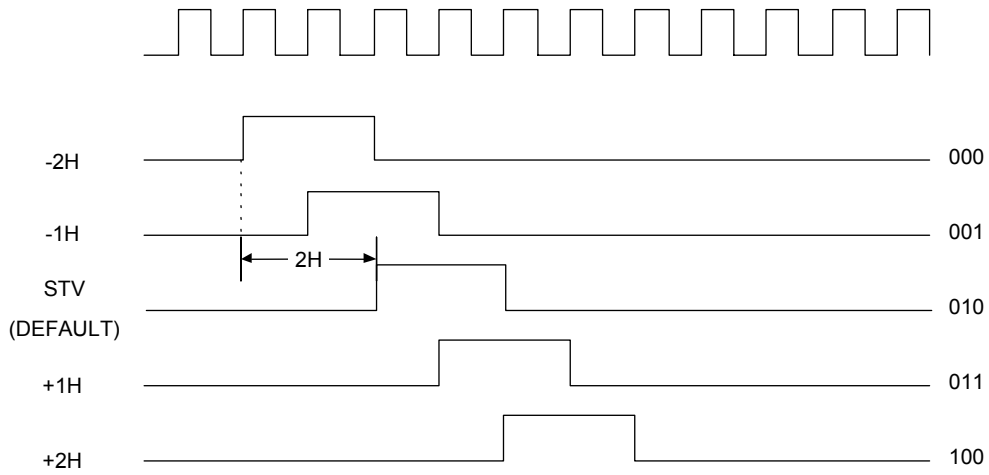
(step 1 =  $2 \times 1/f_{vco}$ ) :  $1/f_{vco} \approx 90\text{ns}$  <521×218, 557×234 mode>

:  $1/f_{vco} \approx 55\text{ns}$  <881×228 mode>



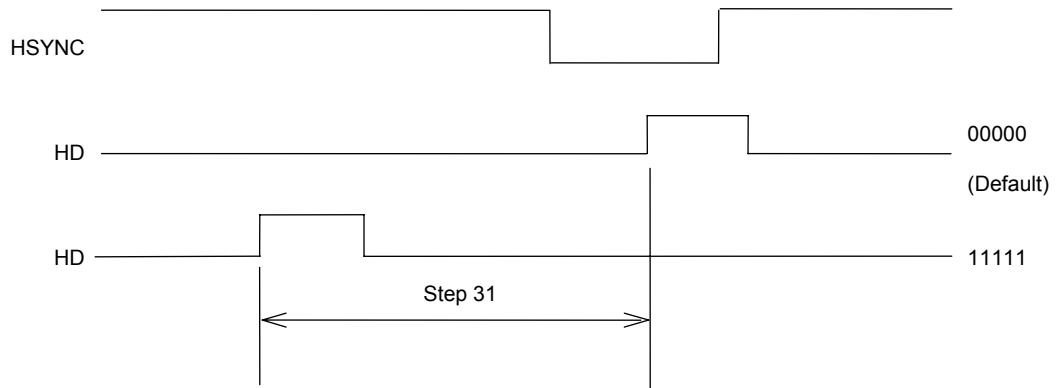


**(Note 3) V-Position set**



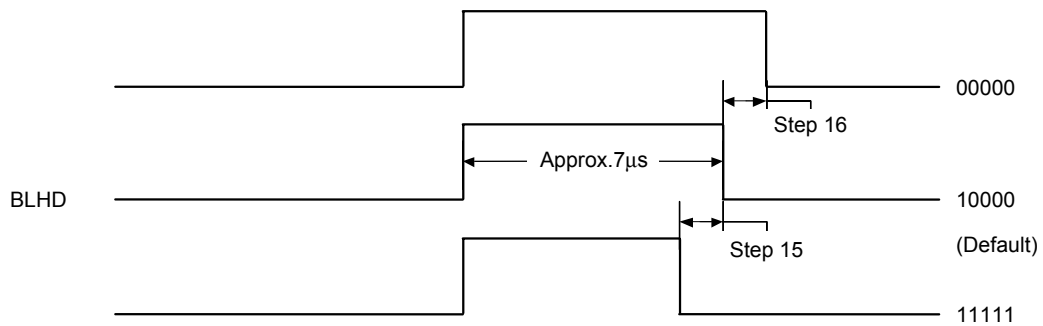
**(Note 4) HD phase set**

(step 1 =  $4 \times 1 / f_{vco}$ )



**(Note 5) BLHD phase set**

(step 1 =  $2 \times 1 / f_{vco}$ )



ON/OFF (output L fixed) possible with the serial bus

# LV4138W

## (Note 6) Output signal by mode

Pin No.	Pin symbol	MODE1 (Note 6-1)			MODE2 (Note 6-2)						Scan OFF	
		Normal			Normal			(521×218)+ (557×234) (Note 6-3)			(Note 6-4)	
		Common	For EVF	For monitor	Common	For EVF	For monitor	Common	For EVF	For monitor	Motor OFF	EVF OFF
18	STH1			○			○			○	"L"	←
17	XSTH1			○			○			○	"H"	←
22	CKH1			○			○			○	"L"	←
21	CKH2			○			○			○	"H"	←
28	STV	○			○				*	○	←	←
27	XSTV/STV2	○			○				○ (STV2)	*	←	←
30	CKV1/CKV2	○				*	○ (CKV2)		*	○ (CKV2)	←	←
29	CKV2/CKV4	○				○ (CKV4)	*		○ (CKV4)	*	←	←
34	ENB	○			○			○			←	←
33	XENB	○			○			○			←	←
24	PCG	○			○			○			←	←
23	XPCG	○			○			○			←	←
16	STH2		○			○			○		←	"L"
15	XSTH2		○			○			○		←	"H"
20	CKH3		○			○			○		←	"L"
21	CKH4		○			○			○		←	"H"

\*: Generated with an external invert

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