R&E INTERNATIONAL, INC.

4518B
4520B

CMOS DUAL UP COUNTERS

FEATURES

- Two Independent 4-Bit Counters
- Internally Synchronous for High Speed
- Dual BCD (4518B) and Dual Binary (4520B) Configurations
- Direct Reset
- Logic Edge-Clocked Design
- Trigger from either Edge of Clock Signal
- Static Operation– DC to 5MHz @ 10Vdc

DESCRIPTION

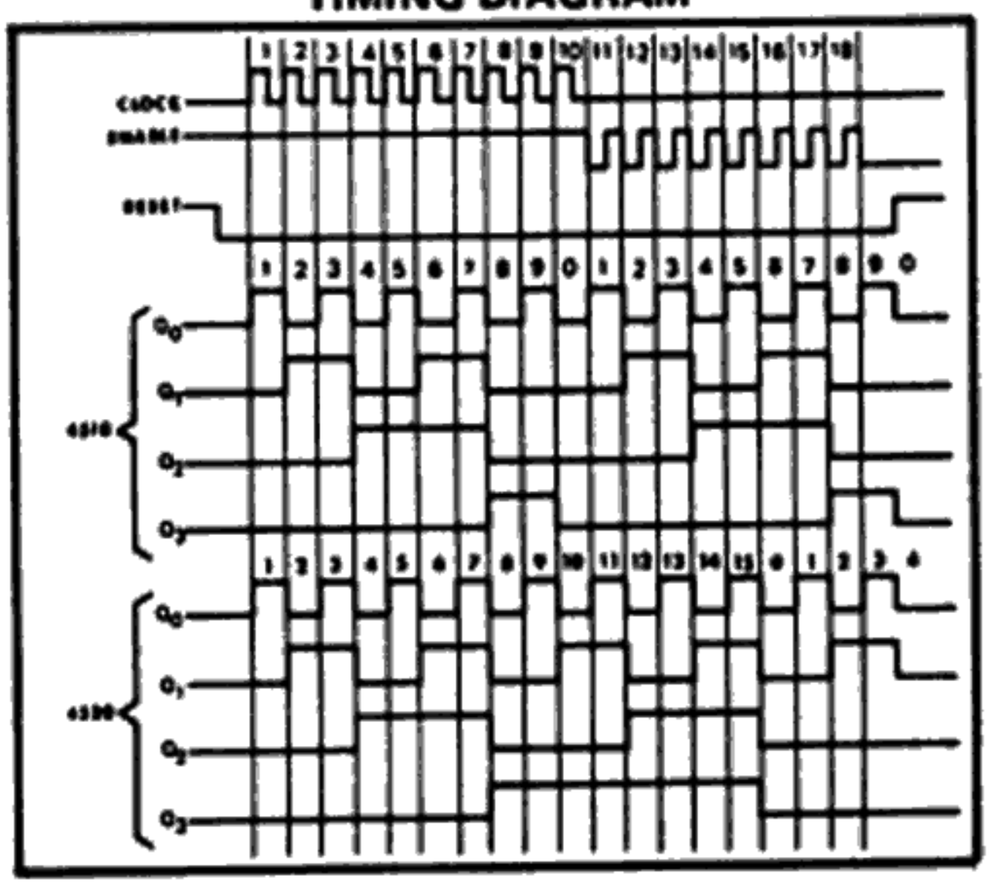
The 4518B Dual BCD Counter and the 4520B Dual Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type-D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the 4518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

TRUTH TABLE

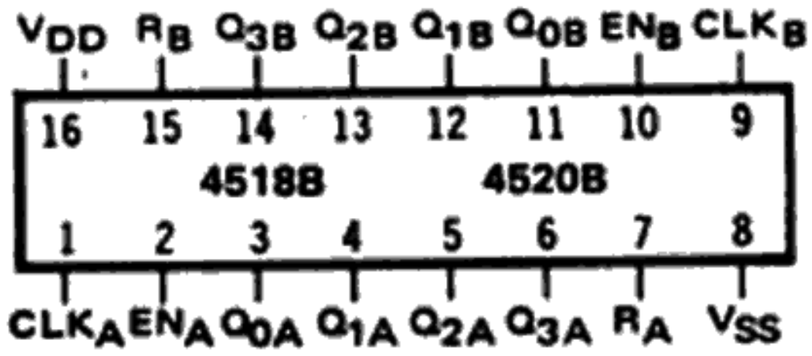
CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment Counter
0	¬	0	Increment Counter
¬	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	¬	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

TIMING DIAGRAM



CONNECTION DIAGRAM
(all packages)

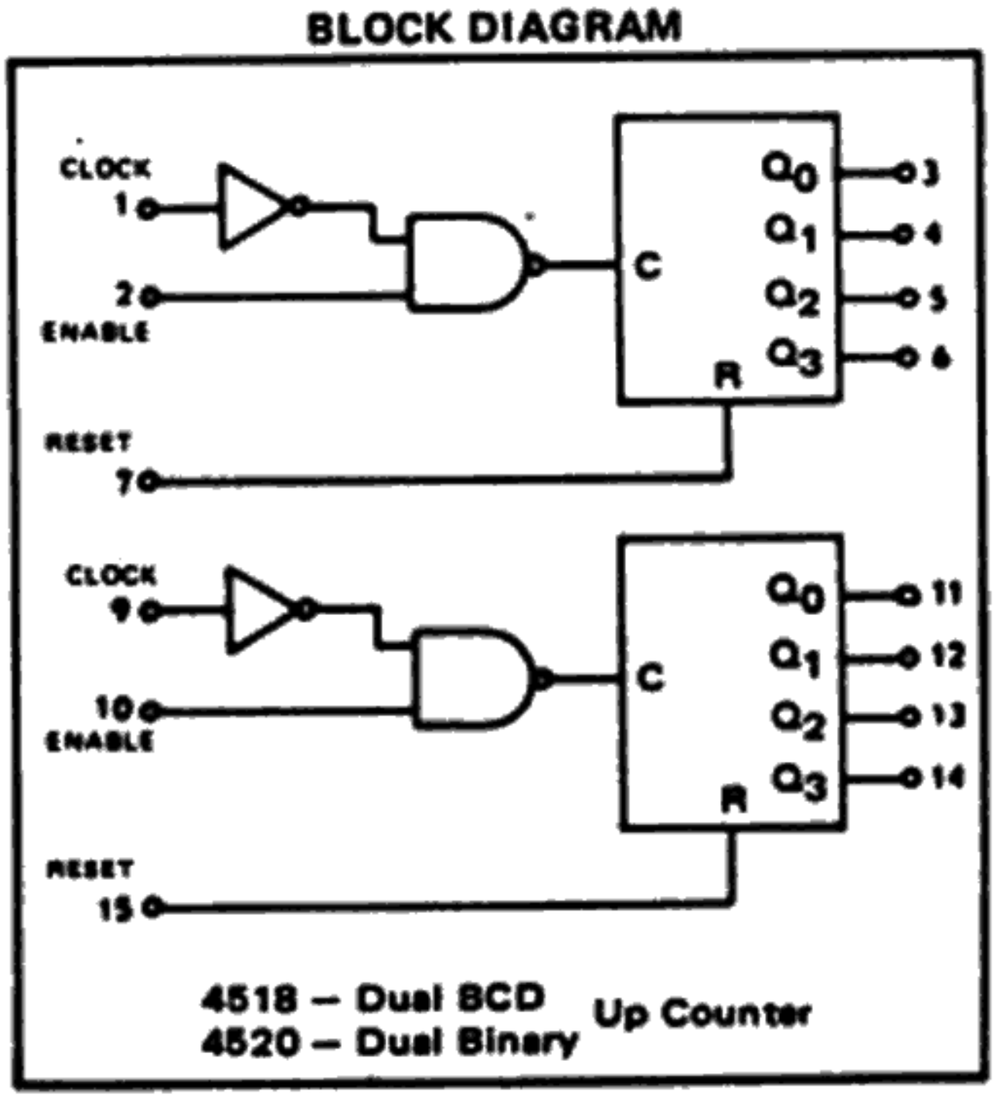


RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

BLOCK DIAGRAM



4518 – Dual BCD
4520 – Dual Binary
Up Counter

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

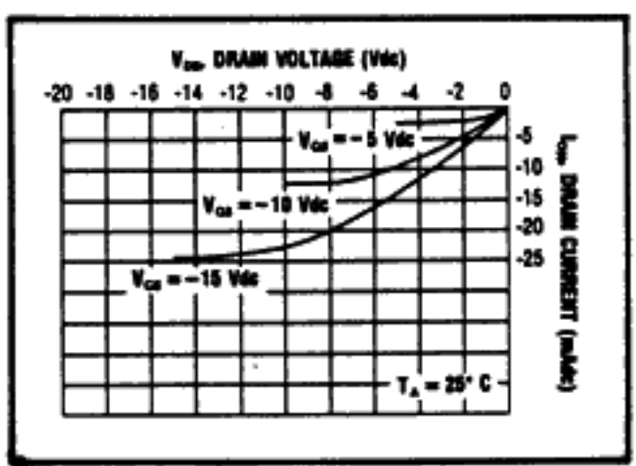
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2] Min.	T_{LOW} [2] Max.	+25°C Min.	+25°C Typ.	+25°C Max.	T_{HIGH} [2] Min.	T_{HIGH} [2] Max.	Units
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

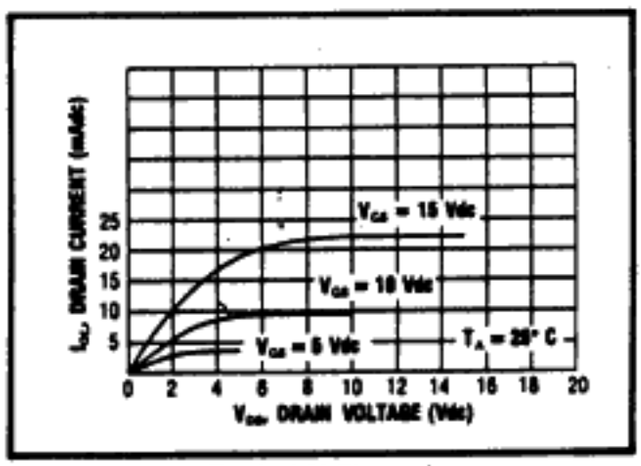
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME From Clock or Clock Enable	t_{PLH}, t_{PHL}	5	–	225	450	ns
		10	–	100	200	
		15	–	80	160	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
MINIMUM CLOCK ENABLE PULSE WIDTH	PW_{CE}	5	–	200	400	ns
		10	–	100	200	
		15	–	70	140	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.5	3.0	–	MHz
		10	3.0	6.0	–	
		15	4.0	8.0	–	
MAXIMUM CLOCK OR CLOCK ENABLE RISE & FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	5	–	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	225	450	ns
		10	–	100	200	
		15	–	80	160	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	120	240	ns
		10	–	50	100	
		15	–	40	80	
RESET REMOVAL TIME	t_{rem}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

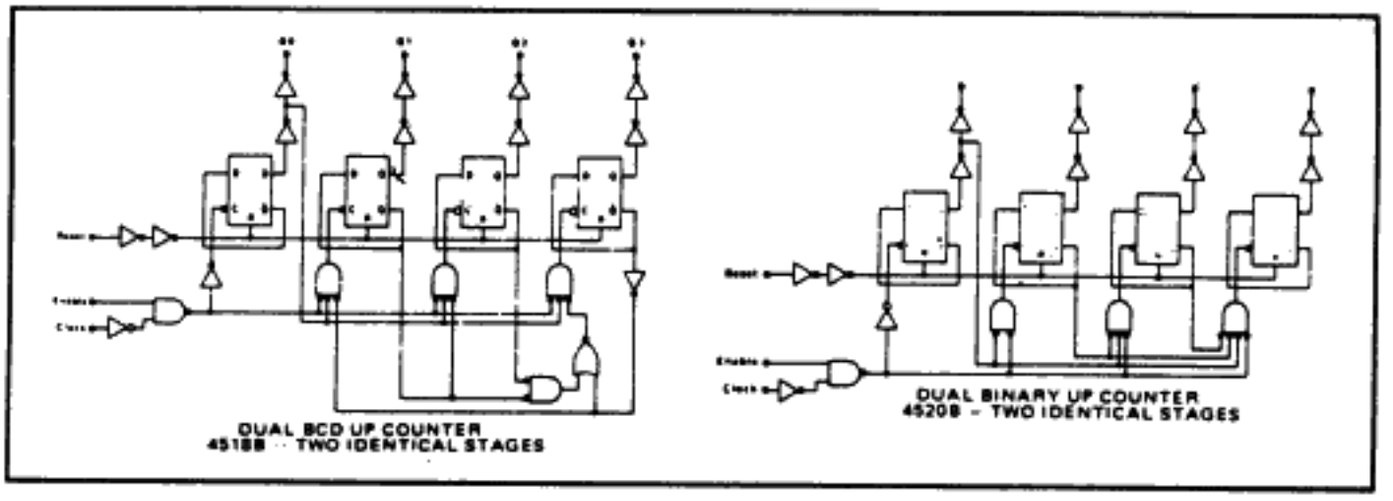


Typical P-Channel Source Current Characteristics

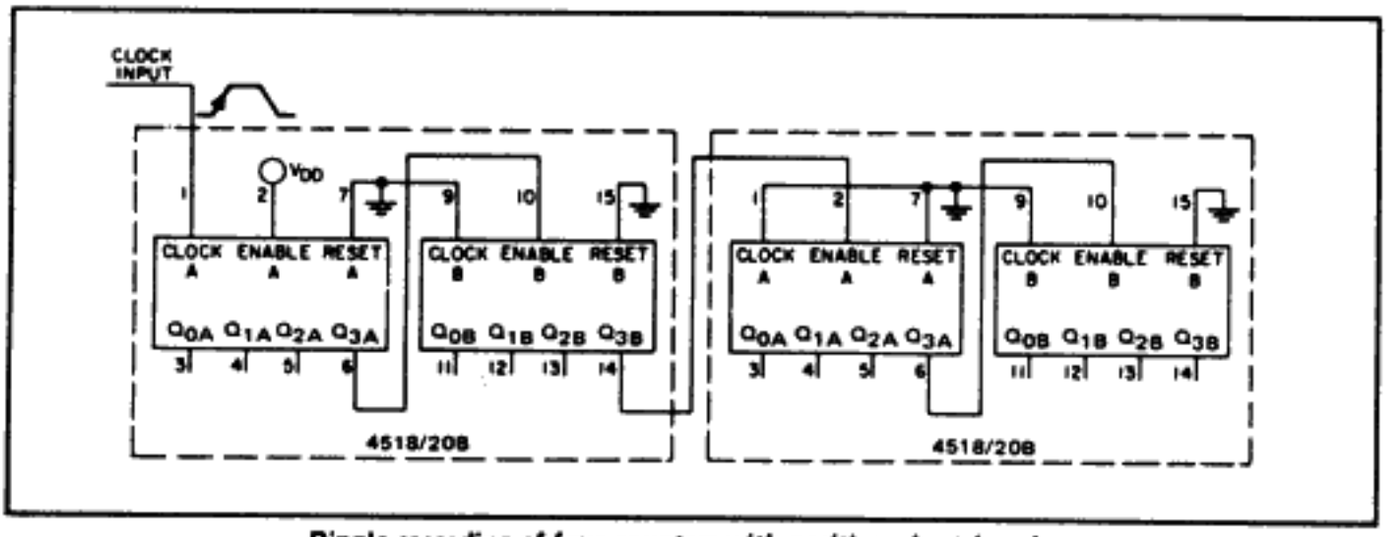


Typical N-Channel Sink Current Characteristics

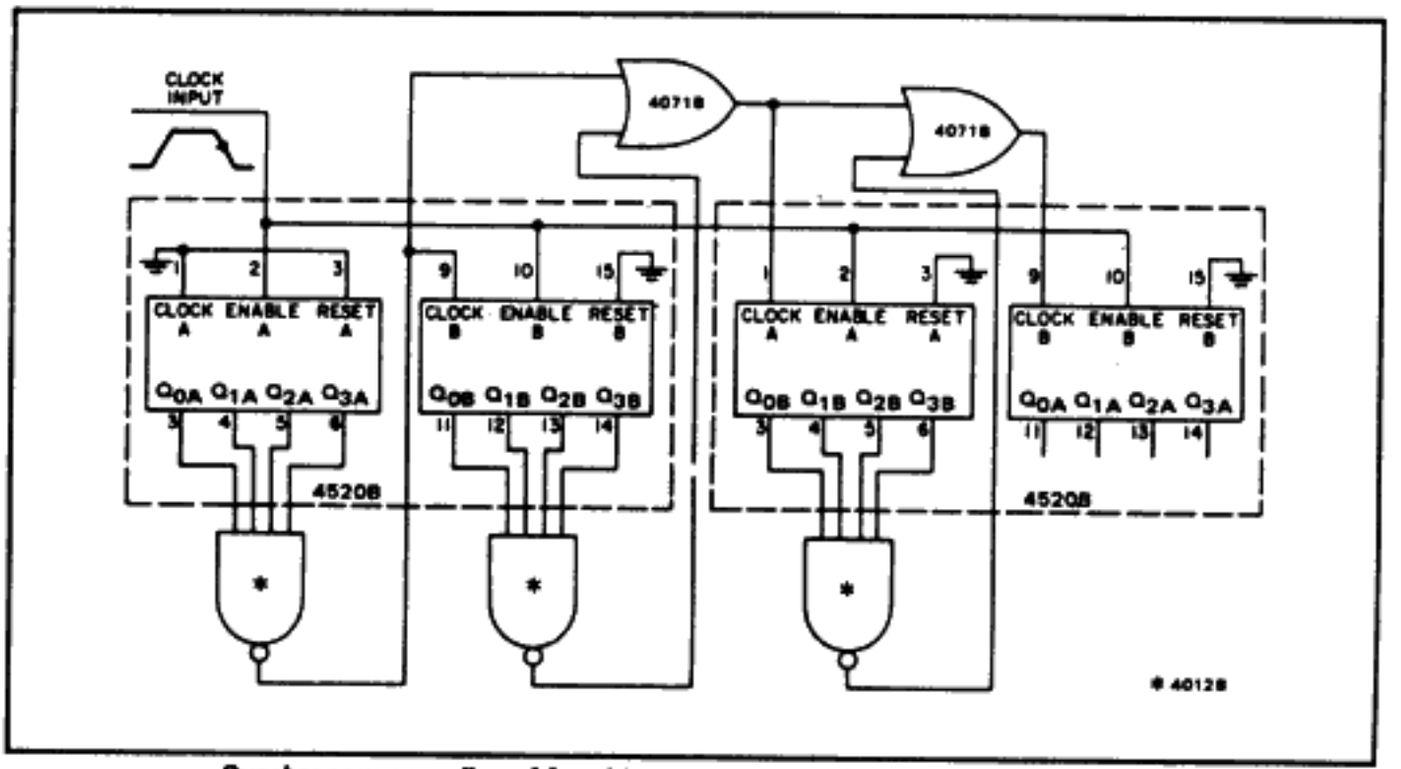
LOGIC DIAGRAMS



APPLICATIONS INFORMATION



Ripple cascading of four counters with positive-edge triggering.



Synchronous cascading of four binary counters with negative-edge triggering.