

## FLASH MEMORY

LH28F016SUHT-10

Ver. 1.0E

SHARP CORPORATION

Engineering Department 2  
Flash Memory Development Center  
Tenri Integrated Circuits (IC) Group

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

## LH28F016SUHT-10 16 Mbit (1 Mbit x 16, 2 Mbit x 8) 5V Single Voltage Flash Memory

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## LH28F016SUHT-10 16 MBIT (1 MBIT x 16, 2 MBIT x 8) 5V SINGLE VOLTAGE FLASH MEMORY

### FEATURES

- **5V Write/Erase Operation (5V  $V_{pp}$ )**
  - No Requirement for DC/DC Converter to Write/Erase
- **User-Selectable 3.3V or 5V  $V_{CC}$**
- **User-Configurable x8 or x16 Operation**
- **100 ns Maximum Access Time**
- **Min. 2.7V Read capability**
  - 180ns Maximum Access Time( $V_{CC}=2.7V$ )
- **0.32 MB/sec Write Transfer Rate**
- **10 Thousand Erase Cycles per Block**
- **56-Lead, 1.2mm x 14mm x 20mm TSOP Package (STANDARD PINOUT)**
- **Revolutionary Architecture**
  - Pipelined Command Execution
  - Write During Erase
  - Command Superset of Sharp LH28F008SA
- **15  $\mu A$  (Max.)  $I_{CC}$  in CMOS Standby**
- **8  $\mu A$  (Max.) Deep Power-Down**
- **32 Independently Lockable Blocks**
- **State-of-the-Art 0.55  $\mu m$  ETOX™ Flash Technology**
- **Not designed or rated as radiation hardened**

Sharp's LH28F016SUHT-10 16-Mbit Flash Memory is a revolutionary architecture which enables the design of truly mobile, high performance, personal computing and communication products. With innovative capabilities, 5V single voltage operation and very high read/write performance, the LH28F016SUHT-10 is also the ideal choice for designing embedded mass storage flash memory systems.

The LH28F016SUHT-10 is a very high density, highest performance non-volatile read/write solution for solid-state storage applications. Its symmetrically blocked architecture (100% compatible with the LH28F008SA 8-Mbit Flash memory, the LH28F016SA 16-Mbit Flash memory and the LH28F800SU 8-Mbit 5V single voltage Flash memory), extended cycling, low power 3.3V operation, very fast write and read performance and selective block locking provide a highly flexible memory component suitable for high density memory cards, Resident Flash Arrays and PCMCIA-ATA Flash Drives. The LH28F016SUHT-10's dual read voltage enables the design of memory cards which can interchangeably be read/written in 3.3V and 5.0V systems. Its x8/x16 architecture allows the optimization of memory to processor interface. The flexible block locking option enables bundling of executable application software in a Resident Flash Array or memory card. Manufactured on Sharp's 0.55  $\mu m$  ETOX™ process technology, the LH28F016SUHT-10 is the most cost-effective, high-density flash memory.

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\* ETOX is a trademark of Intel corporation.

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## 1.0 INTRODUCTION

The specifications intended to give an overview of the chip feature-set and of the operating AC/DC specifications. Please refer to User's Manual also, to learn detail usage.

### 1.1 Product Overview

The LH28F016SUHT-10 is a high performance 16 Mbit (16,777,216 bit) block erasable non-volatile random access memory organized as either 1 Mword x 16 or 2 Mbyte x 8. The LH28F016SUHT-10 includes thirty-two 64 KB (65,536) blocks or thirty-two 32-KW (32,768) blocks. A chip memory map is shown in Figure 3.

The implementation of a new architecture, with many enhanced features, will improve the device operating characteristics and results in greater product reliability and ease of use.

Among the significant enhancements of the LH28F016SUHT-10:

- 5V Write/Erase Operation (5V  $V_{pp}$ )
- 3.3V Low Power Capability (2.7V  $V_{cc}$  Read)
- Improved Write Performance
- Dedicated Block Write/Erase Protection

A 3/5# input pin reconfigures the device internally for optimized 3.3V or 5.0V read/write operation.

The LH28F016SUHT-10 will be available in a 56-lead, 1.2mm thick, 14mm x 20mm TSOP type I package (STANDARD PINOUT). This form factor and pinout allow for very high board layout densities.

A Command User Interface (CUI) serves as the system interface between the microprocessor or micro-controller and the internal memory operation.

Internal Algorithm Automation allows Byte/Word Writes and Block Erase operations to be executed using a Two-Write command sequence to the CUI in the same way as the LH28F008SA 8-Mbit Flash memory.

A Superset of commands have been added to the basic LH28F008SA command-set to achieve higher write performance and provide additional capabilities. These new commands and features include: -

- Page Buffer Writes to Flash
- Command Queuing Capability
- Automatic Data Writes During Erase
- Software Locking of Memory Blocks
- Two-Byte Successive Writes in 8-bit Systems
- Erase All Unlocked Blocks

Writing of memory data is performed in either byte or word increments typically within 8  $\mu$ sec, a 25% improvement over the LH28F008SA. A Block Erase operation erases one of the 32 blocks in typically 0.7 sec, independent of the other blocks, which is about 55% improvement over the LH28F008SA.

The LH28F016SUHT-10 incorporates two Page Buffers of 256 Bytes (128 Words) each to allow page data writes. This feature can improve a system write performance over previous flash memory devices.

All operations are started by a sequence of Write commands to the device. Three Status Registers (described in detail later) and a RY/BY# output pin provide information on the progress of the requested operation.

While the LH28F008SA requires an operation to complete before the next operation can be requested, the LH28F016SUHT-10 allows queuing of the next operation while the memory executes the current operation. This eliminates system overhead when writing several bytes in a row to the array or erasing several blocks at the same time. The LH28F016SUHT-10 can also perform write operations to one block of memory while performing erase of another block.

The LH28F016SUHT-10 provides user-selectable block locking to protect code or data such as Device Drivers, PCMCIA card information, ROM-Executable O/S or Application Code. Each block has an associated non-volatile lock-bit which determines the lock status of the block. In addition, the LH28F016SUHT-10 incorporates Master Write Protection Pin(WP#). When WP# turns  $V_{IL}$  after Block Lock command was issued, the device realizes Block Lock capability. When WP# is  $V_{IH}$ , any Write or Erase operation can be performed in spite of Block Lock status. When WP# is  $V_{IL}$ , please note following points.

1. When WP# is  $V_{IL}$ , any execution for Block Lock command. It is accomplished by keeping WP#  $V_{IH}$  to execute Block Lock command.
2. When WP# is  $V_{IL}$  and also if power off occurs or Reset, Abort command is issued during executing Erase operation, there is a possibility that the Block in which Erase operation is in progress turns to protected Block and succeeding Erase/Write operation in that Block can not be executed. In this case, turn WP# to  $V_{IH}$  and also execute Block Erase operation for that Block or execute Full chip Erase operation.

The LH28F016SUHT-10 contains three types of Status Registers to accomplish various functions:

- A Compatible Status Register (CSR) which is 100% compatible with the LH28F008SA Flash memory's Status Register. This register, when used alone, provides a straightforward upgrade capability to the LH28F016SUHT-10 from a LH28F008SA-based design.
- A Global Status Register (GSR) which informs the system of command Queue status, Page Buffer status, and overall Write State Machine (WSM) status.
- 32 Block Status Registers (BSRs) which provide block-specific status information such as the block lock-bit status.

The GSR and BSR memory maps for Byte-Wide and Word-Wide modes are shown in Figures 4.1 and 4.2.

The LH28F016SUHT-10 incorporates an open drain RY/BY# output pin. This feature allows the user to OR-tie many RY/BY# pins together in a multiple memory configuration such as a Resident Flash Array.

The LH28F016SUHT-10 also incorporates a dual chip-enable function with two input pins, CE<sub>0</sub># and CE<sub>1</sub>#. These pins have exactly the same functionality as the regular chip-enable pin CE# on the LH28F008SA. For minimum chip designs, CE<sub>1</sub># may be tied to ground and use CE<sub>0</sub># as the chip enable input. The LH28F016SUHT-10 uses the logical combination of these two signals to enable or disable the entire chip. Both CE<sub>0</sub># and CE<sub>1</sub># must be active low to enable the device and if either one becomes inactive, the chip will be disabled. This feature, along with the open drain RY/BY# pin, allows the system designer to reduce the number of control pins used in a large array of 8-Mbit devices.

The BYTE# pin allows either x8 or x16 read/writes to the LH28F016SUHT-10. BYTE# at logic low selects 8-bit mode with address A<sub>0</sub> selecting between low byte and high byte. On the other hand, BYTE# at logic high enables 16-bit operation with address A<sub>1</sub> becoming the lowest order address and address A<sub>0</sub> is not used (don't

care). A device diagram is shown in Figure 1.

The LH28F016SUHT-10 is specified for a maximum access time of each version, as follows:

LH28F016SUHT-10

Operating Temperature	Vcc Supply	Max. Access (t <sub>acc</sub> )
0 - 70 °C	4.5 - 5.5 V	100 ns
0 - 70 °C	3.0 - 3.6 V	150 ns
0 - 70 °C	2.7 - 3.6 V	180 ns

The LH28F016SUHT-10 incorporates an Automatic Power Saving (APS) feature which substantially reduces the active current when the device is in static mode of operation (addresses not switching).

In APS mode, the typical I<sub>cc</sub> current is 2 mA at 5.0V (1 mA at 3.3V).

A Deep Power-Down mode of operation is invoked when the RP# (called PWD# on the LH28F008SA) pin transitions low, any current operation is aborted and the device is put into the deep power-down mode. This mode brings the device power consumption to less than 5 μA, typically, and provides additional write protection by acting as a device reset pin during power transitions. When the power is turned on, RP# pin turned to low order to return the device to default configuration. When the 3/5# pin is switched, or when the power transition is occurred, or at the power on/off, RP# is required to stay low in order to protect data from noise. A recovery time of 400ns (V<sub>cc</sub>=5.0V±0.25V) is required from RP# switching high until outputs are again valid. In the Deep Power-Down state, the WSM is reset (any current operation will abort) and the CSR, GSR and BSR registers are cleared.

A CMOS Standby mode of operation is enabled when either CE<sub>0</sub># or CE<sub>1</sub># transitions high and RP# stays high with all input control pins at CMOS levels. In this mode, the device typically draws an I<sub>cc</sub> standby current of 10 μA.

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programmed "1".

- Program "0" for the bit in which you want to change data from "1" to "0".

- Program "1" for the bit which has already been programmed "0".

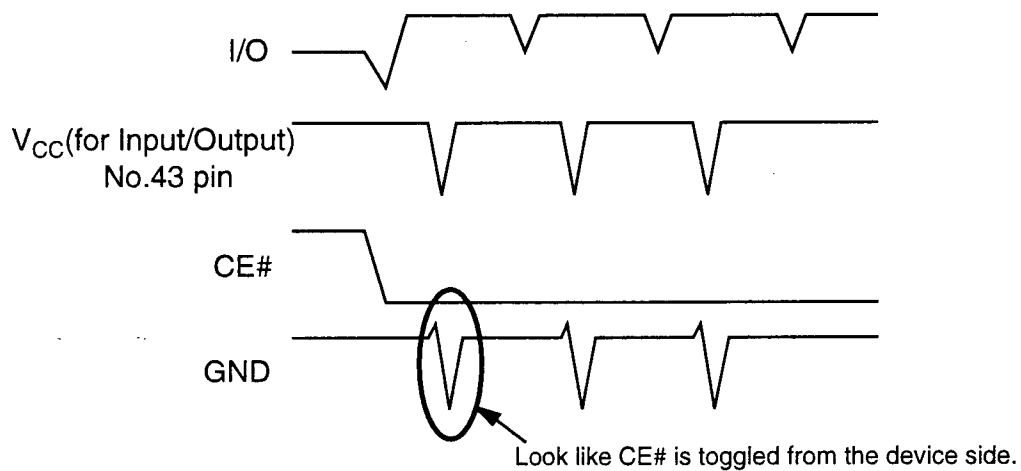
For example, changing data from "10111101" to "10111100" requires "11111110" programming.

When you use LH28F016SUHT-10, please note following points related to output buffer. When the device is in the reading mode, High-Low-High glide may occurs (It is within the access time, not operation error.) In case of the device is used for application in which the GND/ $V_{CC}$  from system is tied by high-inductance connector or flat cable such as memory

card,  $V_{CC}$  current which is generated by the glide induces voltage difference at GND/ $V_{CC}$  between system and device. The detail mechanism is showed in following chart. In these kinds application, GND/ $V_{CC}$  pin (No.42, No.43) should be connected to a single line from outside. GND/ $V_{CC}$  lines from other devices should not be mixed.

Error operation caused by glide occurs as follows.

1. Output High from I/O.
2. Glide at I/O effects GND/ $V_{CC}$  for Input/Output.
3. Device judges CE# Low signal is reversed.
4. At the result Output is reset, outputs High again.



By way of example error operation caused mechanism by glide occurs

## 2.0 DEVICE PINOUT

The LH28F016SUHT-10 56L-TSOP Type I pinout configuration is shown in Figure 2.

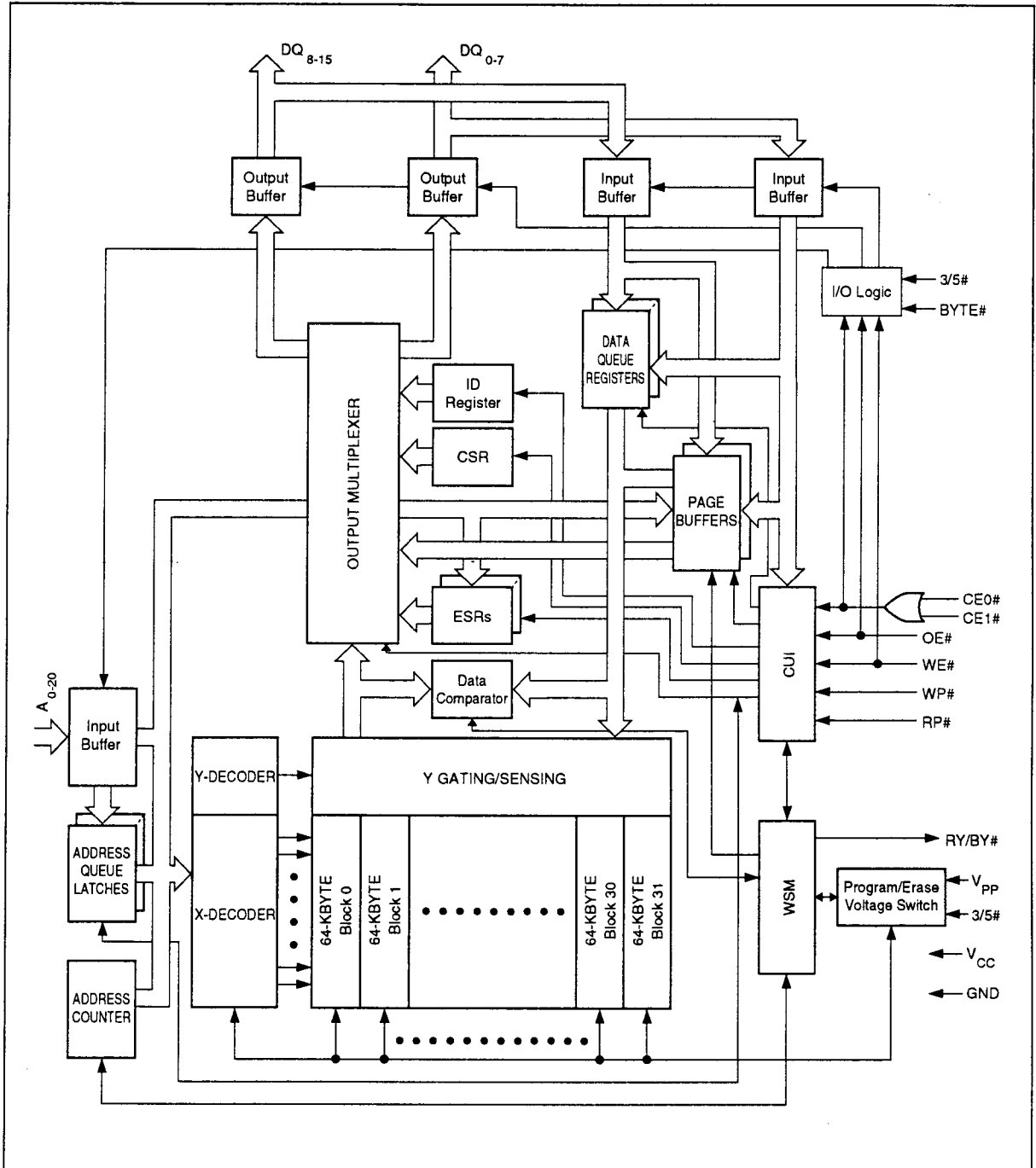


Figure 1. LH28F016SUHT-10 Block Diagram

Architectural Evolution Includes Page Buffers, Queue Registers and Extended Status Registers.



## 2.1 Lead Descriptions

Symbol	Type	Name and Function
A <sub>0</sub>	INPUT	<b>BYTE-SELECT ADDRESS:</b> Selects between high and low byte when device is in x8 mode. This address is latched in x8 Data Writes. Not used in x16 mode (i.e., the A <sub>0</sub> input buffer is turned off when BYTE# is high).
A <sub>1</sub> -A <sub>15</sub>	INPUT	<b>WORD-SELECT ADDRESSES:</b> Select a word within one 64-Kbyte block. A <sub>6-15</sub> selects 1 of 1024 rows, and A <sub>1-5</sub> selects 16 of 512 columns. These addresses are latched during Data Writes.
A <sub>16</sub> -A <sub>20</sub>	INPUT	<b>BLOCK-SELECT ADDRESSES:</b> Select 1 of 32 Erase blocks. These addresses are latched during Data Writes, Erase and Lock-Block operations.
DQ <sub>0</sub> -DQ <sub>7</sub>	INPUT/OUTPUT	<b>LOW-BYTE DATA BUS:</b> Inputs data and commands during CUI write cycles. Outputs array, buffer, identifier or status data in the appropriate Read mode. Floated when the chip is de-selected or the outputs are disabled.
DQ <sub>8</sub> -DQ <sub>15</sub>	INPUT/OUTPUT	<b>HIGH-BYTE DATA BUS:</b> Inputs data during x16 Data-Write operations. Outputs array, buffer or identifier data in the appropriate Read mode; not used for Status register reads. Floated when the chip is de-selected or the outputs are disabled.
CE <sub>0</sub> #, CE <sub>1</sub> #	INPUT	<b>CHIP ENABLE INPUTS:</b> Activate the device's control logic, input buffers, decoders and sense amplifiers. With either CE <sub>0</sub> # or CE <sub>1</sub> # high, the device is de-selected and power consumption reduces to Standby levels upon completion of any current Data-Write or Erase operations. Both CE <sub>0</sub> #, CE <sub>1</sub> # must be low to select the device. All timing specifications are the same for both signals. Device Selection occurs with the latter falling edge of CE <sub>0</sub> # or CE <sub>1</sub> #. The first rising edge of CE <sub>0</sub> # or CE <sub>1</sub> # disables the device.
RP#	INPUT	<b>RESET/POWER-DOWN:</b> With RP# low, the device is reset, any current operation is aborted and device is put into the deep power down mode. When the power is turned on, RP# pin is turned to low in order to return the device to default configuration. When the 3/5# pin is switched, or when the power transition is occurred, or at the power on/off, RP# is required to stay low in order to protect data from noise. When returning from Deep Power-Down, a recovery time of 550ns (V <sub>cc</sub> =5.0V±0.5V) is required to allow these circuits to power-up. When RP# goes low, any current or pending WSM operation(s) are terminated, and the device is reset. All Status registers return to ready (with all status flags cleared). After returning, the device is in read array mode.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Gates device data through the output buffers when low. The outputs float to tri-state off when OE# is high. <b>NOTE:</b> CE <sub>x</sub> # overrides OE#, and OE# overrides WE#.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls access to the CUI, Page Buffers, Data Queue Registers and Address Queue Latches. WE# is active low, and latches both address and data (command or array) on its rising edge.
RY/BY#	OPEN DRAIN OUTPUT	<b>READY/BUSY:</b> Indicates status of the internal WSM. When low, it indicates that the WSM is busy performing an operation. RY/BY# high indicates that the WSM is ready for new operations (or WSM has completed all pending operations), or Erase is Suspended, or the device is in deep power-down mode. This output is always active (i.e., not floated to tri-state off when OE# or CE <sub>0</sub> #, CE <sub>1</sub> # are high), except if a RY/BY# Pin Disable command is issued.

## 2.1 Lead Descriptions (Continued)

Symbol	Type	Name and Function
WP#	INPUT	WRITE PROTECT: Erase blocks can be locked by writing a non-volatile lock-bit for each block. When WP# is low, those locked blocks as reflected by the Block-Lock Status bits (BSR.6), are protected from inadvertent Data Writes or Erases. When WP# is high, all blocks can be Written or Erased regardless of the state of the lock-bits. The WP# input buffer is disabled when RP# transitions low (deep power-down mode).
BYTE#	INPUT	BYTE ENABLE: BYTE# low places device in x8 mode. All data is then input or output on DQ <sub>0-7</sub> , and DQ <sub>8-15</sub> float. Address A <sub>0</sub> selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A <sub>0</sub> input buffer. Address A <sub>1</sub> , then becomes the lowest order address.
3/5#	INPUT	3.3/5.0 VOLT SELECT: 3/5# high configures internal circuits for 3.3V operation. 3/5# low configures internal circuits for 5.0V operation. NOTES: Reading the array with 3/5# high in a 5.0V system could damage the device. There is a significant delay from 3/5# switching to valid data.
V <sub>pp</sub>	SUPPLY	ERASE/WRITE POWER SUPPLY (5.0V ± 0.5V): For erasing memory array blocks or writing words/bytes/pages into the flash array.
V <sub>cc</sub>	SUPPLY	DEVICE POWER SUPPLY (3.3V ± 0.3V, 5.0V ± 0.5V): Do not leave any power pins floating.
GND	SUPPLY	GROUND FOR ALL INTERNAL CIRCUITRY: Do not leave any ground pins floating.
NC		NO CONNECT: No internal connection to die, lead may be driven or left floating.

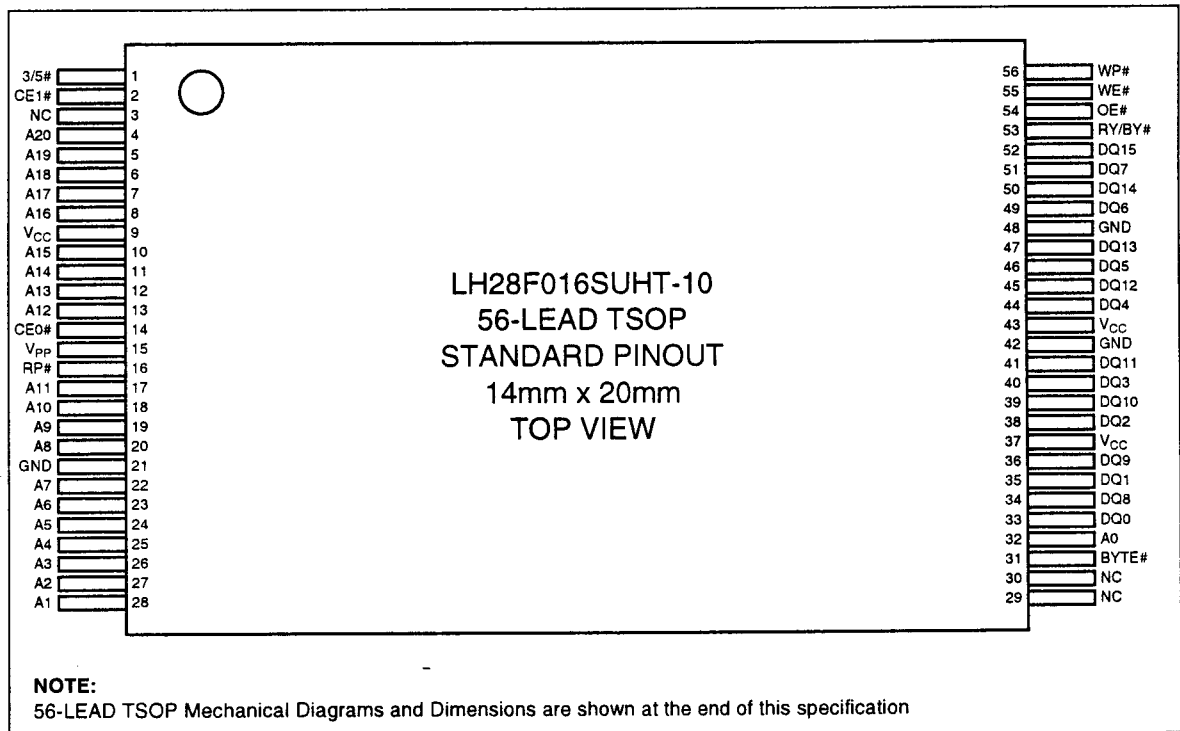


Figure 2. TSOP Configuration

## 3.0 MEMORY MAPS

1FFFFFFH	64 KByte Block	31
1F0000H		
1EFFFFFFH	64 KByte Block	30
1E0000H		
1DFFFFFFH	64 KByte Block	29
1D0000H		
1CFFFFFFH	64 KByte Block	28
1C0000H		
1BFFFFFFH	64 KByte Block	27
1B0000H		
1AFFFFFFH	64 KByte Block	26
1A0000H		
19FFFFFFH	64 KByte Block	25
190000H		
18FFFFFFH	64 KByte Block	24
180000H		
17FFFFFFH	64 KByte Block	23
170000H		
16FFFFFFH	64 KByte Block	22
160000H		
15FFFFFFH	64 KByte Block	21
150000H		
14FFFFFFH	64 KByte Block	20
140000H		
13FFFFFFH	64 KByte Block	19
130000H		
12FFFFFFH	64 KByte Block	18
120000H		
11FFFFFFH	64 KByte Block	17
110000H		
10FFFFFFH	64 KByte Block	16
100000H		
0FFFFFFH	64 KByte Block	15
0F0000H		
0EFFFFFFH	64 KByte Block	14
0E0000H		
0DFFFFFFH	64 KByte Block	13
0D0000H		
0CFFFFFFH	64 KByte Block	12
0C0000H		
0BFFFFFFH	64 KByte Block	11
0B0000H		
0AFFFFFFH	64 KByte Block	10
0A0000H		
09FFFFFFH	64 KByte Block	9
090000H		
08FFFFFFH	64 KByte Block	8
080000H		
07FFFFFFH	64 KByte Block	7
070000H		
06FFFFFFH	64 KByte Block	6
060000H		
05FFFFFFH	64 KByte Block	5
050000H		
04FFFFFFH	64 KByte Block	4
040000H		
03FFFFFFH	64 KByte Block	3
030000H		
02FFFFFFH	64 KByte Block	2
020000H		
01FFFFFFH	64 KByte Block	1
010000H		
00FFFFFFH	64 KByte Block	0
000000H		

Figure 3. LH28F016SUHT-10 Memory Map (Byte-wide mode)



## 4.0 BUS OPERATIONS, COMMANDS AND STATUS REGISTER DEFINITIONS

### 4.1 Bus Operations for Word-Wide Mode (BYTE# = V<sub>IH</sub>)

Mode	Notes	RP#	CE <sub>1</sub> #	CE <sub>0</sub> #	OE#	WE#	A <sub>1</sub>	DQ <sub>0-15</sub>	RY/BY#
Read	1,2,7	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	D <sub>OUT</sub>	X
Output Disable	1,6,7	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	High Z	X
Standby	1,6,7	V <sub>IH</sub>	V <sub>IL</sub> V <sub>IH</sub> V <sub>IH</sub>	V <sub>IH</sub> V <sub>IL</sub> V <sub>IH</sub>	X	X	X	High Z	X
Deep Power-Down	1,3	V <sub>IL</sub>	X	X	X	X	X	High Z	V <sub>OH</sub>
Manufacturer ID	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	00B0H	V <sub>OH</sub>
Device ID	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	6688H	V <sub>OH</sub>
Write	1,5,6	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	D <sub>IN</sub>	X

### 4.2 Bus Operations For Byte-Wide Mode (BYTE# = V<sub>IL</sub>)

Mode	Notes	RP#	CE <sub>1</sub> #	CE <sub>0</sub> #	OE#	WE#	A <sub>0</sub>	DQ <sub>0-7</sub>	RY/BY#
Read	1,2,7	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	D <sub>OUT</sub>	X
Output Disable	1,6,7	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	High Z	X
Standby	1,6,7	V <sub>IH</sub>	V <sub>IL</sub> V <sub>IH</sub> V <sub>IH</sub>	V <sub>IH</sub> V <sub>IL</sub> V <sub>IH</sub>	X	X	X	High Z	X
Deep Power-Down	1,3	V <sub>IL</sub>	X	X	X	X	X	High Z	V <sub>OH</sub>
Manufacturer ID	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	B0H	V <sub>OH</sub>
Device ID	4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	88H	V <sub>OH</sub>
Write	1,5,6	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	D <sub>IN</sub>	X

#### NOTES:

- X can be V<sub>IH</sub> or V<sub>IL</sub> for address or control pins except for RY/BY#, which is either V<sub>OL</sub> or V<sub>OH</sub>.
- RY/BY# output is open drain. When the WSM is ready, Erase is suspended or the device is in deep power-down mode, RY/BY# will be at V<sub>OH</sub> if it is tied to V<sub>CC</sub> through a resistor. When the RY/BY# at V<sub>OH</sub> is independent of OE# while a WSM operation is in progress.
- RP# at GND ± 0.2V ensures the lowest deep power-down current.
- A<sub>0</sub> and A<sub>1</sub> at V<sub>IL</sub> provide manufacturer ID codes in x8 and x16 modes respectively.
- A<sub>0</sub> and A<sub>1</sub> at V<sub>IH</sub> provide device ID codes in x8 and x16 modes respectively. All other addresses are set to zero.
- Commands for different Erase operations, Data Write operations of Lock-Block operations can only be successfully completed when V<sub>PP</sub> = V<sub>PPH</sub>.
- While the WSM is running, RY/BY# in Level-Mode (default) stays at V<sub>OL</sub> until all operations are complete. RY/BY# goes to V<sub>OH</sub> when the WSM is not busy or in erase suspend mode.
- RY/BY# may be at V<sub>OL</sub> while the WSM is busy performing various operations. For example, a status register read during a write operation.

### 4.3 LH28F008SA-Compatible Mode Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH	Read	AA	AD
Intelligent Identifier	1	Write	X	90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	70H	Read	X	CSRD
Clear Status Register	3	Write	X	50H			
Word/Byte Write		Write	X	40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm	4	Write	X	20H	Write	BA	D0H
Erase Suspend/Resume	4	Write	X	B0H	Write	X	D0H

**ADDRESS**

AA = Array Address  
 BA = Block Address  
 IA = Identifier Address  
 WA = Write Address  
 X = Don't Care

**DATA**

AD = Array Data  
 CSRD = CSR Data  
 ID = Identifier Data  
 WD = Write Data

**NOTES:**

- Following the intelligent identifier command, two Read operations access the manufacturer and device signature codes.
- The CSR is automatically available after device enters Data Write, Erase, or Suspend operations.
- Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits. See Status register definitions.
- While device performs Block Erase, if you issue Erase Suspend Command (B0H), be sure to confirm ESS (Erase-Suspend-Status) is set to 1 on compatible status register. In the case, ESS bit was not set to 1, also completed the Erase (ESS=0, WSMS=1), be sure to issue Resume command (D0H) after completed next Erase command. Beside, when the Erase Suspend command is issued, while the device is not in Erase, be sure to issue Resume command (D0H) after the next erase completed. When you use Erase-Suspend /Resume command, we recommend to issue serial Block Erase command (20H, D0H) and Resume command (D0H). (Refer to 4.4 Performance Enhancement Command Bus Definitions.)

## 4.4 LH28F016SUHT-10 -Performance Enhancement Command Bus Definitions

Command	Mode	Notes	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
			Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Read Extended Status Register		1	Write	X	71H	Read	RA	GSRD BSRD			
Page Buffer Swap		7	Write	X	72H						
Read Page Buffer			Write	X	75H	Read	PA	PD			
Single Load to Page Buffer			Write	X	74H	Write	PA	PD			
Sequential Load to Page Buffer	x8	4,6,10	Write	X	E0H	Write	X	BCL	Write	X	BCH
	x16	4,5,6,10	Write	X	E0H	Write	X	WCL	Write	X	WCH
Page Buffer Write to Flash	x8	3,4,9,10	Write	X	0CH	Write	A0	BC(L,H)	Write	WA	BC(H,L)
	x16	4,5,10	Write	X	0CH	Write	X	WCL	Write	WA	WCH
Two-Byte Write	x8	3	Write	X	FBH	Write	A0	WD(L,H)	Write	WA	WD(H,L)
Block Erase /Confirm		11	Write	X	20H	Write	BA	D0H	Write	X	D0H
Lock Block /Confirm			Write	X	77H	Write	BA	D0H			
Upload Status Bits /Confirm		2	Write	X	97H	Write	X	D0H			
Upload Device Information			Write	X	99H	Write	X	D0H			
Erase All Unlocked Blocks/Confirm		11	Write	X	A7H	Write	X	D0H	Write	X	D0H
RY/BY# Enable to Level-Mode		8	Write	X	96H	Write	X	01H			
RY/BY# Pulse-On-Write		8	Write	X	96H	Write	X	02H			
RY/BY# Pulse-On-Erase		8	Write	X	96H	Write	X	03H			
RY/BY# Disable		8	Write	X	96H	Write	X	04H			
Sleep			Write	X	F0H						
Abort			Write	X	80H						

### ADDRESS

BA = Block Address  
 PA = Page Buffer Address  
 RA = Extended Register Address  
 WA = Write Address  
 X = Don't Care

### DATA

AD = Array Data  
 PD = Page Buffer Data  
 BSRD = BSR Data  
 GSRD = GSR Data

WC (L.H) = Word Count (Low, High)  
 BC (L.H) = Byte Count (Low, High)  
 WD (L.H) = Write Data (Low, High)

**NOTES:**

1. RA can be the GSR address or any BSR address. See Figure 4.1 and 4.2 for Extended Status Register Memory Maps.
2. Upon device power-up, all BSR lock-bits come up locked. The Upload Status Bits command must be written to reflect the actual lock-bit status.
3.  $A_0$  is automatically complemented to load second byte of data. BYTE# must be at  $V_{LL}$ .  
 $A_0$  value determines which WD/BC is supplied first:  $A_0 = 0$  looks at the WDL/BCL,  $A_0 = 1$  looks at the WDH/BCH.
4. BCH/WCH must be at 00H for this product because of the 256-Byte (128 Word) Page Buffer size and to avoid writing the Page Buffer contents into more than one 256-Byte segment within an array block. They are simply shown for future Page Buffer expandability.
5. In x16 mode, only the lower byte  $DQ_{0,7}$  is used for WCL and WCH. The upper byte  $DQ_{8,15}$  is a don't care.
6. PA and PD (Whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle which is not shown.
7. This command allows the user to swap between available Page Buffers (0 or 1).
8. These commands reconfigure RY/BY# output to one of two pulse-modes or enable and disable the RY/BY# function.
9. Write address, WA, is the Destination address in the flash array which must match the Source address in the Page Buffer. Refer to the LH28F800SU User's Manual.
10. BCL = 00H corresponds to a Byte count of 1. Similarly, WCL = 00H corresponds to a Word count of 1.
11. Unless you issue Erase-Suspend command, it is not necessary to input DOH on third bus cycle.

**4.5 Compatible Status Register**

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

**NOTES:**

- |   |  |
|---|--|
| <p>CSR.7 = WRITE STATE MACHINE STATUS (WSMS)<br/>1 = Ready<br/>0 = Busy</p> <p>CSR.6 = ERASE-SUSPEND STATUS (ESS)<br/>1 = Erase Suspended<br/>0 = Erase in Progress/Completed</p> <p>CSR.5 = ERASE STATUS (ES)<br/>1 = Error in Block Erasure<br/>0 = Successful Block Erase</p> <p>CSR.4 = DATA-WRITE STATUS (DWS)<br/>1 = Error in Data Write<br/>0 = Data Write Successful</p> <p>CSR.3 = <math>V_{PP}</math> STATUS (VPPS)<br/>1 = <math>V_{PP}</math> Low Detect, Operation Abort<br/>0 = <math>V_{PP}</math> OK</p> | <p>RY/BY# output or WSMS bit must be checked to determine completion of an operation (Erase Suspend, Erase or Data Write) before the appropriate Status bit (ESS, ES or DWS) is checked for success.</p> <p>If DWS and ES are set to "1" during an erase attempt, an improper command sequence was entered. Clear the CSR and attempt the operation again.</p> <p>The VPPS bit, unlike an A/D converter, does not provide continuous indication of <math>V_{PP}</math> level. The WSM interrogates <math>V_{PP}</math>'s level only after the Data-Write or Erase command sequences have been entered, and informs the system if <math>V_{PP}</math> has not been switched on. VPPS is not guaranteed to report accurate feedback between <math>V_{PPL}</math> and <math>V_{PPH}</math>.</p> |
|---|--|

CSR.2-0 = RESERVED FOR FUTURE ENHANCEMENTS  
These bits are reserved for future use: mask them out when polling the CSR.



## 4.6 Global Status Register

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

NOTES:	
<p><b>GSR.7 = WRITE STATE MACHINE STATUS (WSMS)</b>                      1 = Ready                      0 = Busy</p>	<p>[1] RY/BY# output or WSMS bit must be checked to determine completion of an operation (Block Lock, Suspend, any RY/BY# reconfiguration, Upload Status Bits, Erase or Data Write) before the appropriate Status bit (OSS or DOS) is checked for success.</p>
<p><b>GSR.6 = OPERATION SUSPEND STATUS (OSS)</b>                      1 = Operation Suspended                      0 = Operation in Progress/Completed</p>	
<p><b>GSR.5 = DEVICE OPERATION STATUS (DOS)</b>                      1 = Operation Unsuccessful                      0 = Operation Successful or Currently Running</p>	
<p><b>GSR.4 = DEVICE SLEEP STATUS (DSS)</b>                      1 = Device in Sleep                      0 = Device Not in Sleep</p>	
<p><b>MATRIX 5/4</b>                      00 = Operation Successful or Currently Running                      01 = Device in Sleep Mode or Pending Sleep                      10 = Operation Unsuccessful                      11 = Operation Unsuccessful or Aborted</p>	<p>If operation currently running, then GSR.7 = 0.                      If device pending sleep, then GSR.7 = 0.                      Operation aborted: Unsuccessful due to Abort command.</p>
<p><b>GSR.3 = QUEUE STATUS (QS)</b>                      1 = Queue Full                      0 = Queue Available</p>	
<p><b>GSR.2 = PAGE BUFFER AVAILABLE STATUS (PBAS)</b>                      1 = One or Two Page Buffers Available                      0 = No Page Buffer Available</p>	<p>The device contains two Page Buffers.</p>
<p><b>GSR.1 = PAGE BUFFER STATUS (PBS)</b>                      1 = Selected Page Buffer Ready                      0 = Selected Page Buffer Busy</p>	<p>Selected Page Buffer is currently busy with WSM operation.</p>
<p><b>GSR.0 = PAGE BUFFER SELECT STATUS (PBSS)</b>                      1 = Page Buffer 1 Selected                      0 = Page Buffer 0 Selected</p>	

**NOTE:**

1. When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. GSR.7 provides indication when all queued operations are completed.

## 4.7 Block Status Register

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

**NOTES:**

BSR.7 = BLOCK STATUS (BS)  
 1 = Ready  
 0 = Busy

[1] RY/BY# output or BS bit must be checked to determine completion of an operation (Block Lock, Suspend, Erase or Data Write) before the appropriate Status bits (BOS, BLS) is checked for success.

BSR.6 = BLOCK-LOCK STATUS (BLS)  
 1 = Block Unlocked for Write/Erase  
 0 = Block Locked for Write/Erase

BSR.5 = BLOCK OPERATION STATUS (BOS)  
 1 = Operation Unsuccessful  
 0 = Operation Successful or Currently Running

BSR.4 = BLOCK OPERATION ABORT STATUS (BOAS)  
 1 = Operation Aborted  
 0 = Operation Not Aborted

The BOAS bit will not be set until BSR.7 = 1.

MATRIX 5/4  
 00 = Operation Successful or Currently Running  
 01 = Not a valid Combination  
 10 = Operation Unsuccessful  
 11 = Operation Aborted

Operation halted via Abort command.

BSR.3 = QUEUE STATUS (QS)  
 1 = Queue Full  
 0 = Queue Available

BSR.2 = V<sub>pp</sub> STATUS (VPPS)  
 1 = V<sub>pp</sub> Low Detect, Operation Abort  
 0 = V<sub>pp</sub> OK

**NOTES:**

BSR.1-0 = RESERVED FOR FUTURE ENHANCEMENTS

These bits are reserved for future use; mask them out when polling the BSRs.

- When multiple operations are queued, checking BSR.7 only provides indication of completion for that particular block. BSR.7 provides indication when all queued operations are completed.

## 5.0 ELECTRICAL SPECIFICATIONS

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### 5.1 Absolute Maximum Ratings\*

Temperature Under Bias ..... -40°C to +85°C  
 Storage Temperature ..... -65°C to +125°C

#### V<sub>CC</sub> = 3.3V ± 0.3V Systems<sup>(4)</sup>

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T <sub>A</sub>	Operating Temperature, Extended	1	-40	85	°C	Ambient Temperature
V <sub>CC</sub>	V <sub>CC</sub> with Respect to GND	2	-0.2	7.0	V	
V <sub>PP</sub>	V <sub>PP</sub> Supply Voltage with Respect to GND	2	-0.2	7.0	V	
V	Voltage on any Pin (except V <sub>CC</sub> , V <sub>PP</sub> ) with Respect to GND	2	-0.5	V <sub>CC</sub> + 0.5	V	
I	Current into any Non-Supply Pin			± 30	mA	
I <sub>OUT</sub>	Output Short Circuit Current	3		100	mA	

#### V<sub>CC</sub> = 5.0V ± 0.5V Systems<sup>(4)</sup>

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
T <sub>A</sub>	Operating Temperature, Extended	1	-40	85	°C	Ambient Temperature
V <sub>CC</sub>	V <sub>CC</sub> with Respect to GND	2	-0.2	7.0	V	
V <sub>PP</sub>	V <sub>PP</sub> Supply Voltage with Respect to GND	2	-0.2	7.0	V	
V	Voltage on any Pin (except V <sub>CC</sub> , V <sub>PP</sub> ) with Respect to GND	2	-0.5	7.0	V	
I	Current into any Non-Supply Pin			± 30	mA	
I <sub>OUT</sub>	Output Short Circuit Current	3		100	mA	

**NOTES:**

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V<sub>CC</sub> + 0.5V which, during transitions, may overshoot to V<sub>CC</sub> + 2.0V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. AC specifications are valid at both voltage ranges. See DC Characteristics tables for voltage range-specific specifications.

## 5.2 Capacitance

### For a 3.3V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C <sub>IN</sub>	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T <sub>A</sub> = 25°C, f = 1.0 MHz
C <sub>OUT</sub>	Capacitance Looking into an Output Pin	1	8	12	pF	T <sub>A</sub> = 25°C, f = 1.0 MHz
C <sub>LOAD</sub>	Load Capacitance Driven by Outputs for Timing Specifications	1		50	pF	For V <sub>CC</sub> = 3.3V ± 0.3V
	Equivalent Testing Load Circuit			2.5	ns	50Ω transmission line delay

### For a 5.0V System:

Symbol	Parameter	Note	Typ	Max	Units	Test Conditions
C <sub>IN</sub>	Capacitance Looking into an Address/Control Pin	1	6	8	pF	T <sub>A</sub> = 25°C, f = 1.0 MHz
C <sub>OUT</sub>	Capacitance Looking into an Output Pin	1	8	12	pF	T <sub>A</sub> = 25°C, f = 1.0 MHz
C <sub>LOAD</sub>	Load Capacitance Driven by Outputs for Timing Specifications	1		100	pF	For V <sub>CC</sub> = 5.0V ± 0.5V
	Equivalent Testing Load Circuit			2.5	ns	25Ω transmission line delay

#### NOTE:

1. Sampled, not 100% tested.

### 5.3 Timing Nomenclature

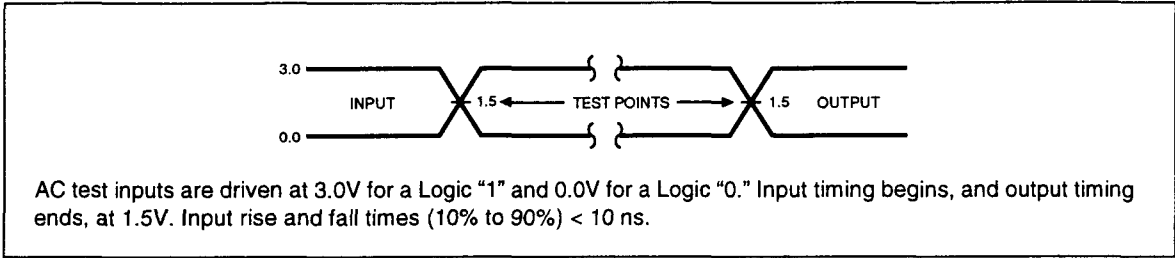
All 3.3V system timings are measured from where signals cross 1.5V.

For 5.0V systems use the standard JEDEC cross point definitions.

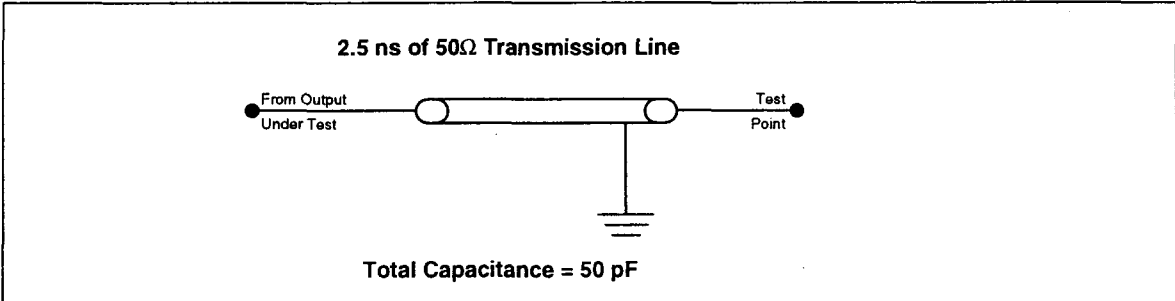
Each timing parameter consists of 5 characters. Some common examples are defined below:

- $t_{CE}$   $t_{ELOV}$  time(t) from CE# (E) going low (L) to the outputs (Q) becoming valid (V)
- $t_{OE}$   $t_{GLOV}$  time(t) from OE# (G) going low (L) to the outputs (Q) becoming valid (V)
- $t_{ACC}$   $t_{AVQV}$  time(t) from address (A) valid (V) to the outputs (Q) becoming valid (V)
- $t_{AS}$   $t_{AVWH}$  time(t) from address (A) valid (V) to WE# (W) going high (H)
- $t_{DH}$   $t_{WHDx}$  time(t) from WE# (W) going high (H) to when the data (D) can become undefined (X)

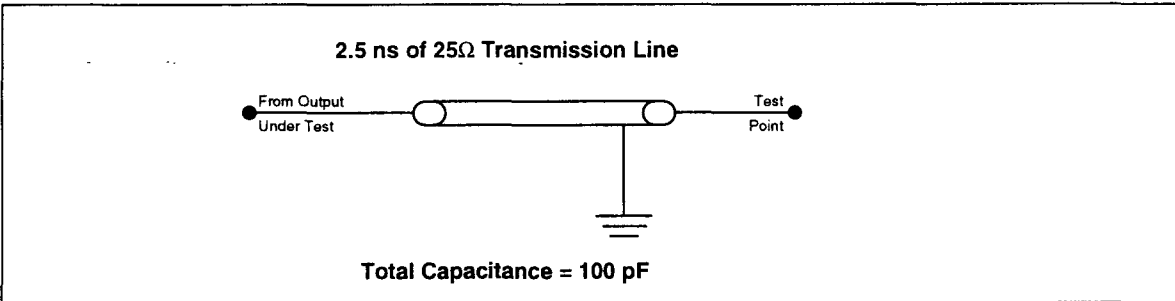
	Pin Characters		Pin States
A	Address Inputs	H	High
D	Data Inputs	L	Low
Q	Data Outputs	V	Valid
E	CE# (Chip Enable)	X	Driven, but not necessarily valid
G	OE# (Output Enable)	Z	High Impedance
W	WE# (Write Enable)		
P	RP# (Deep Power-Down Pin)		
R	RY/BY# (Ready/Busy#)		
V	Any Voltage Level		
Y	3/5# Pin		
5V	V <sub>CC</sub> at 4.5V Minimum		
3V	V <sub>CC</sub> at 3.0V Minimum		



**Figure 5. Transient Input/Output Reference Waveform**



**Figure 6. Transient Equivalent Testing Load Circuit ( $V_{CC} = 3.3V$ )**



**Figure 7. Transient Equivalent Testing Load Circuit ( $V_{CC} = 5.0V$ )**

## 5.4 DC Characteristics

$V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$

3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
$I_{IL}$	Input Load Current	1			$\pm 1$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ , $V_{IN} = V_{CC}$ or GND
$I_{LO}$	Output Leakage Current	1			$\pm 10$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ , $V_{IN} = V_{CC}$ or GND
$I_{CCS}$	$V_{CC}$ Standby Current	1,4		4	12	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ , CE <sub>0</sub> #, CE <sub>1</sub> #, RP# = $V_{CC} \pm 0.2V$ BYTE#, WP#, 3/5# = $V_{CC} \pm 0.2V$ or GND $\pm 0.2V$
				1	4	mA	$V_{CC} = V_{CC} \text{ Max}$ , CE <sub>0</sub> #, CE <sub>1</sub> #, RP# = $V_{IH}$ BYTE#, WP#, 3/5# = $V_{IH}$ or $V_{IL}$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	1		1	8	$\mu A$	RP# = GND $\pm 0.2V$
$I_{CCR1}$	$V_{CC}$ Read Current	1,3,4		30	35	mA	$V_{CC} = V_{CC} \text{ Max}$ , CMOS: CE <sub>0</sub> #, CE <sub>1</sub> # = GND $\pm 0.2V$ BYTE# = GND $\pm 0.2V$ or $V_{CC} \pm 0.2V$ Inputs = GND $\pm 0.2V$ or $V_{CC} \pm 0.2V$ , TTL: CE <sub>0</sub> #, CE <sub>1</sub> # = $V_{IL}$ , BYTE# = $V_{IL}$ or $V_{IH}$ Inputs = $V_{IL}$ or $V_{IH}$ , f = 8 MHz, $I_{OUT} = 0 \text{ mA}$
$I_{CCR2}$	$V_{CC}$ Read Current	1,3,4		15	20	mA	$V_{CC} = V_{CC} \text{ Max}$ , CMOS: CE <sub>0</sub> #, CE <sub>1</sub> # = GND $\pm 0.2V$ , BYTE# = $V_{CC} \pm 0.2V$ or GND $\pm 0.2V$ Inputs = GND $\pm 0.2V$ or $V_{CC} \pm 0.2V$ , TTL: CE <sub>0</sub> #, CE <sub>1</sub> # = $V_{IL}$ BYTE# = $V_{IH}$ or $V_{IL}$ Inputs = $V_{IL}$ or $V_{IH}$ , f = 4 MHz, $I_{OUT} = 0 \text{ mA}$
$I_{CCW}$	$V_{CC}$ Write Current	1		8	12	mA	Word/Byte Write in Progress
$I_{CCE}$	$V_{CC}$ Block Erase Current	1		6	12	mA	Block Erase in Progress
$I_{CCES}$	$V_{CC}$ Erase Suspend Current	1,2		3	6	mA	CE <sub>0</sub> #, CE <sub>1</sub> # = $V_{IH}$ Block Erase Suspended
$I_{PPS}$	$V_{PP}$ Standby Current	1		$\pm 1$	$\pm 10$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PPD}$	$V_{PP}$ Deep Power-Down Current	1		0.2	8	$\mu A$	RP# = GND $\pm 0.2V$

## DC Characteristics (Continued)

$V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

3/5# = Pin Set High for 3.3V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I <sub>PPR</sub>	V <sub>PP</sub> Read Current	1			200	μA	V <sub>PP</sub> > V <sub>CC</sub>
I <sub>PPW</sub>	V <sub>PP</sub> Write Current	1		40	60	mA	V <sub>PP</sub> = V <sub>PPH</sub> , Word/Byte Write in Progress
I <sub>PPE</sub>	V <sub>PP</sub> Erase Current	1		20	40	mA	V <sub>PP</sub> = V <sub>PPH</sub> , Block Erase in Progress
I <sub>PPES</sub>	V <sub>PP</sub> Erase Suspend Current	1			200	μA	V <sub>PP</sub> = V <sub>PPH</sub> , Block Erase Suspended
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V	
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> + 0.3	V	
V <sub>OL</sub>	Output Low Voltage				0.4	V	V <sub>CC</sub> = V <sub>CC</sub> Min and I <sub>OL</sub> = 4 mA
V <sub>OH1</sub>	Output High Voltage		2.4			V	I <sub>OH</sub> = -2.0 mA V <sub>CC</sub> = V <sub>CC</sub> Min
V <sub>OH2</sub>			V <sub>CC</sub> - 0.2			V	I <sub>OH</sub> = -100 μA V <sub>CC</sub> = V <sub>CC</sub> Min
V <sub>PPL</sub>	V <sub>PP</sub> during Normal Operations		0.0		5.5	V	
V <sub>PPH</sub>	V <sub>PP</sub> during Write/ Erase Operations	5	0		GND+0.2	V	
			V <sub>CC</sub> -0.2		5.5	V	
V <sub>LKO</sub>	V <sub>CC</sub> Erase/Write Lock Voltage		2.0			V	

### NOTES:

- All currents are in RMS unless otherwise noted. Typical values at  $V_{CC} = 3.3V$ ,  $V_{PP} = 5.0V$ ,  $T = 25^{\circ}C$ . These currents are valid for all product versions (package and speeds).
- I<sub>CCES</sub> is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I<sub>CCES</sub> and I<sub>CCR</sub>.
- Automatic Power Saving (APS) reduces I<sub>CCR</sub> to less than 1 mA in static operation.
- CMOS Inputs are either  $V_{CC} \pm 0.2V$  or  $GND \pm 0.2V$ . TTL Inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
- V<sub>PPL</sub> in read is  $V_{CC} - 0.2V < V_{PPL} < 5.5V$  or  $GND < V_{PPL} < GND + 0.2V$ .



### 5.5 DC Characteristics

$V_{CC} = 5.0V \pm 0.5V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$

3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
$I_{IL}$	Input Load Current	1			$\pm 1$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ , $V_{IN} = V_{CC}$ or GND
$I_{LO}$	Output Leakage Current	1			$\pm 10$	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ , $V_{IN} = V_{CC}$ or GND
$I_{CCS}$	$V_{CC}$ Standby Current	1,4		5	15	$\mu A$	$V_{CC} = V_{CC} \text{ Max}$ , CE <sub>0</sub> #, CE <sub>1</sub> #, RP# = $V_{CC} \pm 0.2V$ BYTE#, WP#, 3/5# = $V_{CC} \pm 0.2V$ or GND $\pm 0.2V$
				2	4	mA	$V_{CC} = V_{CC} \text{ Max}$ , CE <sub>0</sub> #, CE <sub>1</sub> #, RP# = $V_{IH}$ BYTE#, WP#, 3/5# = $V_{IH}$ or $V_{IL}$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	1		1	8	$\mu A$	RP# = GND $\pm 0.2V$
$I_{CCR1}$	$V_{CC}$ Read Current	1,3,4		50	60	mA	$V_{CC} = V_{CC} \text{ Max}$ , CMOS: CE <sub>0</sub> #, CE <sub>1</sub> # = GND $\pm 0.2V$ BYTE# = GND $\pm 0.2V$ or $V_{CC} \pm 0.2V$ Inputs = GND $\pm 0.2V$ or $V_{CC} \pm 0.2V$ , TTL: CE <sub>0</sub> #, CE <sub>1</sub> # = $V_{IL}$ , BYTE# = $V_{IL}$ or $V_{IH}$ Inputs = $V_{IL}$ or $V_{IH}$ , $f = 10 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$
$I_{CCR2}$	$V_{CC}$ Read Current	1,3,4		30	35	mA	$V_{CC} = V_{CC} \text{ Max}$ , CMOS: CE <sub>0</sub> #, CE <sub>1</sub> # = GND $\pm 0.2V$ , BYTE# = $V_{CC} \pm 0.2V$ or GND $\pm 0.2V$ Inputs = GND $\pm 0.2V$ or $V_{CC} \pm 0.2V$ , TTL: CE <sub>0</sub> #, CE <sub>1</sub> # = $V_{IL}$ BYTE# = $V_{IH}$ or $V_{IL}$ Inputs = $V_{IL}$ or $V_{IH}$ , $f = 5 \text{ MHz}$ , $I_{OUT} = 0 \text{ mA}$
$I_{CCW}$	$V_{CC}$ Write Current	1		25	35	mA	Word/Byte Write in Progress
$I_{CCE}$	$V_{CC}$ Block Erase Current	1		18	25	mA	Block Erase in Progress
$I_{CCES}$	$V_{CC}$ Erase Suspend Current	1,2		5	10	mA	CE <sub>0</sub> #, CE <sub>1</sub> # = $V_{IH}$ Block Erase Suspended
$I_{PPS}$	$V_{PP}$ Standby Current	1			$\pm 10$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PPD}$	$V_{PP}$ Deep Power-Down Current	1		0.2	8	$\mu A$	RP# = GND $\pm 0.2V$

## DC Characteristics (Continued)

$V_{CC} = 5.0V \pm 0.5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

3/5# Pin Set Low for 5V Operations

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
I <sub>PPR</sub>	V <sub>PP</sub> Read Current	1		65	200	μA	V <sub>PP</sub> > V <sub>CC</sub>
I <sub>PPW</sub>	V <sub>PP</sub> Write Current	1		40	60	mA	V <sub>PP</sub> = V <sub>PPH</sub> , Word/Byte Write in Progress
I <sub>PPE</sub>	V <sub>PP</sub> Erase Current	1		20	40	mA	V <sub>PP</sub> = V <sub>PPH</sub> , Block Erase in Progress
I <sub>PPES</sub>	V <sub>PP</sub> Erase Suspend Current	1		65	200	μA	V <sub>PP</sub> = V <sub>PPH</sub> , Block Erase Suspended
V <sub>IL</sub>	Input Low Voltage		-0.5		0.8	V	
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage				0.45	V	V <sub>CC</sub> = V <sub>CC</sub> Min and I <sub>OL</sub> = 5.8 mA
V <sub>OH1</sub>	Output High Voltage		0.85 V <sub>CC</sub>			V	I <sub>OH</sub> = -2.5 mA V <sub>CC</sub> = V <sub>CC</sub> Min
V <sub>OH2</sub>			V <sub>CC</sub> - 0.4			V	I <sub>OH</sub> = -100 μA V <sub>CC</sub> = V <sub>CC</sub> Min
V <sub>PPL</sub>	V <sub>PP</sub> during Normal Operations		0.0		5.5	V	
V <sub>PPH</sub>	V <sub>PP</sub> during Write/ Erase Operations	5	0		GND+0.2	V	
			V <sub>CC</sub> -0.2		5.5	V	
V <sub>LKO</sub>	V <sub>CC</sub> Erase/Write Lock Voltage		2.0			V	

### NOTES:

- All currents are in RMS unless otherwise noted. Typical values at  $V_{CC} = 5.0V$ ,  $V_{PP} = 5.0V$ ,  $T = 25^{\circ}C$ . These currents are valid for all product versions (package and speeds).
- I<sub>CCES</sub> is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of I<sub>CCES</sub> and I<sub>CCR</sub>.
- Automatic Power Saving (APS) reduces I<sub>CCR</sub> to less than 2 mA in Static operation.
- CMOS Inputs are either  $V_{CC} \pm 0.2V$  or  $GND \pm 0.2V$ . TTL Inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
- V<sub>PPL</sub> in read is  $V_{CC} - 0.2V < V_{PPL} < 5.5V$  or  $GND < V_{PPL} < GND + 0.2V$ .

5.6 AC Characteristics - Read Only Operations<sup>(1)</sup> $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ 

Symbol	Parameter	Notes	Vcc=3.3V±0.3V		Vcc=2.7V-3.0V		Units
			Min	Max	Min	Max	
tAVAV	Read Cycle Time		150		180		ns
tAVEL	Address Setup to CE# Going Low	3,4	10		10		ns
tAVGL	Address Setup to OE# Going Low	3,4	0		0		ns
tAVQV	Address to Output Delay			150		180	ns
tELQV	CE# to Output Delay	2		150		180	ns
tPHQV	RP# High to Output Delay			750		800	ns
tGLQV	OE# to Output Delay	2		50		55	ns
tELQX	CE# to Output in Low Z	3	0		0		ns
tEHQZ	CE# to Output in High Z	3		55		60	ns
tGLQX	OE# to Output in Low Z	3	0		0		ns
tGHQZ	OE# to Output in High Z	3		40		45	ns
tOH	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		0		ns
tFLQV tFHQV	BYTE# to Output Delay	3		150		180	ns
tFLQZ	BYTE# Low to Output in High Z	3		40		45	ns
tELFL tELFH	CE# Low to BYTE# High or Low	3		5		5	ns

AC Characteristics - Read Only Operations<sup>(1)</sup> (Continued) $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ 

Symbol	Parameter	Notes	Vcc=5.0V±0.5V		Units
			Min	Max	
t <sub>AVAV</sub>	Read Cycle Time		100		ns
t <sub>AVEL</sub>	Address Setup to CE# Going Low	3,4	10		ns
t <sub>AVGL</sub>	Address Setup to OE# Going Low	3,4	0		ns
t <sub>AVQV</sub>	Address to Output Delay			100	ns
t <sub>ELQV</sub>	CE# to Output Delay	2		100	ns
t <sub>PHQV</sub>	RP# High to Output Delay			550	ns
t <sub>GLQV</sub>	OE# to Output Delay	2		40	ns
t <sub>ELQX</sub>	CE# to Output in Low Z	3	0		ns
t <sub>EHQZ</sub>	CE# to Output in High Z	3		35	ns
t <sub>GLQX</sub>	OE# to Output in Low Z	3	0		ns
t <sub>GHQZ</sub>	OE# to Output in High Z	3		35	ns
t <sub>OH</sub>	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t <sub>FLQV</sub> t <sub>FHQV</sub>	BYTE# to Output Delay	3		100	ns
t <sub>FLQZ</sub>	BYTE# Low to Output in High Z	3		30	ns
t <sub>ELFL</sub> t <sub>ELFH</sub>	CE# Low to BYTE# High or Low	3		5	ns

**NOTES:**

1. See AC Input/Output Reference Waveforms for timing measurements, Figures 5 and 6.
2. OE# may be delayed up to  $t_{ELQV} - t_{GLOV}$  after the falling edge of CE# without impact on  $t_{ELQV}$ .
3. Sampled, not 100% tested.
4. This timing parameter is used to latch the correct BSR data onto the outputs.

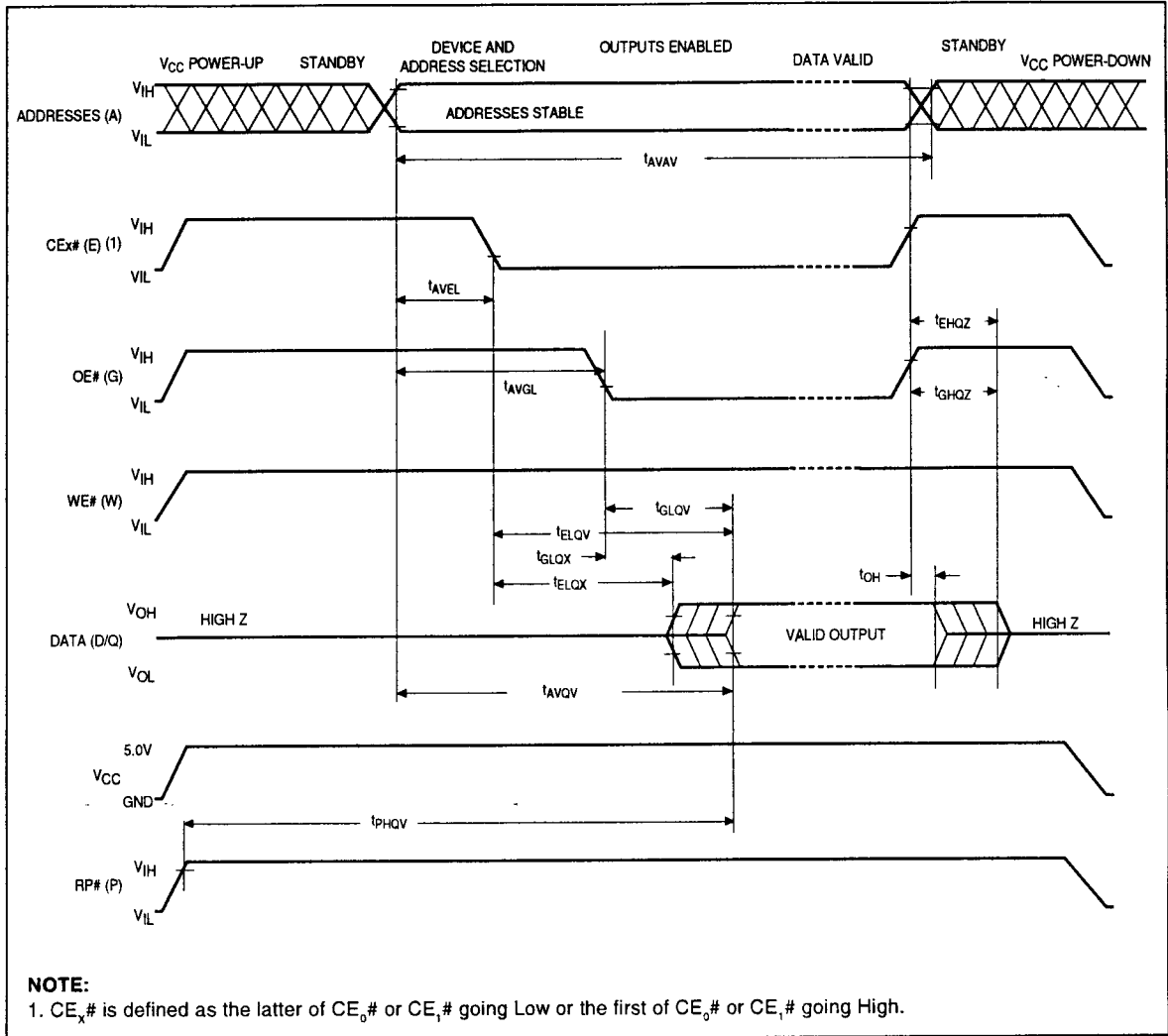
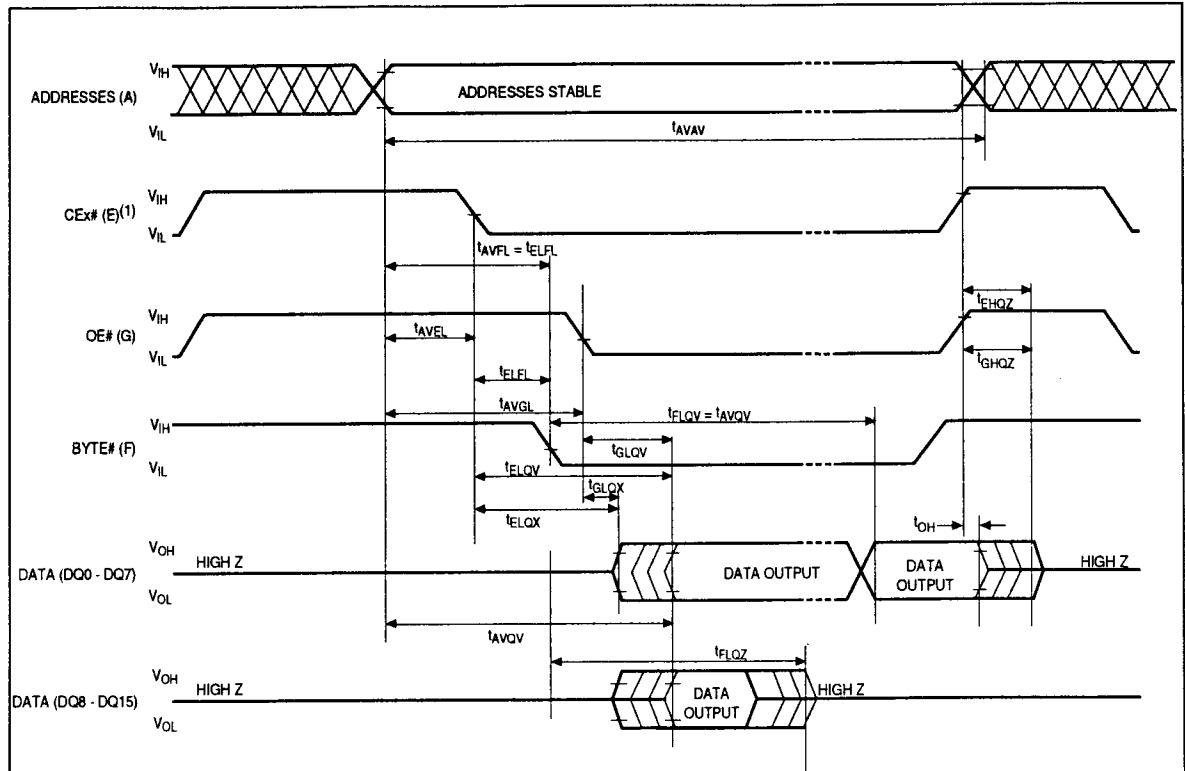


Figure 9. Read Timing Waveforms



**NOTE:**

1.  $CE_x\#$  is defined as the latter of  $CE_0\#$  or  $CE_1\#$  going Low or the first of  $CE_0\#$  or  $CE_1\#$  going High.

Figure 10. BYTE# Timing Waveforms

## 5.7 Power-Up and Reset Timings

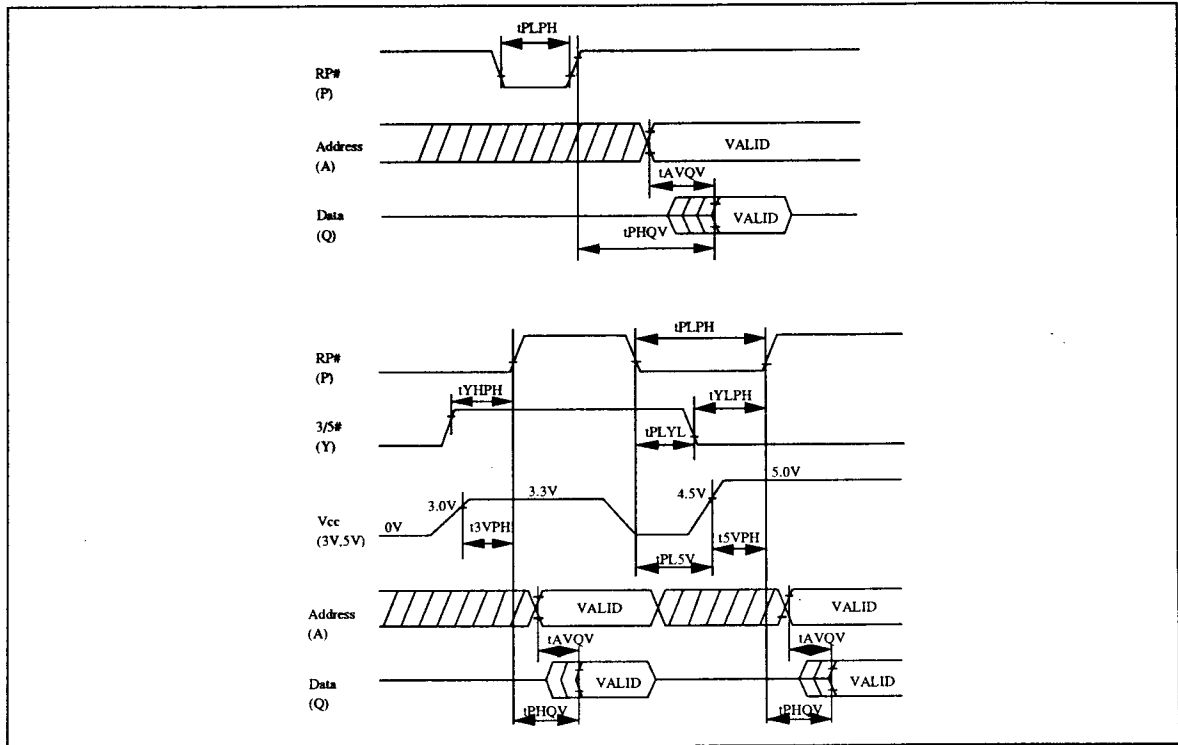


Figure 11.  $V_{CC}$  Power-Up and RP# Reset Waveforms

Symbol	Parameter	Note	Min.	Max.	Unit
tPLYL tPLYH	RP# Low to 3/5# Low (High)		0		$\mu s$
tYLPH tYHPH	3/5# Low (High) to RP# High	1	2		$\mu s$
tPL5V tPL3V	RP# Low to $V_{CC}$ at 4.5V Minimum (to $V_{CC}$ at 3.0V min or 3.6V max)	2	0		$\mu s$
tPLPH	RP# "Low" 期間		100		ns
t5VPH	$V_{CC}$ at 4.5V to RP# High	3	100		ns
t3VPH	$V_{CC}$ at 3.0V to RP# High	3	100		ns
tAVQV	Address Valid to Data Valid for $V_{CC}=5V \pm 10\%$	4		100	ns
tPHQV	RP# High to Data Valid for $V_{CC}=5V \pm 10\%$	4		550	ns

**NOTES:**

$CE_0\#$ ,  $CE_1\#$  and  $OE\#$  are switched low after Power-Up.

1. Minimum of 2  $\mu s$  is required to meet the specified  $t_{PHQV}$  times.

2. The power supply may start to switch concurrently with RP# going Low. RP# is required to stay low, until  $V_{CC}$  stays at recommended operating voltage.

3. The address access time and RP# high to data valid time are shown for 5V  $V_{CC}$  operation. Refer to the AC Characteristics Read Only Operations 3.3V  $V_{CC}$  operation and all other speed options.

5.8 AC Characteristics for WE# - Controlled Command Write Operations<sup>(1)</sup>T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Notes	V <sub>CC</sub> =3.3V±0.3V			Unit
			Min	Typ	Max	
t <sub>AVAV</sub>	Write Cycle Time		150			ns
t <sub>VPWH</sub>	V <sub>PP</sub> Setup to WE# Going High	3	100			ns
t <sub>PHEL</sub>	RP# Setup to CE# Going Low		480			ns
t <sub>ELWL</sub>	CE# Setup to WE# Going Low		10			ns
t <sub>AVWH</sub>	Address Setup to WE# Going High	2,6	75			ns
t <sub>DVWH</sub>	Data Setup to WE# Going High	2,6	75			ns
t <sub>WLWH</sub>	WE# Pulse Width		75			ns
t <sub>WHDX</sub>	Data Hold from WE# High	2	10			ns
t <sub>WHAX</sub>	Address Hold from WE# High	2	10			ns
t <sub>WHEH</sub>	CE# Hold from WE# High		10			ns
t <sub>WHWL</sub>	WE# Pulse Width High		75			ns
t <sub>GHWL</sub>	Read Recovery before Write		0			ns
t <sub>WHRL</sub>	WE# High to RY/BY# Going Low				100	ns
t <sub>RHPL</sub>	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t <sub>PHWL</sub>	RP# High Recovery to WE# Going Low		1			μs
t <sub>WHGL</sub>	Write Recovery before Read		120			ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			μs
t <sub>WHQV1</sub>	Duration of Word/Byte Write Operation	4,5	5	12		μs
t <sub>WHQV2</sub>	Duration of Block Erase Operation	4	0.3			s



AC Characteristics for WE# - Controlled Command Write Operations<sup>(1)</sup> (Continued)T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Notes	V <sub>CC</sub> =5.0V±0.5V			Unit
			Min	Typ	Max	
t <sub>AVAV</sub>	Write Cycle Time		100			ns
t <sub>VPWH</sub>	V <sub>PP</sub> Setup to WE# Going High	3	100			ns
t <sub>PHEL</sub>	RP# Setup to CE# Going Low		480			ns
t <sub>ELWL</sub>	CE# Setup to WE# Going Low		0			ns
t <sub>AVWH</sub>	Address Setup to WE# Going High	2,6	50			ns
t <sub>DVWH</sub>	Data Setup to WE# Going High	2,6	50			ns
t <sub>WLWH</sub>	WE# Pulse Width		50			ns
t <sub>WHDX</sub>	Data Hold from WE# High	2	0			ns
t <sub>WHAX</sub>	Address Hold from WE# High	2	10			ns
t <sub>WHEH</sub>	CE# Hold from WE# High		10			ns
t <sub>WHWL</sub>	WE# Pulse Width High		50			ns
t <sub>GHWL</sub>	Read Recovery before Write		0			ns
t <sub>WHRL</sub>	WE# High to RY/BY# Going Low				100	ns
t <sub>RHPL</sub>	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t <sub>PHWL</sub>	RP# High Recovery to WE# Going Low		1			μs
t <sub>WHGL</sub>	Write Recovery before Read		80			ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			μs
t <sub>WHQV1</sub>	Duration of Word/Byte Write Operation	4,5	4.5	8		μs
t <sub>WHQV2</sub>	Duration of Block Erase Operation	4	0.3			s

**NOTES:**CE# is defined as the latter of CE<sub>n</sub># or CE<sub>n</sub># going Low or the first of CE<sub>n</sub># or CE<sub>n</sub># going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of WE# for all Command Write operations.

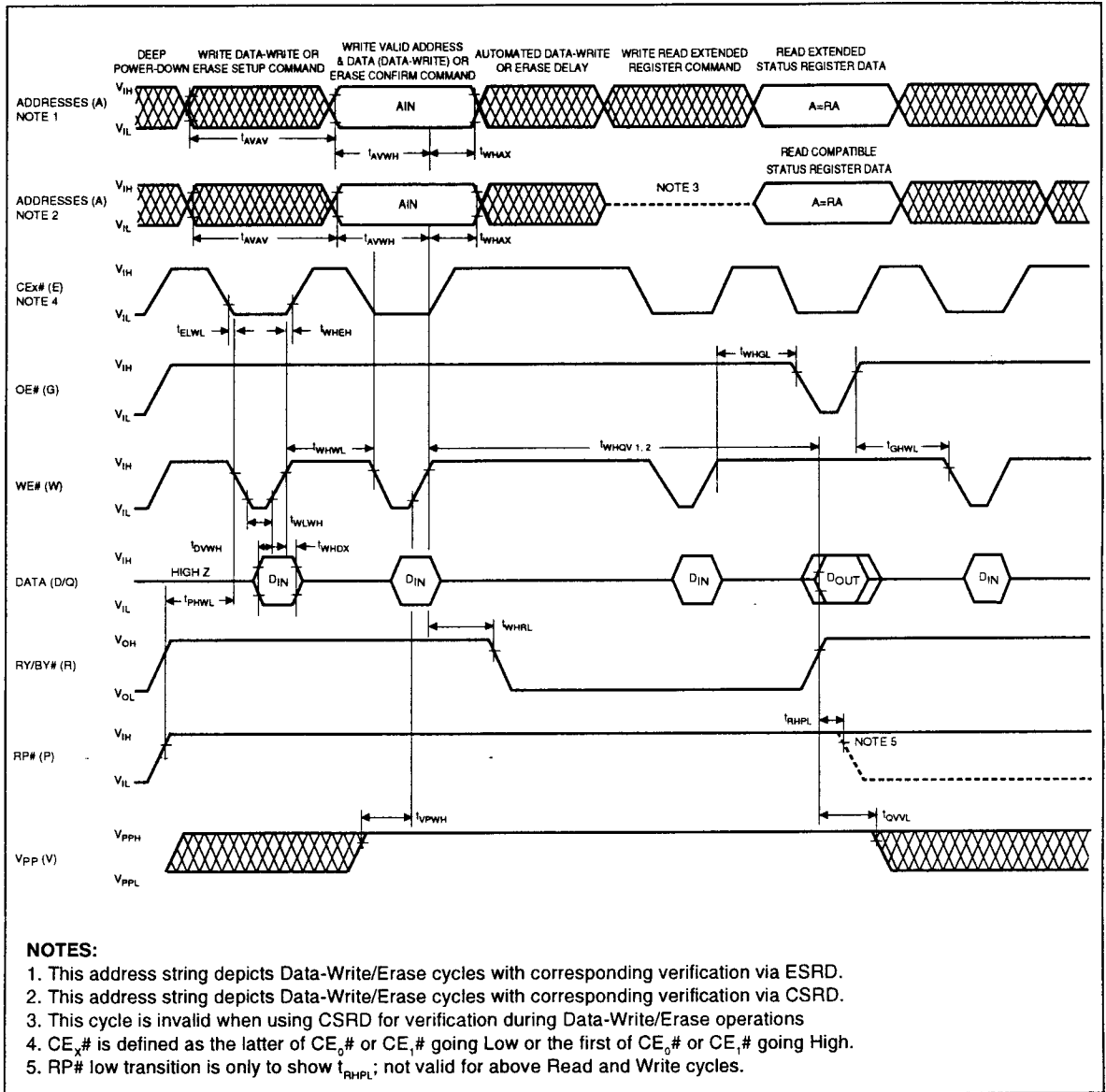


Figure 12. AC Waveforms for Command Write Operations

5.9 AC Characteristics for CE# - Controlled Command Write Operations<sup>(1)</sup>T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Notes	V <sub>CC</sub> =3.3V±0.3V			Unit
			Min	Typ	Max	
t <sub>AVAV</sub>	Write Cycle Time		150			ns
t <sub>PHWL</sub>	RP# Setup to WE# Going Low	3	480			ns
t <sub>VPEH</sub>	V <sub>PP</sub> Setup to CE# Going High	3	100			ns
t <sub>WLEL</sub>	WE# Setup to CE# Going Low		0			ns
t <sub>AVEH</sub>	Address Setup to CE# Going High	2,6	75			ns
t <sub>DVEH</sub>	Data Setup to CE# Going High	2,6	75			ns
t <sub>ELEH</sub>	CE# Pulse Width		75			ns
t <sub>EHDX</sub>	Data Hold from CE# High	2	10			ns
t <sub>EHAX</sub>	Address Hold from CE# High	2	10			ns
t <sub>EHWH</sub>	WE# Hold from CE# High		10			ns
t <sub>EHEL</sub>	CE# Pulse Width High		75			ns
t <sub>GHEL</sub>	Read Recovery before Write		0			ns
t <sub>EHRL</sub>	CE# High to RY/BY# Going Low				100	ns
t <sub>RHPL</sub>	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t <sub>PHEL</sub>	RP# High Recovery to CE# Going Low		1			μs
t <sub>EHGL</sub>	Write Recovery before Read		120			ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			μs
t <sub>EHQV1</sub>	Duration of Word/Byte Write Operation	4,5	5	12		μs
t <sub>EHQV2</sub>	Duration of Block Erase Operation	4	0.3			s

AC Characteristics for CE# - Controlled Command Write Operations<sup>(1)</sup> (Continued)T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Notes	V <sub>CC</sub> =5.0V±0.5V			Unit
			Min	Typ	Max	
t <sub>AVAV</sub>	Write Cycle Time		100			ns
t <sub>PHWL</sub>	RP# Setup to WE# Going Low	3	480			ns
t <sub>VPEH</sub>	V <sub>PP</sub> Setup to CE# Going High	3	100			ns
t <sub>WLEL</sub>	WE# Setup to CE# Going Low		0			ns
t <sub>AVEH</sub>	Address Setup to CE# Going High	2,6	50			ns
t <sub>DVEH</sub>	Data Setup to CE# Going High	2,6	50			ns
t <sub>LEH</sub>	CE# Pulse Width		0			ns
t <sub>EHDX</sub>	Data Hold from CE# High	2	10			ns
t <sub>EHAX</sub>	Address Hold from CE# High	2	10			ns
t <sub>EHWH</sub>	WE# Hold from CE# High		10			ns
t <sub>EHEL</sub>	CE# Pulse Width High		50			ns
t <sub>GH</sub>	Read Recovery before Write		0			ns
t <sub>EHRL</sub>	CE# High to RY/BY# Going Low				100	ns
t <sub>RHPL</sub>	RP# Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High	3	0			ns
t <sub>PH</sub>	RP# High Recovery to CE# Going Low		1			µs
t <sub>EHGL</sub>	Write Recovery before Read		80			ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid Status Register (CSR, GSR, BSR) Data and RY/BY# High		0			µs
t <sub>EHQV1</sub>	Duration of Word/Byte Write Operation	4,5	4.5	8		µs
t <sub>EHQV2</sub>	Duration of Block Erase Operation	4	0.3			s

**NOTES:**

CE# is defined as the latter of CE<sub>0</sub># or CE<sub>1</sub># going Low or the first of CE<sub>0</sub># or CE<sub>1</sub># going High.

1. Read timing during write and erase are the same as for normal read.
2. Refer to command definition tables for valid address and data values.
3. Sampled, but not 100% tested.
4. Write/Erase durations are measured to valid Status Register (CSR) Data.
5. Word/Byte write operations are typically performed with 1 Programming Pulse.
6. Address and Data are latched on the rising edge of CE# for all Command Write Operations.

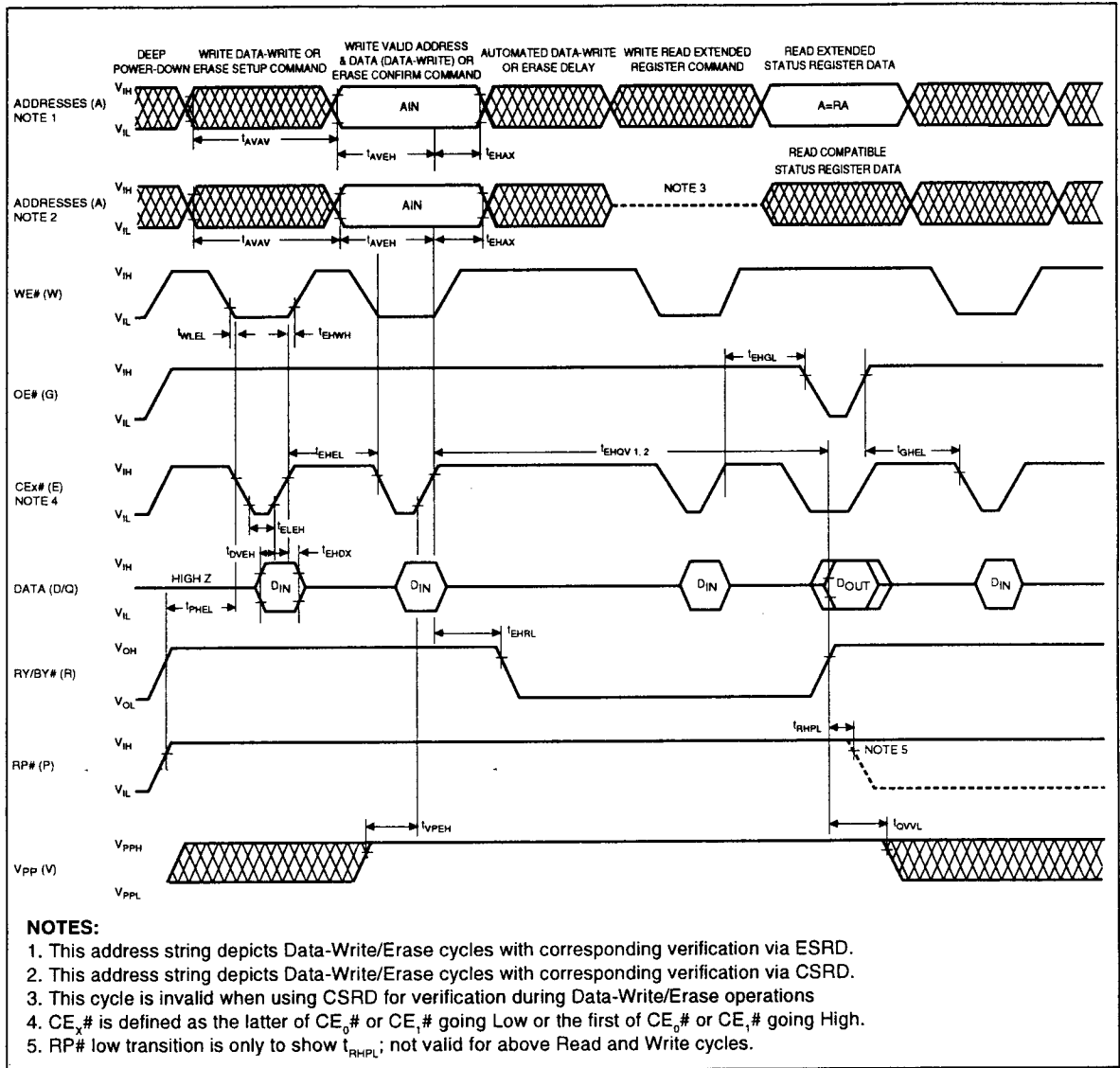


Figure 13. Alternate AC Waveforms for Command Write Operations

### 5.10 AC Characteristics for Page Buffer Write Operations<sup>(1)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Notes	V <sub>CC</sub> =3.3V±0.3V			Unit
			Min	Typ	Max	
t <sub>AVAV</sub>	Write Cycle Time		150			ns
t <sub>ELWL</sub>	CE# Setup to WE# Going Low		10			ns
t <sub>AVWL</sub>	Address Setup to WE# Going Low	3	0			ns
t <sub>DVWH</sub>	Data Setup to WE# Going High	2	75			ns
t <sub>WLWH</sub>	WE# Pulse Width		75			ns
t <sub>WHDX</sub>	Data Hold from WE# High	2	10			ns
t <sub>WHAX</sub>	Address Hold from WE# High	2	10			ns
t <sub>WHEH</sub>	CE# Hold from WE# High		10			ns
t <sub>WHWL</sub>	WE# Pulse Width High		75			ns
t <sub>GHWL</sub>	Read Recovery before Write		0			ns
t <sub>WHGL</sub>	Write Recovery before Read		120			ns

Symbol	Parameter	Notes	V <sub>CC</sub> =5.0V±0.5V			Unit
			Min	Typ	Max	
t <sub>AVAV</sub>	Write Cycle Time		100			ns
t <sub>ELWL</sub>	CE# Setup to WE# Going Low		0			ns
t <sub>AVWL</sub>	Address Setup to WE# Going Low	3	0			ns
t <sub>DVWH</sub>	Data Setup to WE# Going High	2	50			ns
t <sub>WLWH</sub>	WE# Pulse Width		50			ns
t <sub>WHDX</sub>	Data Hold from WE# High	2	0			ns
t <sub>WHAX</sub>	Address Hold from WE# High	2	10			ns
t <sub>WHEH</sub>	CE# Hold from WE# High		10			ns
t <sub>WHWL</sub>	WE# Pulse Width High		50			ns
t <sub>GHWL</sub>	Read Recovery before Write		0			ns
t <sub>WHGL</sub>	Write Recovery before Read		80			ns

**NOTES:**

CE# is defined as the latter of CE<sub>0</sub># or CE<sub>1</sub># going Low or the first of CE<sub>0</sub># or CE<sub>1</sub># going High.

1. These are WE#-controlled write timings, equivalent CE#-controlled write timings apply.
2. Sampled, but not 100% tested.
3. Address must be valid during the entire WE# Low pulse.

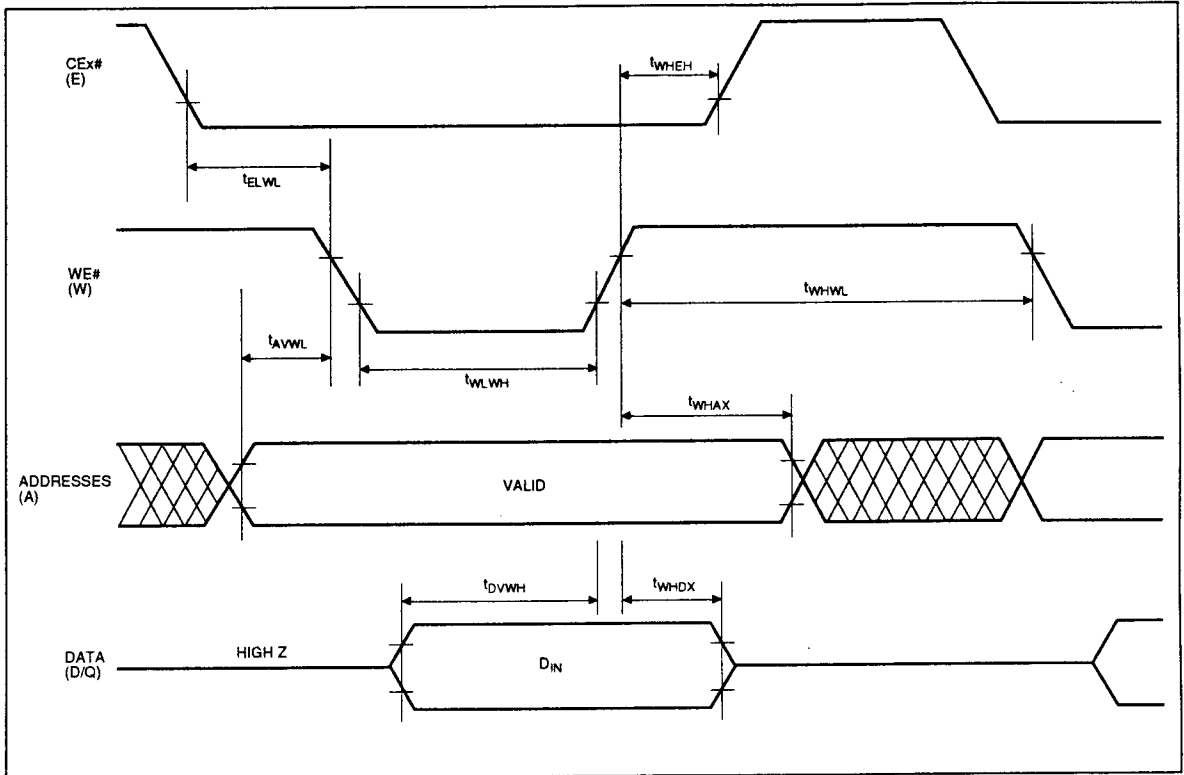


Figure 14. Page Buffer Write Timing Waveforms

## 5.11 Erase and Word/Byte Write Performance

$V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Symbol	Parameter	Notes	Min	Typ <sup>(1)</sup>	Max	Units	Test Conditions
t <sub>WHRH1</sub>	Word/Byte Write Time	2		12		μs	
t <sub>WHRH2</sub>	Block Write Time	2		0.8	2.1	s	Byte Write Mode
t <sub>WHRH3</sub>	Block Write Time	2		0.4	1.0	s	Word Write Mode
	Block Erase Time	2		0.9	10	s	
	Full Chip Erase Time	2		28.8		s	

$V_{CC} = 5.0V \pm 0.5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

Symbol	Parameter	Notes	Min	Typ <sup>(1)</sup>	Max	Units	Test Conditions
t <sub>WHRH1</sub>	Word/Byte Write Time	2		8		μs	
t <sub>WHRH2</sub>	Block Write Time	2		0.54	2.1	s	Byte Write Mode
t <sub>WHRH3</sub>	Block Write Time	2		0.27	1.0	s	Word Write Mode
	Block Erase Time	2		0.7	10	s	
	Full Chip Erase Time	2		22.4		s	

**NOTES:**

1. 25°C,  $V_{PP} = 5.0V$ .
2. Excludes System-Level Overhead.



LH28Fxxx FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM  
READ ONLY MEMORY ETOX LH28F016SUHT-10 16M (1M x 16/2M x 8)