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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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2SK2569

Silicon N-Channel MOS FET

RENESAS

ADE-208-384 (Z)
1st. Edition
Aug. 1995

Application

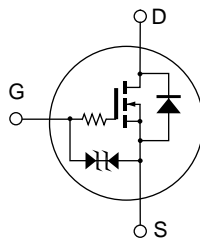
Low frequency power switching

Features

- Low on-resistance.
- $R_{DS(on)} = 2.6 \text{ max.}$ (at $V_{GS} = 4 \text{ V}$, $I_D = 100\text{mA}$)
- 2.5V gate drive device.
- Small package (MPAK).

Outline

MPAK



1. Source
2. Gate
3. Drain

Absolute Maximum Ratings (Ta = 25°C)

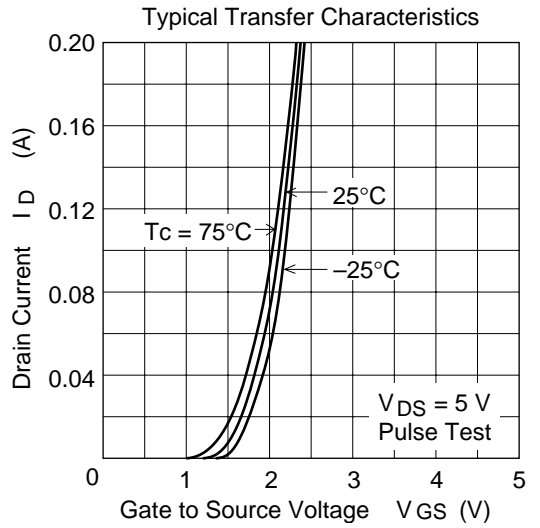
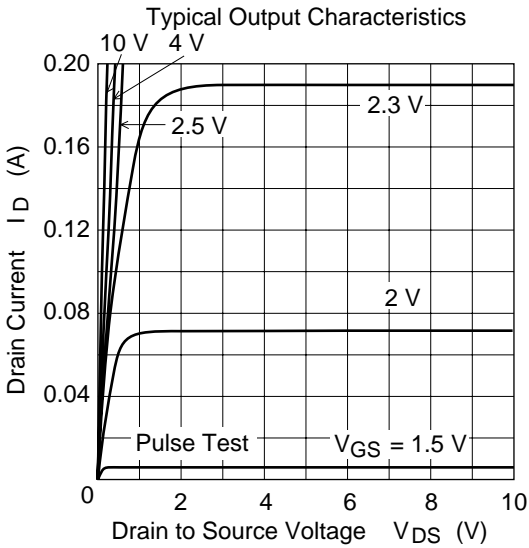
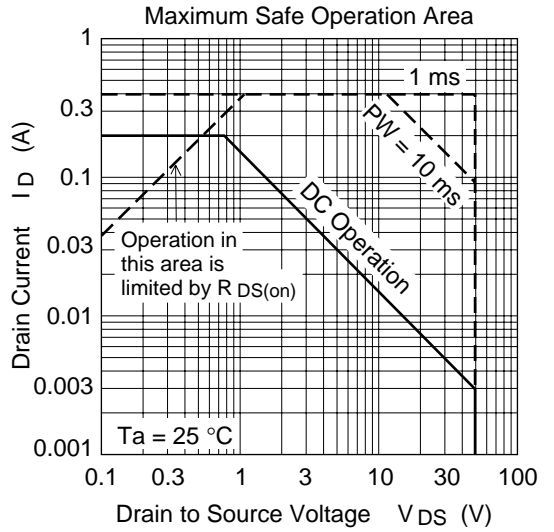
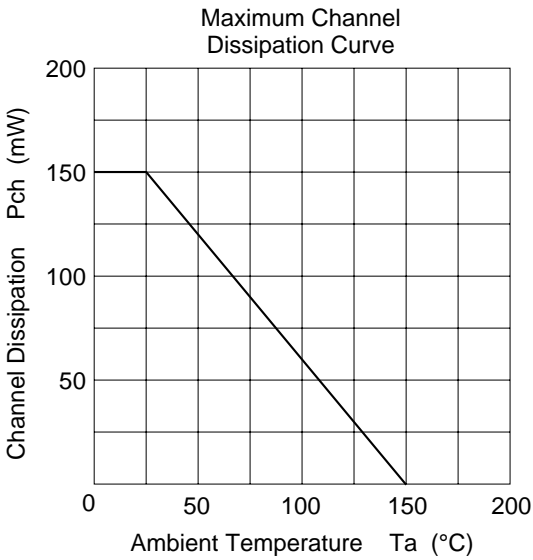
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	50	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	0.2	A
Drain peak current	$I_{D(pulse)}^{*1}$	0.4	A
Channel dissipation	P_{ch}^{*2}	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes 1. PW 10 μs, duty cycle 1 %

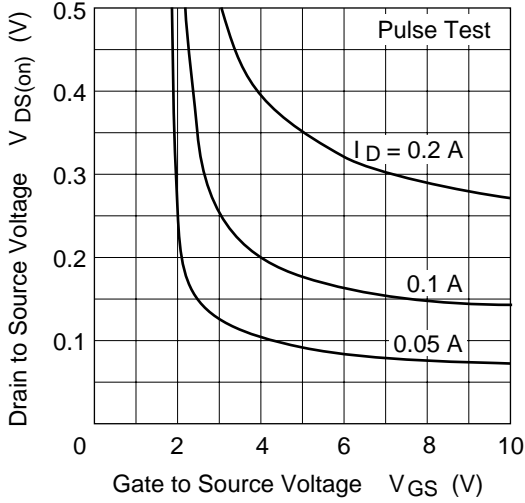
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	50	—	—	V	$I_D = 100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 40 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±2.0	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$I_D = 10 \mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)1}$	—	2.0	2.6		$I_D = 100 mA$ $V_{GS} = 4 V^{*1}$
Static drain to source on state resistance	$R_{DS(on)2}$	—	3.1	5.0		$I_D = 40 mA$ $V_{GS} = 2.5 V^{*1}$
Foward transfer admittance	$ y_{fs} $	0.13	0.23	—	S	$I_D = 100 mA$ $V_{DS} = 10 V$
Input capacitance	C_{iss}	—	14.0	—	pF	$V_{DS} = 10 V$
Output capacitance	C_{oss}	—	17.2	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	1.73	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	40	—	μs	$V_{GS} = 10 V, I_D = 100 mA$
Rise time	t_r	—	86	—	μs	$R_L = 300$
Turn-off delay time	$t_{d(off)}$	—	1120	—	μs	
Fall time	t_f	—	430	—	μs	

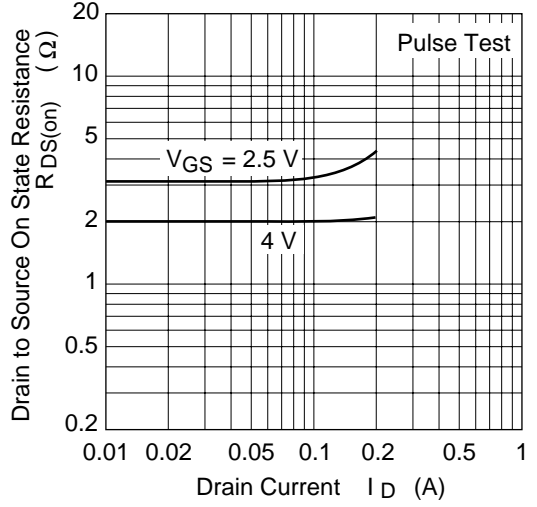
Notes 1. Pulse Test
2. Marking is "ZN-"



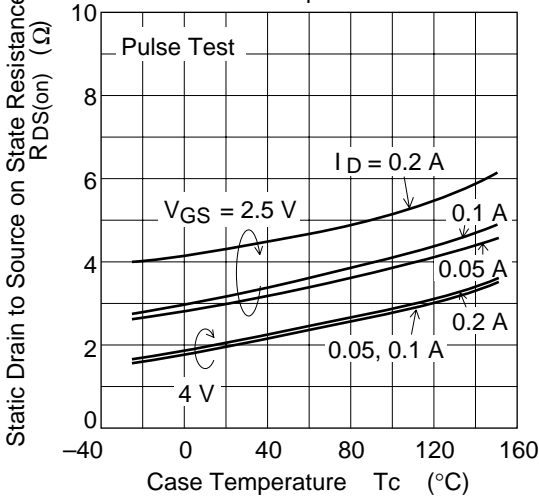
Drain to Source Saturation Voltage vs. Gate to Source Voltage



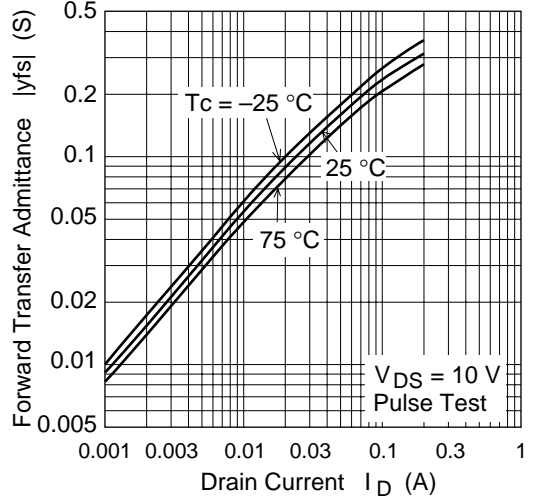
Static Drain to Source on State Resistance vs. Drain Current

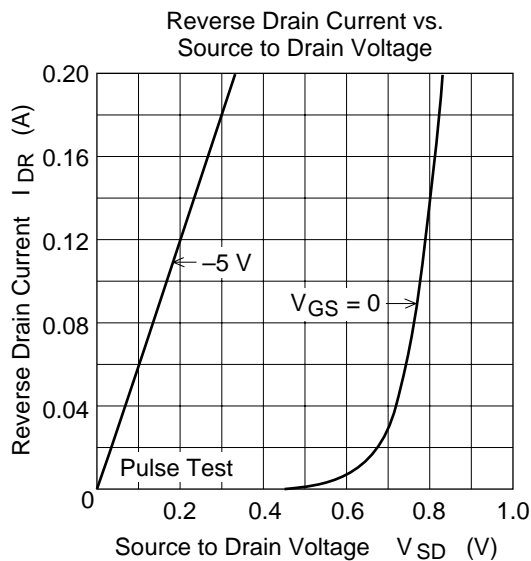
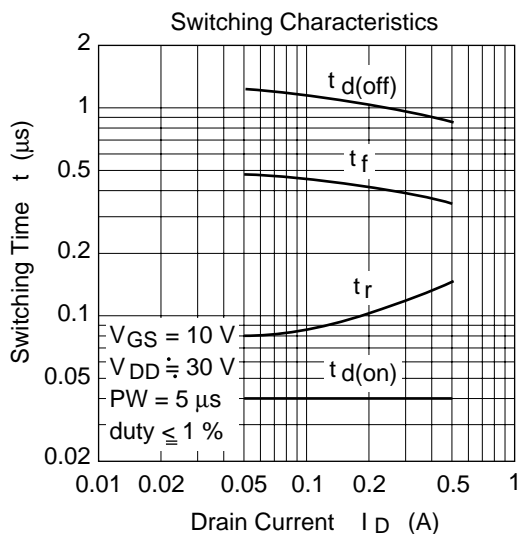
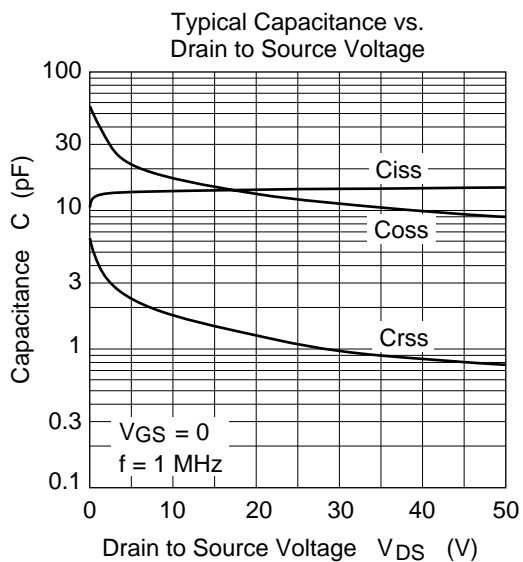


Static Drain to Source on State Resistance vs. Temperature

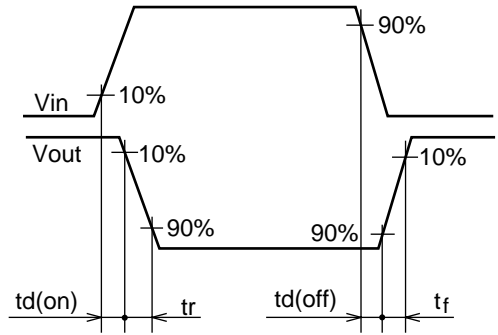
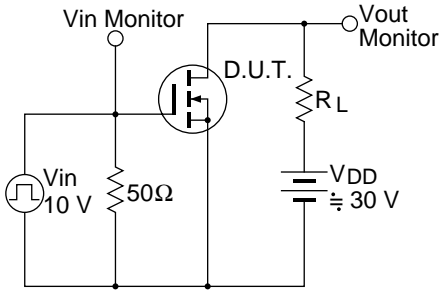


Forward Transfer Admittance vs. Drain Current





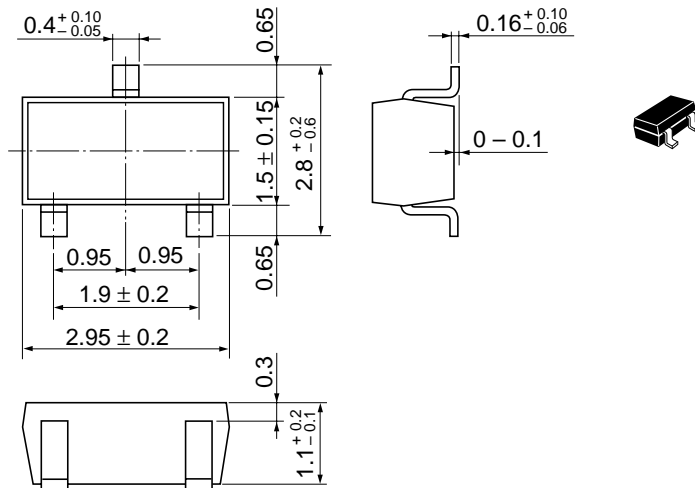
Avalanche Test Circuit and Waveform



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

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