FEATURES

- 8-Bit Resolution and Accuracy
- No Missing Codes over Full Temperature Range
- 6μs Conversion Time
- Flexible μP Interface
- 2.5mA Maximum Standby Current
- Replaces AD7574 with Improved Speed
- Available in Die Form

ORDERING INFORMATION †

		PACKAGE: 18-PIN DIP AND SO		
INL (LSB)	DNL (LSB)	MILITARY* TEMPERATURE −55°C TO +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO +70°C
±1/2	±3/4	ADC908AX	ADC908EX	ADC908GP
±3/4	±7/8	ADC908BX	ADC908FX	—
±3/4	±7/8	—	ADC908FP	—
±3/4	±7/8	—	ADC908FS	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

GENERAL DESCRIPTION

The ADC-908 is a monolithic CMOS successive-approximation analog-to-digital converter. When used with a 1.35MHz clock, a conversion time of 6μs is achieved, with full accuracy over the operating temperature range.

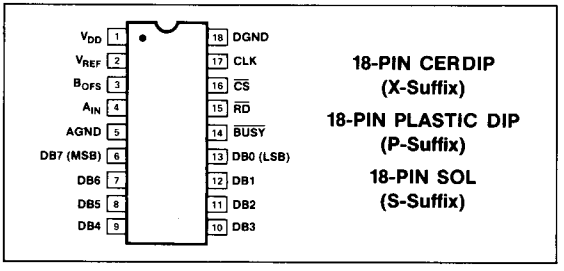
The ADC-908 outputs use 3-state logic, allowing direct connection to the data bus or system input port. Active-LOW chip select ($\overline{CS}$) and read/write ($\overline{RD}$) inputs are used to control all operations. This input structure permits the ADC-908 to be used as a memory-mapped input device. Depending on the control timing waveforms, the ADC-908 is interfaced like static RAM, ROM, or slow memory.

The low power consumption of the ADC-908 is derived from a single +5V supply. A negative reference voltage must also be supplied. Optimum accuracy is achieved when the reference is at −10.00V with a low output resistance. For a low-cost precision −10V/−10.24V reference, ask your PMI sales representative about the REF-08.

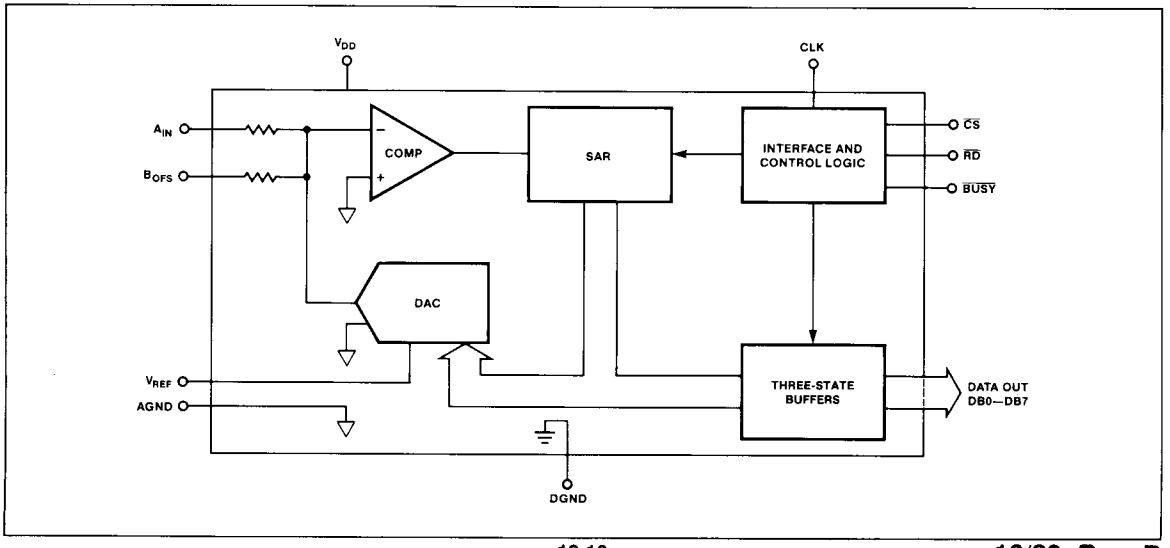
With its on-board comparator, interface logic, optional internal clock, and +5V operation, the ADC-908 is the ideal low-cost solution for microprocessor-based 8-bit A/D systems.

PMI's ADC-908 is pin-and-function compatible with the PM-7574, but offers faster conversion time and faster microprocessor bus interface timing. Conversion time has been reduced by 60% and most key timing specifications, including data access time, START command propagation delay (t_{WBPD}), and reset time, have been improved.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to AGND ..... 0V, +7.0V
V_{DD} to DGND ..... 0V, +7.0V
AGND to DGND ..... –0.3V, V_{DD}
$\overline{CS}$, $\overline{RD}$ to DGND ..... –0.3V, V_{DD} + –.3V
DB_0-DB_7 to DGND ..... –0.3V, V_{DD}
CLK, $\overline{BUSY}$ to DGND ..... –0.3, V_{DD}
B_{OFS}, A_{IN} ..... ±20V
V_{REF} ..... 0V, –20V
Operating Temperature Range
ADC-908AX, BX ..... –55°C to +125°C
ADC-908EX, FX, FP, FS ..... –40°C to +85°C
ADC-908GP ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W
18-Pin Plastic DIP (P)	70	30	°C/W
18-Pin SOL (S)	88	25	°C/W

NOTES:
1. Digital pins are zener protected. However, proper ESD handling precautions are recommended.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = –10V, Unipolar Configuration, R_{CLK} = 43kΩ, C_{CLK} = 100pF; –40°C ≤ T_A ≤ +85°C for ADC-908E/F, 0°C ≤ T_A ≤ +70°C for ADC-908G, –55°C ≤ T_A ≤ +125°C for ADC-908A/B, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-908 MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	N		8	–	–	Bits
Integral Nonlinearity	INL	A/E/G Grades	–1/2	–	+1/2	LSB
		B/F Grades	–3/4	–	+3/4	
Differential Nonlinearity	DNL	A/E/G Grades	–3/4	–	+3/4	LSB
		B/F Grades	–7/8	–	+7/8	
Gain Error	G_{FSE}	A/E/G Grades T_A = +25°C	–3	–	+3	LSB
		T_A = Full Temp Range	–4.5	–	+4.5	
		B/F Grades T_A = +25°C	–5	–	+5	
		T_A = Full Temp Range	–6.5	–	+6.5	
Offset Error	V_{ZSE}	A/E/G Grades T_A = +25°C	–30	–	+30	mV
		T_A = Full Temp Range	–50	–	+50	
		B/F Grades T_A = +25°C	–60	–	+60	
		T_A = Full Temp Range	–80	–	+80	
ANALOG INPUTS						
Resistance Mismatch B_{OFS} to A_{IN}	ΔR_{AB}		–1	–	+1	%
Input Resistance at V_{REF} (Note 1)	R_{REF}		5	–	15	kΩ
Input Resistance at B_{OFS}, A_{IN}	R_{BOFS} R_{AIN}		10	–	30	kΩ
Reference Voltage Range	V_{REF}	Specified Conversion Accuracy	–	–10	–	V
Reference Voltage Range	V_{REF}	Degraded Conversion Accuracy	–5	–	–15	V
Reference Current (Note 6)	I_{REF}	Conversion Complete Prior to Reset	–	–	2.4	mA
Nominal Analog Input Range						
Unipolar Mode	V_{INU}		–	0 to + $\lvert V_{REF}\rvert$	–	V
Bipolar Mode	V_{INB}		–	–$\lvert V_{REF}\rvert$ to +$\lvert V_{REF}\rvert$	–	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = –10V, Unipolar Configuration, R_{CLK} = 43kΩ, C_{CLK} = 100pF; –40°C ≤ T_A ≤ +85°C for ADC-908E/F, 0°C ≤ T_A ≤ +70°C for ADC-908G, –55°C ≤ T_A ≤ +125°C for ADC-908A/B, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	ADC-908 MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input HIGH Voltage $\overline{RD}$, $\overline{CS}$ Inputs	V_{IH}		2.4	—	—	V
Input LOW Voltage $\overline{RD}$, $\overline{CS}$ Inputs	V_{IL}		—	—	0.8	V
Input Current $\overline{RD}$, $\overline{CS}$ Inputs	I_{IN}	T_A = +25°C T_A = Full Temp Range	— —	— —	1 10	µA
Input Capacitance $\overline{RD}$, $\overline{CS}$ Inputs (Note 6)	C_{IN}		—	—	5	pF
Input HIGH Voltage, Clock Input	V_{IH}		2.4	—	—	V
Input LOW Voltage, Clock Input	V_{IL}		—	—	0.8	V
Input HIGH Current, Clock Input	I_{IH}		—	—	2	mA
Input LOW Current, Clock Input	I_{IL}	T_A = +25°C T_A = Full Temp Range	— —	— —	1 10	µA
LOGIC OUTPUTS						
Output HIGH Voltage $\overline{BUSY}$, DB0-7	V_{OH}	I_{SOURCE} = 40µA	4.0	—	—	V
Output LOW Voltage $\overline{BUSY}$, DB0-7	V_{OL}	I_{SINK} = 1.6mA	—	—	0.4	V
Floating Leakage Current, DB0-7	I_{LKG}	T_A = +25°C T_A = Full Temp Range	— —	— —	1 10	µA
Floating State Output Capacitance	C_{OZ}	(Note 6)	—	—	7	pF
POWER REQUIREMENTS						
Standby Current	I_{DD}	V_{DD} = +4.75V to +5.25V	—	—	2.5	mA
DIGITAL INTERFACE TIMING						
$\overline{CS}$ Minimum Pulse Width (Note 6)	t_{CS}	T_A = +25°C T_A = T_{MIN} T_A = T_{MAX}	60 50 90	— — —	— — —	ns
$\overline{RD}$ to $\overline{CS}$ Setup Time (Note 6)	t_{WSCS}		0	—	—	ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 6)	t_{CBPD}	$\overline{BUSY}$ Load = 20pF T_A = +25°C T_A = T_{MIN} T_A = T_{MAX} $\overline{BUSY}$ Load = 100pF T_A = +25°C T_A = T_{MIN} T_A = T_{MAX}	 — — — — — —	 — — — — — —	 120 100 150 150 120 200	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time (Notes 2, 6)	t_{BSR}		0	—	—	ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time (Note 6)	t_{BSCS}		0	—	—	ns

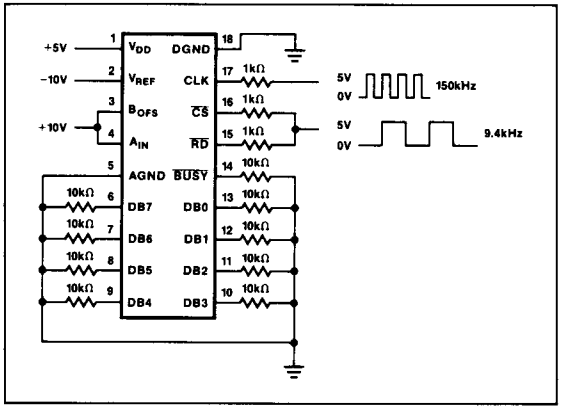
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = −10V, Unipolar Configuration, R_{CLK} = 43kΩ, C_{CLK} = 100pF; −40°C ≤ T_A ≤ +85°C for ADC-908E/F, 0°C ≤ T_A ≤ +70°C for ADC-908G, −55°C ≤ T_A ≤ +125°C for ADC-908A/B, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	ADC-908 MIN	ADC-908 TYP	ADC-908 MAX	UNITS
Data Access Time (Note 6)	t_{RAD}	C_L = 20pF				ns
		T_A = +25°C	—	—	140	
		T_A = T_{MIN}	—	—	100	
		T_A = T_{MAX}	—	—	200	
		C_L = 100pF				
		T_A = +25°C	—	—	170	
		T_A = T_{MIN}	—	—	150	
		T_A = T_{MAX}	—	—	230	
Data Hold Time (Notes 3, 6)	t_{RHD}	T_A = +25°C (Note 3)	30	—	100	ns
		T_A = T_{MIN}	20	—	70	
		T_A = T_{MAX}	40	—	140	
$\overline{CS}$ to $\overline{RD}$ Hold Time (Note 6)	t_{RHCS}	T_A = +25°C	—	—	200	ns
		T_A = T_{MIN}	—	—	120	
		T_A = T_{MAX}	—	—	250	
Reset Time Requirement (Note 6)	t_{RESET}	T_A = +25°C	450	—	—	ns
		T_A = Full Temp. Range	500	—	—	
Conversion Time (Note 4) (Notes 4, 5, 6)	$t_{CONVERT}$	Static RAM Mode External Clock f = 1.35MHz	—	—	6	µs
		ROM Mode Internal Clock	—	—	7	
$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay, ROM Mode (Notes 4, 5, 6)	t_{WBPD}	C_L = 20pF				ns
		T_A = +25°C	—	—	600	
		T_A = T_{MIN}	—	—	400	
		T_A = T_{MAX}	—	—	800	

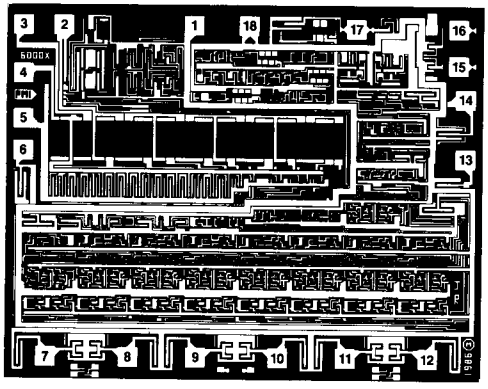
NOTES:

1. For optimum gain accuracy over the full temperature range, the source resistance at pin 2 should be kept low.
2. In ROM mode, $\overline{RD}$ can go LOW prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH.
3. Output loading 10pF. A 3kΩ pullup resistor to +5V is used for V_{OL} to High-Z, for V_{OH} to High-Z, a 3kΩ pulldown to GND is used. Measured to 0.5V output change.
4. When using the ADC-908 internal oscillator, actual conversion time depends on clock resistor and capacitor as well as temperature.
5. ROM interface mode conversion times are typically 1µs longer than conversion times for other modes, but the ROM interface mode includes an automatic reset in the conversion time.
6. Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.129 × 0.103 inch, 13,287 sq. mils
(3.28 × 2.62 mm, 8.58 sq. mm)

1. V_{DD}
2. V_{REF}
3. B_{OFS}
4. A_{IN}
5. AGND
6. DB7(MSB)
7. DB6
8. DB5
9. DB4
10. DB3
11. DB2
12. DB1
13. DB0(LSB)
14. $\overline{BUSY}$
15. $\overline{RD}$
16. $\overline{CS}$
17. CLK
18. DGND

For additional DICE ordering infromation, refer to PMI's Data Book, Secion 2.

WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = −10.000V, AGND = DGND = 0V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-908 LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Integral Nonlinearity	INL		±3/4	LSB MAX
Differential Nonlinearity	DNL		±7/8	LSB MAX
Gain Error	G_{FSE}		±5	LSB MAX
Offset Error	V_{ZSE}		±60	mV MAX
ANALOG INPUTS				
Resistance Mismatch B_{OFS} to A_{IN}	ΔR_{AB}		±1	% MAX
Input Resistance at V_{REF}	R_{REF}		5/15	kΩ MIN/MAX
Input Resistance at B_{OFS}, A_{IN}	R_{BOFS}, R_{IN}		10/30	kΩ MIN/MAX
DIGITAL INPUTS				
Input HIGH Voltage at $\overline{RD}$, $\overline{CS}$ Inputs	V_{IH}		2.4	V MIN
Input LOW Voltage at $\overline{RD}$, $\overline{CS}$ Inputs	V_{IL}		0.8	V MAX
Input Current $\overline{RD}$, $\overline{CS}$ Inputs	I_{IN}		±1	μA MAX
Input HIGH Voltage Clock Input	V_{IH}		2.4	V MIN
Input LOW Voltage Clock Input	V_{IL}		0.8	V MAX
Input HIGH Current Clock Input	I_{IH}		2	mA MAX
Input LOW Current Clock Input	I_{IL}		1	μA MAX

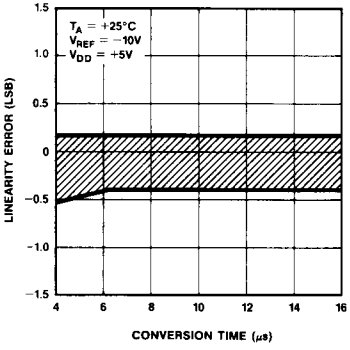
WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = −10.000V, AGND = DGND = 0V, T_A = +25°C, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	ADC-908 LIMIT	UNITS
DIGITAL OUTPUTS				
Output HIGH Voltage $\overline{BUSY}$, DB0-7	V_{OH}	I_{SOURCE} = 40μA	4	V MIN
Output LOW Voltage $\overline{BUSY}$, DB0-7	V_{OL}	I_{SINK} = 1.6mA	0.4	V MAX
Floating Leakage Current	I_{LKG}		1	μA
POWER REQUIREMENTS				
Standby Current	I_{DD}	V_{DD} = +4.75V to 5.25V	2.5	mA MAX
TIMING				
Conversion Time	$t_{CONVERT}$	Static RAM Mode, External Clock, f = 1.35MHz	6	μs MAX

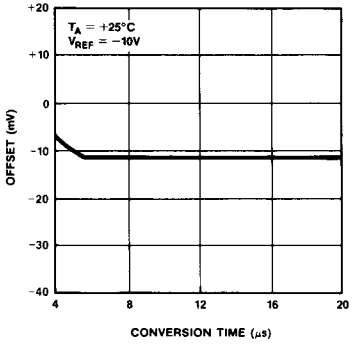
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

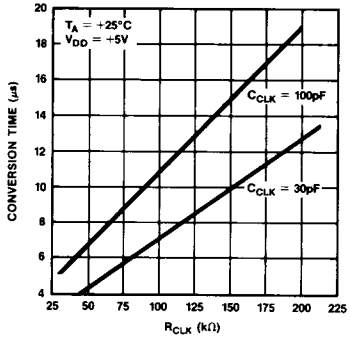
LINEARITY ERROR vs CONVERSION TIME



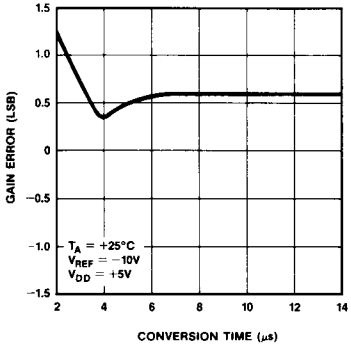
OFFSET ERROR vs CONVERSION TIME RAM MODE



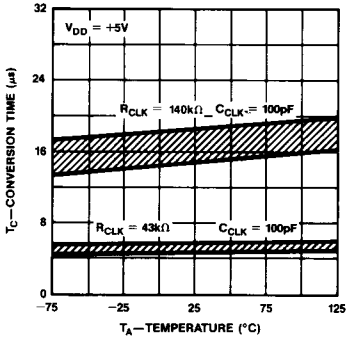
CONVERSION TIME vs R_{CLK} AND C_{CLK}



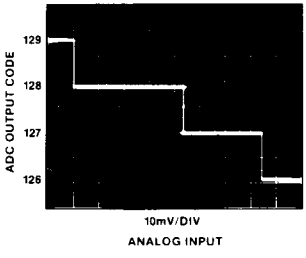
GAIN ERROR vs CONVERSION TIME



CONVERSION TIME vs TEMPERATURE WITH INTERNAL CLOCK



CONVERSION UNCERTAINTY AROUND MAJOR CARRY



GENERAL CIRCUIT INFORMATION

The ADC-908 is an 8-bit analog-to-digital converter which uses a successive approximation technique to convert an unknown analog input into a digital code output. The control logic inputs allow easy interface to most microprocessors while three-state outputs allow direct connection to the data bus. Most applications require only passive RC clock components, a −10V reference, and a +5V power supply. The RC-timed internal clock may be used, or an external clock may be applied to the ADC to maximize performance.

When a Start Conversion command is applied to the $\overline{CS}$ or $\overline{RD}$ inputs (see Operating Descriptions for details), $\overline{BUSY}$ goes LOW indicating a conversion in progress. $\overline{BUSY}$ may be used as an interrupt to halt the controlling microprocessor during conversion or may be polled to prevent premature data reads.

Starting with the most significant bit (MSB), each successive bit in the DAC is turned on (see Figure 1). The comparator then decides if the DAC output is less than or greater than the signal being converted, and that bit is latched on or off, respectively, before proceeding to the next lower bit and repeating the cycle. When all eight bits have been tested, $\overline{BUSY}$ goes HIGH, signaling a completed conversion.

Under control of the $\overline{RD}$ input, the three-state data outputs (D0-D7) change from high-impedance to presenting the new conversion results to the data bus. Following the data read, $\overline{RD}$ returns HIGH resetting the SAR to 1000 0000 and preparing the ADC for its next conversion.

PIN FUNCTIONS

NOTE: For greater detail on digital input functions, consult Truth Tables and Timing Diagrams.

Pin 1. V_{DD} Power Supply input, +5V.

Pin 2. V_{REF} Voltage Reference input, nominal −10V.

Pin 3. B_{OFS} Bipolar Offset input. +10V input for bipolar mode operation, tie to V_{IN} for unipolar mode operation.

Pin 4. A_{IN} Analog Input. 0V to +10V in unipolar mode, −10V to +10V in bipolar mode.

Pin 14. $\overline{BUSY}$ Conversion status output. BUSY indicates conversion in progress by going LOW at start of conversion and returning HIGH at end of conversion. May be used to interrupt controlling microprocessor or to gate control inputs.

Pin 15. $\overline{RD}$ READ input. Used to read data (on falling edge) and to reset converter (on rising edge).

Pin 16. $\overline{CS}$ Chip Select input. Asserted to allow ADC operation. Starts conversion when converter is in reset condition. Note: Holding $\overline{CS}$ HIGH will not prevent a rising edge on $\overline{RD}$ from resetting the converter.

Pin 17. CLK External clock input/internal clock RC timing input.

APPLICATIONS INFORMATION

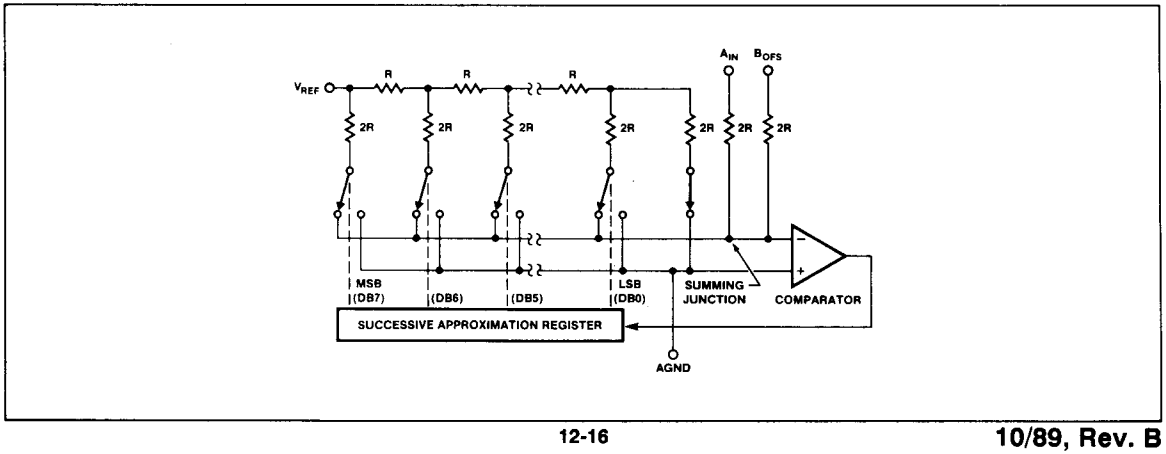
The ADC-908 may be interfaced as if it were a static RAM, a ROM, or a slow-memory device. Each of these interface modes has its own timing and software requirements as described below. These requirements must be rigidly met, as improper timing may cause the ADC-908 to change modes.

HOW TO CHOOSE AN OPERATING MODE

The static-RAM interface mode offers advantages in a tightly controlled hardware and software environment, where the relationship between WRITE and READ instruction pairs is certain. As long as minimum timing is satisfied, converted data may be read at any convenient time after conversion. The use of separate commands to start a conversion, and then read the results, is conceptually easy. However, if the software is subject to uncontrolled modifications, then the paired relationship between WRITE and READ instructions may be lost. Resulting software bugs may result in converted data of unknown age, or altogether invalid data being read.

By contrast, the ROM mode may be more resistant to software bugs. As long as minimum timing is satisfied, each READ instruction obtains new, valid data. However, since the data

FIGURE 1: D/A Converter Used in ADC-908



output at any previous READ instruction is obtained from a conversion performed just after the previous READ instruction, data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, acting as a substitute for the static-RAM mode WRITE command; the second READ gets the results. The advantage of the ROM mode is the use of a single command, rather than the alternating READ-WRITE required by static-RAM mode.

The slow-memory mode is the simplest mode of all. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the slow-memory mode is virtually immune to subsequent software modifications.

OPERATING DESCRIPTION: STATIC-RAM MODE

In this mode, input $\overline{CS}$ is derived from the ADC-908 address decoder, and input $\overline{RD}$ is derived from an active-LOW memory READ signal. (See Figure 2.)

To start a conversion, execute a memory WRITE to the ADC-908. The completed conversion data is obtained by executing a memory READ to the ADC-908. During conversion, output $\overline{BUSY}$ will be LOW. Do not attempt to read data until $\overline{BUSY}$ returns HIGH. The required minimum time between WRITE and READ is usually obtained by including one or more NOP or other program instructions. The use of branch or conditional commands between the WRITE and READ instructions is not recommended due to the possibility of software bugs.

It is important that the WRITE and READ commands be alternately executed. A WRITE instruction has no effect unless the results of the previous WRITE have already been read. Once data has been read, the ADC-908 is internally reset. In other words, two or more READ operations cannot be used in succession, since only the first READ will produce valid data. A new conversion must be started using WRITE, and the conversion must be completed, before a new READ will produce valid data.

TABLE 1: Truth Table, Static RAM Mode

INPUTS $\overline{CS}$	INPUTS $\overline{RD}$	OUTPUTS $\overline{BUSY}$	OUTPUTS DB7-DB0	ADC-908 OPERATION
L	H	H	HIGH-Z	Start Convert (Write Cycle)
L	↓	H	HIGH-Z to DATA	Read Data (Read Cycle)
L	↑	H	DATA to HIGH-Z	Reset Converter
H	X (Note 1)	X	HIGH-Z	No Effect (Not Selected)
L	H	L	HIGH-Z	No Effect (Converter Busy)
L	↓	L	HIGH-Z	No Effect (Converter Busy)
L	↑ (Note 1)	L	HIGH-Z	Conversion Error Not Allowed

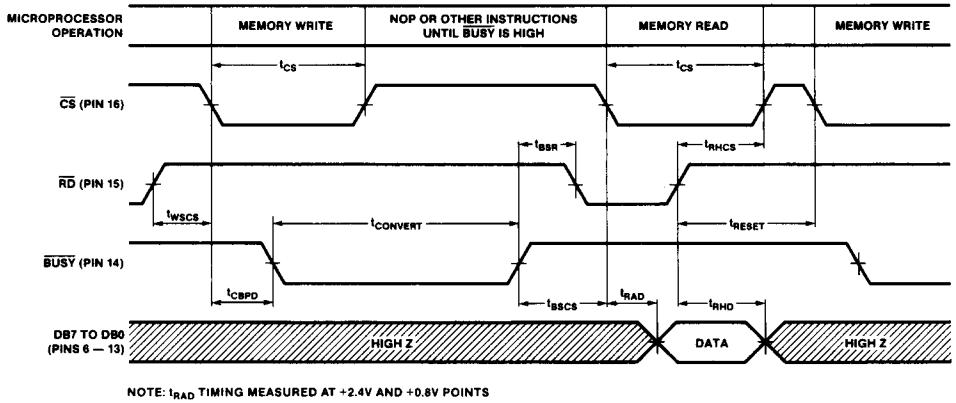
NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

OPERATING DESCRIPTION: ROM MODE

In ROM mode, input $\overline{CS}$ is tied LOW, and input $\overline{RD}$ is derived from the ADC-908 address decoder. To satisfy timing, it is recommended that the decoder be enabled by a system MEMRD (8080), VMA (6800), or similar strobe. (See Figure 3.)

In ROM mode, data is read by executing a READ instruction to the ADC-908 address. At the conclusion of the READ instruction, the ADC-908 automatically resets itself and then proceeds to perform a new data conversion. Output $\overline{BUSY}$ is LOW during conversion. A new READ instruction to the ADC-908 must not be executed until $\overline{BUSY}$ returns HIGH.

FIGURE 2: Static RAM Mode Timing Diagram



This requirement may be met by inserting NOP or other program instructions between consecutive READ operations. Conditional or branch instructions may be used, but keep in mind that data may become out-of-date if excessive time elapses between consecutive READ instructions.

TABLE 2: Truth Table, ROM Mode

INPUTS $\overline{CS}$	INPUTS $\overline{RD}$	OUTPUTS $\overline{BUSY}$	OUTPUTS DB7-DB0	ADC-908 OPERATION
L	↓	H	HIGH-Z to DATA	Read Data
L	↑	↓	DATA to HIGH-Z	Reset and Start New Conversion
L	↓	L	HIGH-Z	No Effect (Converter Busy)
L	↑ (Note 1)	L	HIGH-Z	Conversion Error Not Allowed

NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

OPERATING DESCRIPTION: SLOW-MEMORY MODE

The slow-memory mode is intended for systems in which the ADC-908 $\overline{BUSY}$ output is used as an interrupt to force the microprocessor into WAIT states during data conversion.

In slow-memory mode, inputs $\overline{CS}$ and $\overline{RD}$ are tied together. The common $\overline{RD}$ and $\overline{CS}$ signal is derived from the ADC-908 address decoder. To satisfy the timing requirements, it is advisable to latch the address using ALE (8085) or SYNC (8080). For 8080 or 8085-based systems, connect the microprocessor READY input to the ADC-908 $\overline{BUSY}$ output. (See Figure 4.)

TABLE 3: Truth Table, Slow-Memory Mode

INPUTS $\overline{CS}$ & $\overline{RD}$	OUTPUTS $\overline{BUSY}$	OUTPUTS DB7-DB0	ADC-908 OPERATION
H	H	HIGH-Z	No Effect (Not Selected)
↓	↓	HIGH-Z	Start Conversion
L	L	HIGH-Z	Conversion in Progress. μP in WAIT State
L	↑	HIGH-Z to DATA	Conversion Complete. Read Data
↑	H	DATA to HIGH-Z	Reset and Deselect Converter

FIGURE 3: ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)

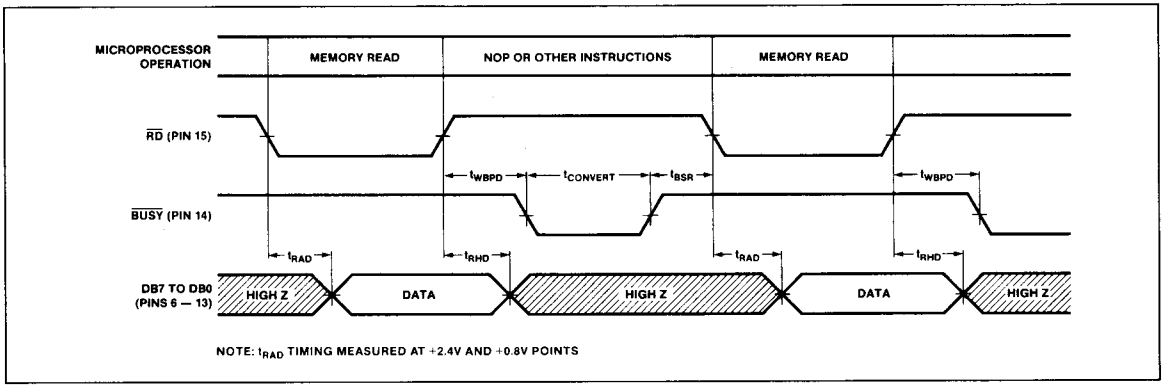
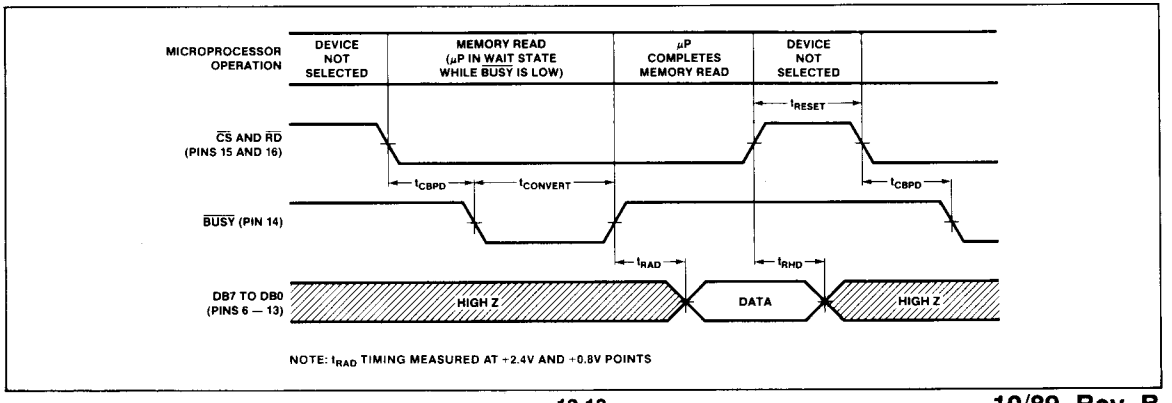


FIGURE 4: Slow-Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)



Do not execute a WRITE instruction at the ADC-908 address when in slow-memory mode, since bus conflicts will arise. In some architectures, an accidental WRITE instruction may be locked out in hardware, by proper strobing of the ADC-908 address decoder.

INITIALIZATION

In all operating modes, the ADC-908 is initialized by executing a READ instruction to the ADC-908 address. The data obtained should be ignored.

CLOCK OSCILLATOR

The ADC-908 may be used with its internal asynchronous clock oscillator. An external resistor and capacitor are required. Typical values are R = 43kΩ and C = 100pF, for conversion times in the 6μs range. For applications in which the fastest conversion times are required, an external clock is recommended. The external clock must be gated by the use of a 74125-type three-state buffer, with an output pullup resistor. Optimum conversion accuracy is obtained when $\overline{CS}$ goes LOW on a positive clock edge. The maximum external clock frequency is 1.35MHz (See Figure 5 and 6.)

REFERENCE VOLTAGE

A negative reference voltage must be applied to the ADC-908 V_{REF} input. Optimum full-scale accuracy is obtained using −10.00V, although V_{REF} may be −5.00V, −10.24V, or other voltages within its specified range.

Over the full temperature range, optimum gain accuracy is obtained when the input to the V_{REF} pin is from a low-impedance source. A resistor or trimmer may be used in series with the V_{REF} pin, but this trim technique is not as accurate as a low-impedance source. (See Figure 7.)

For a cost-effective −10.00V or −10.24V reference with excellent accuracy and low temperature coefficient, ask for PMI's REF-08. Consult your sales representative for availability.

FIGURE 5: Using the Internal Clock Oscillator

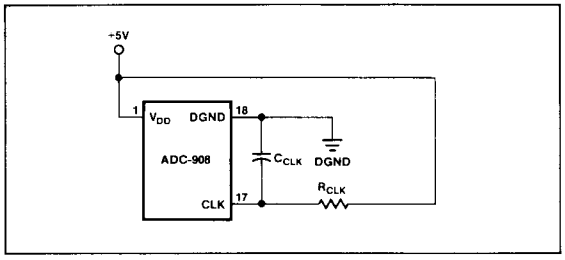


FIGURE 6: Using an External Clock

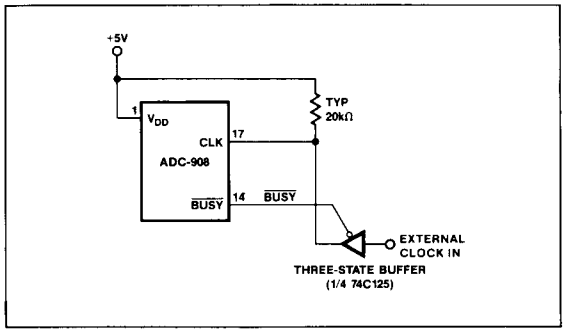
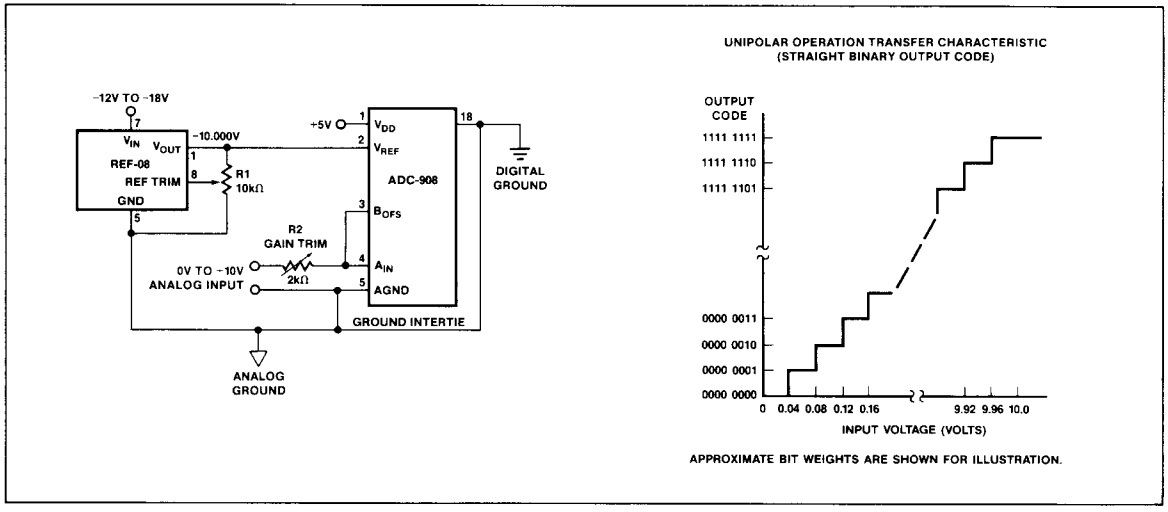


FIGURE 7: Unipolar Operation



ANALOG INPUT VOLTAGE

The ADC-908 unipolar operation is obtained when the analog input voltage is between 0V and $|V_{REF}|$. With the A_{IN} and B_{OFS} pins tied together, input 0V will correspond to code 0000 0000, and input full-scale will correspond to code 1111 1111.

Bipolar operation is obtained by using the B_{OFS} input to offset the A_{IN} input voltage. For example, with $V_{REF} = -10V$, an offset voltage of +10V may be applied to B_{OFS}. The analog signal range will then be −10V to +10V at A_{IN}. Code 0000 0000 will correspond to −10V, and positive full scale will be code 1111 1111. Calibration may be performed using trimmers in series with A_{IN} and B_{OFS}. (See Figure 8).

Another method of obtaining bipolar operation is to use an op-amp with gain = −1/2, to sum the analog signal with the reference voltage. With a −10V reference and −10V to +10V analog signal, the op amp output will then be 0V to +10V. This signal is then treated as an ordinary unipolar input to the ADC-908. With this arrangement, input +10V corresponds to code 0000 0000, and negative full-scale corresponds to code 1111 1111.

UNIPOLAR BINARY OPERATION

Figure 7 shows the analog circuit connections for unipolar operation. The REF-08 supplies the necessary −10V reference input.

Calibration for offset should be made before gain calibration is attempted.

Offset calibration must be performed in the signal conditioning circuitry which drives the A_{IN} input.

To adjust offset:

1) Apply −39.1mV (1 LSB) to the input of the buffer amplifier driving A_{IN}.
2) While performing continuous conversions, adjust the buffer amplifier's offset adjustment potentiometer until DB7 to DB1 are LOW and DB0 (LSB) flickers.

Following offset calibration, full scale gain can be calibrated:

1) Apply −9.961V to the input of the buffer amplifier.
2) While performing continuous conversions, adjust the reference trim pot until DB7 to DB1 are HIGH, and DB0 (LSB) flickers.

BIPOLAR OPERATION

Offset Binary—Figure 8 shows a circuit for offset binary bipolar operation. Offset correction should be made at the buffer amplifier driving A_{IN}. Gain error correction should be accomplished by adjusting V_{REF}.

To calibrate this circuit:

1) Adjust R1 until $V_{REF} = -10.00V$.
2) Adjust R2 and R3 to their mid-points.
3) Apply +10.000V to the input buffer amplifier.
4) While performing continuous conversions, adjust R2 until DB7 to DB1 are LOW and DB0 (LSB) flickers.
5) Ground the input of the input buffer circuit.
6) While performing continuous conversions, adjust R3 until the ADC's output code flickers between 0111 1111 and 1000 0000.
7) Apply −10.000V to the signal input.
8) While performing continuous conversions, adjust R1 until DB7 to DB1 are LOW and the DB0 (LSB) flickers.
9) Apply +9.922V to the signal input.
10) If the ADC output code is not 1111 1110 ±1 bit, repeat the calibration procedure, omitting step 1.

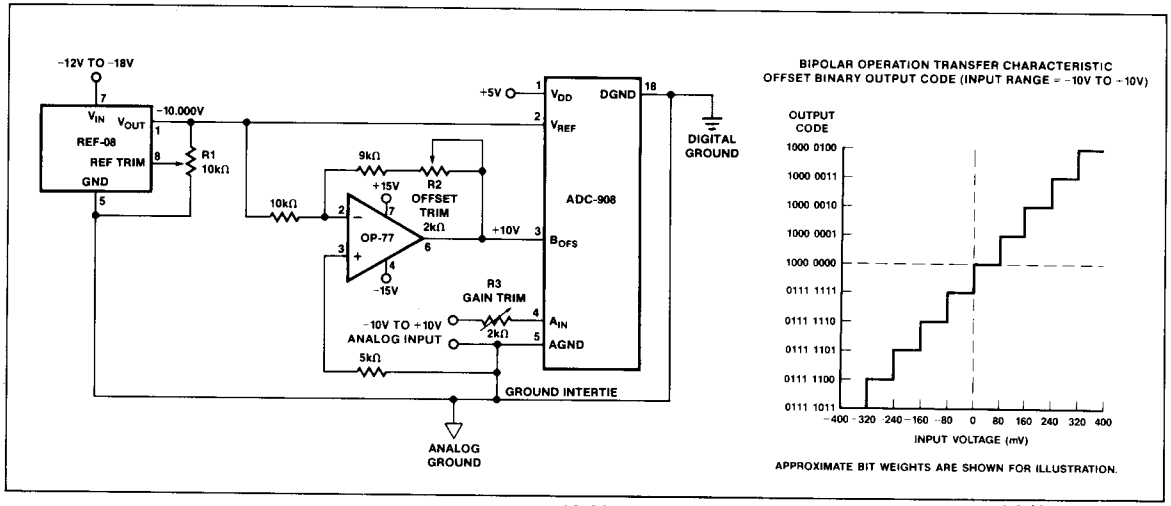
Complementary Offset Binary—Figure 9 shows a complementary offset binary circuit. In this bipolar mode, the +10V to −10V analog input is conditioned to a 0 to +10V signal range for normal unipolar conversion.

In calibrating this circuit, adjust offset before gain.

Offset Adjustment:

1) Adjust R1 until $V_{REF} = -10.000V$.
2) Adjust R3 to its mid-point.
3) Adjust R2 until its tap is at 0V.
4) Ground the analog input.
5) While performing continuous conversions, adjust R2 until the ADC output flickers between 0111 1111 and 1000 0000.

FIGURE 8: Offset Binary Operation



Gain Adjustment:
1) Apply +9.922V across the analog input.
2) While performing continuous conversions, adjust R3 until DB7 to DB1 are HIGH and DB0 (LSB) flickers.

DIGITAL CONSIDERATIONS

Control Timing—Fresh data from a recent conversion must be read before beginning a new conversion. Following the data READ, as $\overline{RD}$ goes HIGH, it resets the SAR and clears the data from the previous conversion.

The timing restrictions detailed in the interface timing diagrams must be observed to prevent the ADC-908 from changing interface modes. For example, if $\overline{CS}$ is held LOW too long while in RAM mode, the converter will change to ROM mode and initiate a new conversion.

Logic Deglitching—Unrelated activity on the address bus may cause unexpected glitch inputs to the ADC. The glitches may cause unwanted READs, resets, or conversions. In ROM or RAM modes, these may be avoided by gating the address decode logic with $\overline{RD}$ or $\overline{WR}$ (8080) or VMA (6800). In slow-memory mode, ALE (8085) or SYNC (8080) may be used to latch the address.

Initialization—Following power-up, the SAR is in an unknown state. Executing a memory READ (disregard the data) will reset the ADC.

ANALOG CONSIDERATIONS

Analog Input Impedances—Low impedance sources must be used to drive the V_{REF}, A_{IN}, and B_{OFS} inputs. Excessive source impedances may cause errors due to the loading effects of the inputs' finite impedances.

Ground Management—AGND and DGND pins should be connected at or near the ADC to minimize noise effects. If the two grounds cannot be connected near the ADC, the grounds should be clamped with back-to-back Schottky diodes between the AGND and DGND pins.

Offset Correction—Conversion offset errors may be corrected by counter-offsetting the buffer amplifier driving A_{IN}. This offset correction may be accomplished by applying a correction current to the buffer's summing junction or by tapping a voltage divider sitting between V_{DD} and V_{REF}, and applying this tap voltage to the noninverting input of the buffer.

Ratiometric Operation—The R-2R type DAC in the ADC-908 permits ratiometric operation of the ADC. Performance degradation may, however, occur as V_{REF} varies from −10.000V. This decrease in performance is due to comparator limitations including offset-voltage, gain, and input noise.

The ADC-908 uses the reference as a power supply for the comparator to increase speed and accuracy. Reference voltages of a magnitude less than −9V must be avoided for accurate comparator operation. For best accuracy, the use of a 0.1μF bypass capacitor from V_{REF}(Pin 2 to AGND) is recommended.

Power Supply Bypassing—For best accuracy, V_{DD} (Pin 1) should be bypassed to AGND with a 0.1μF capacitor.

FIGURE 9: Complementary Offset Bipolar Operation