

2N7012, 2N7013

N-Channel Enhancement Mode Transistors

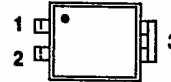
T-39-05

4-PIN DIP
(Similar to TO-250)

TOP VIEW

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
2N7012	60	0.35	1.2
2N7013	40	0.35	1.2



- 1 GATE
- 2 SOURCE
- 3 DRAIN

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS
		2N7012	2N7013	
Drain-Source Voltage	V_{DS}	60	40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current	I_D	$T_A = 25^\circ\text{C}$	1.2	A
		$T_A = 100^\circ\text{C}$	0.80	
Pulsed Drain Current ¹	I_{DM}	10	10	
Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	1.0	W
		$T_A = 100^\circ\text{C}$	0.4	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$
Lead Temperature ($1/16"$ from case for 10 sec.)	T_L	300		

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	R_{thJA}		120	K/W

¹Pulse width limited by maximum junction temperature.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS		UNIT
				MIN	MAX	
STATIC						
Drain-Source Breakdown Voltage	2N7012 2N7013	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$		60 40	V
Gate Threshold Voltage		$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1000\ \mu\text{A}$		2.0	4.0
Gate-Body Leakage		I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100
Zero Gate Voltage Drain Current		I_{DSS}	$V_{DS} = V_{(BR)DSS}, V_{GS} = 0\text{ V}$			250
			$V_{DS} = 0.8 \times V_{(BR)DSS}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			
On-State Drain Current ¹		$I_{D(ON)}$	$V_{DS} = 2\text{ V}, V_{GS} = 10\text{ V}$		1.2	A
Drain-Source On-State Resistance ¹		$r_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$	0.3		0.35
			$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}, T_J = 125^\circ\text{C}$	0.55		0.64
Forward Transconductance ¹		g_{fs}	$V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}$	1.5	1.2	S
DYNAMIC						
Input Capacitance		C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	220		300
Output Capacitance		C_{oss}		120		200
Reverse Transfer Capacitance		C_{rss}		30		100
Total Gate Charge ²		Q_g	$V_{DS} = 0.8 \times V_{(BR)DSS}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	4.8		6.0
Gate-Source Charge ²		Q_{gs}		1		
Gate-Drain Charge ²		Q_{gd}		2		
Turn-On Delay Time ²		$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 25\ \Omega$ $I_D \approx 1.2\text{ A}, V_{GEN} = 10\text{ V}, R_G = 25\ \Omega$	7		20
Rise Time ²		t_r		13		30
Turn-Off Delay Time ²		$t_{d(off)}$		18		30
Fall Time ²		t_f		13		25
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_A = 25^\circ\text{C}$)						
Continuous Current		I_S			1.2	A
Pulsed Current ³		I_{SM}			10	
Forward Voltage ¹		V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$		1.6	V
Reverse Recovery Time		t_{rr}	$I_F = I_S, dI_F/dt = 100\text{ A}/\mu\text{s}$	45		ns
Reverse Recovery Charge		Q_{rr}		0.6		μC

¹Pulse test: Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

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Figure 1. Output Characteristics

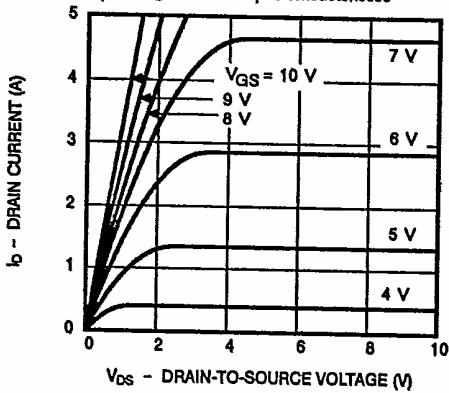


Figure 2. Transfer Characteristics

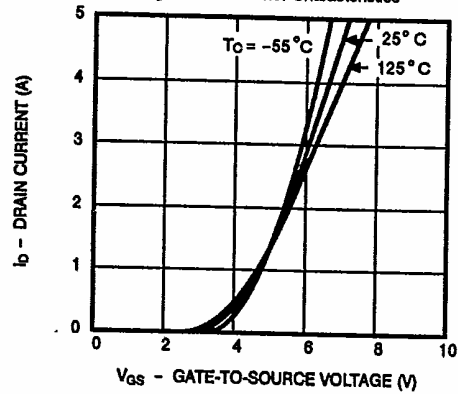


Figure 3. Transconductance

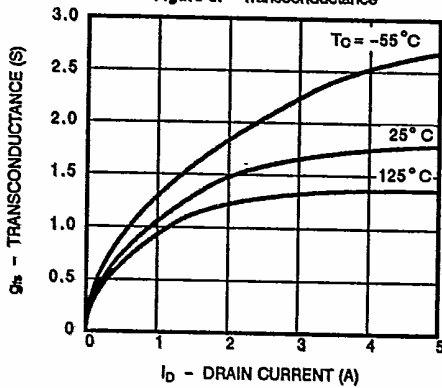
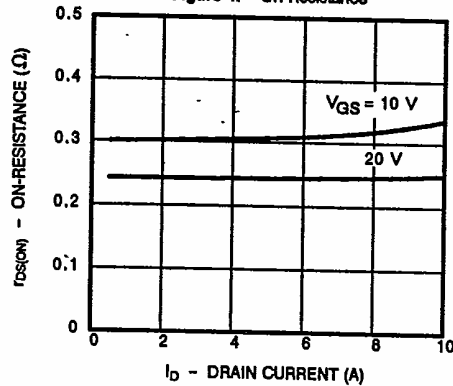


Figure 4. On-Resistance



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Figure 5. Capacitance

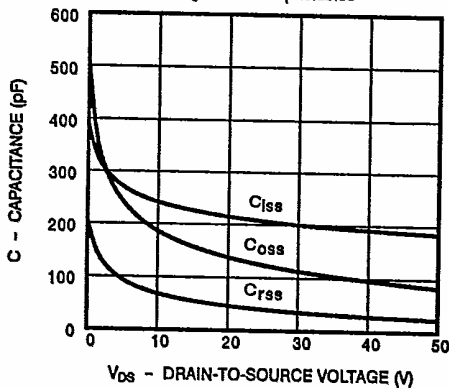


Figure 6. Gate Charge

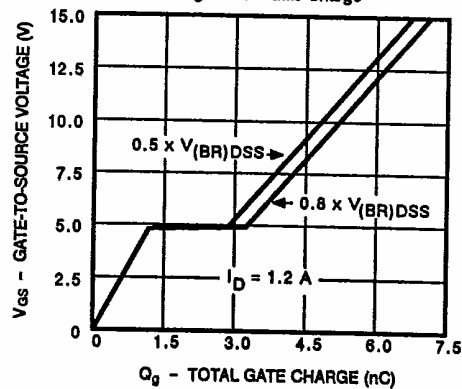


Figure 7. On-Resistance vs. Junction Temperature

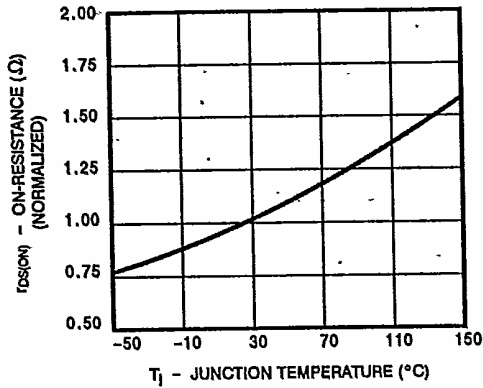
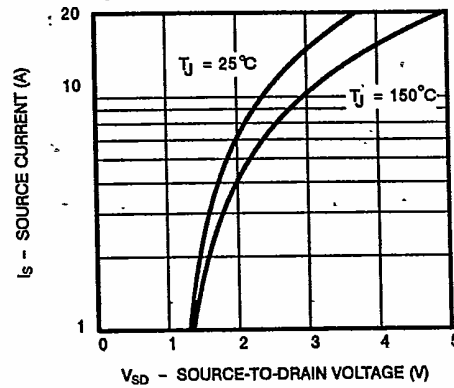


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Drain Current vs. Ambient Temperature

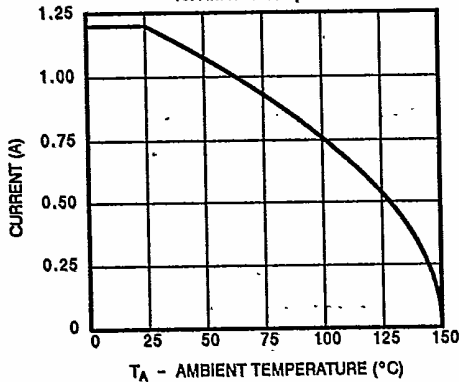


Figure 10. Safe Operating Area

