

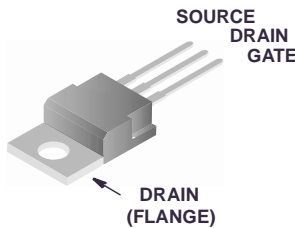
**71A, 60V, 0.014 Ohm, N-Channel, Logic Level UltraFET® Power MOSFET**



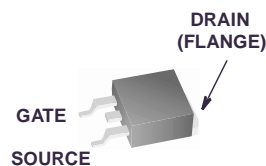
**Packaging**

JEDEC TO-220AB

JEDEC TO-263AB

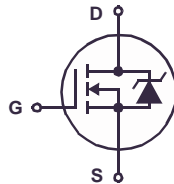


HUFA76439P3



HUFA76439S3S

**Symbol**



**Features**

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.012\Omega$ ,  $V_{GS} = 10V$
  - $r_{DS(ON)} = 0.014\Omega$ ,  $V_{GS} = 5V$
- Simulation Models
  - Temperature Compensated PSpice® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - [www.fairchildsemi.com](http://www.fairchildsemi.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs  $R_{GS}$  Curves

**Ordering Information**

PART NUMBER	PACKAGE	BRAND
HUFA76439P3	TO-220AB	76439P
HUFA76439S3S	TO-263AB	76439S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUFA76439S3ST.

**Absolute Maximum Ratings**  $T_C = 25^\circ C$ , Unless Otherwise Specified

	HUFA76439P3, HUFA76439S3S	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	60 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	60 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 16$ V
Drain Current		
Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 5V$ ) . . . . .	$I_D$	71 A
Continuous ( $T_C = 25^\circ C$ , $V_{GS} = 10V$ ) (Figure 2) . . . . .	$I_D$	75 A
Continuous ( $T_C = 100^\circ C$ , $V_{GS} = 5V$ ) . . . . .	$I_D$	50 A
Continuous ( $T_C = 100^\circ C$ , $V_{GS} = 4.5V$ ) (Figure 2) . . . . .	$I_D$	48 A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4
Pulsed Avalanche Rating . . . . .	UIS	Figures 6, 17, 18
Power Dissipation . . . . .	$P_D$	155 W
Derate Above $25^\circ C$ . . . . .		1.04 W/ $^\circ C$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 175 $^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300 $^\circ C$
Package Body for 10s, See Techbrief TB334. . . . .	$T_{pkg}$	260 $^\circ C$

NOTES:

1.  $T_J = 25^\circ C$  to  $150^\circ C$ .

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

# HUFA76439P3, HUFA76439S3S

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OFF STATE SPECIFICATIONS</b>							
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 12)	60	-	-	V	
		$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ , $T_C = -40^\circ\text{C}$ (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 55\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{V}$	-	-	$\pm 100$	nA	
<b>ON STATE SPECIFICATIONS</b>							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 11)	1	-	3	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 75\text{A}$ , $V_{GS} = 10\text{V}$ (Figures 9, 10)	-	0.010	0.012	$\Omega$	
		$I_D = 71\text{A}$ , $V_{GS} = 5\text{V}$ (Figure 9)	-	0.0117	0.014	$\Omega$	
		$I_D = 68\text{A}$ , $V_{GS} = 4.5\text{V}$ (Figure 9)	-	0.0125	0.015	$\Omega$	
<b>THERMAL SPECIFICATIONS</b>							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220AB and TO-263AB	-	-	0.96	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^\circ\text{C/W}$	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 4.5\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}$ , $I_D = 50\text{A}$ $V_{GS} = 4.5\text{V}$ , $R_{GS} = 3.9\Omega$ (Figures 15, 21, 22)	-	-	470	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	16	-	ns	
Rise Time	$t_r$		-	300	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	29	-	ns	
Fall Time	$t_f$		-	105	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	200	ns	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 10\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}$ , $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GS} = 3.9\Omega$ (Figures 16, 21, 22)	-	-	205	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	11	-	ns	
Rise Time	$t_r$		-	125	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	45	-	ns	
Fall Time	$t_f$		-	125	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	255	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 30\text{V}$ , $I_D = 50\text{A}$ , $I_{g(REF)} = 1.0\text{mA}$ (Figures 14, 19, 20)	-	70	84	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V to } 5\text{V}$		-	38	45	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V to } 1\text{V}$		-	2.5	3	nC
Gate to Source Gate Charge	$Q_{gs}$			-	8	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$			-	19	-	nC
<b>CAPACITANCE SPECIFICATIONS</b>							
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 13)	-	2745	-	pF	
Output Capacitance	$C_{OSS}$		-	840	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	145	-	pF	

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 54\text{A}$	-	-	1.25	V
		$I_{SD} = 27\text{A}$	-	-	1.00	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 54\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	72	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 54\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	140	nC

Typical Performance Curves

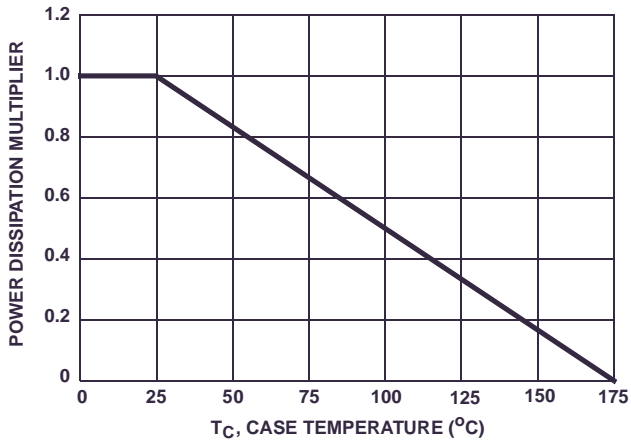


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

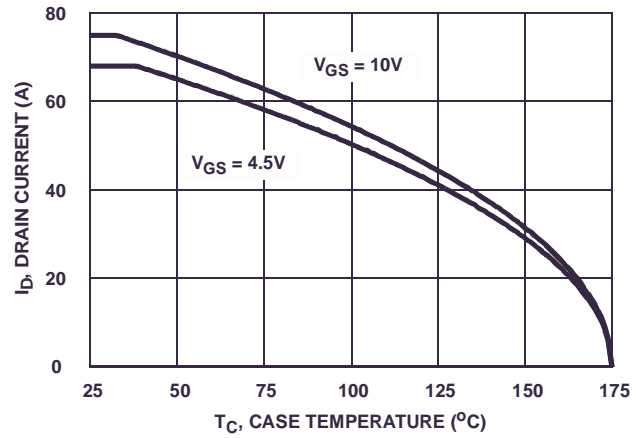


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

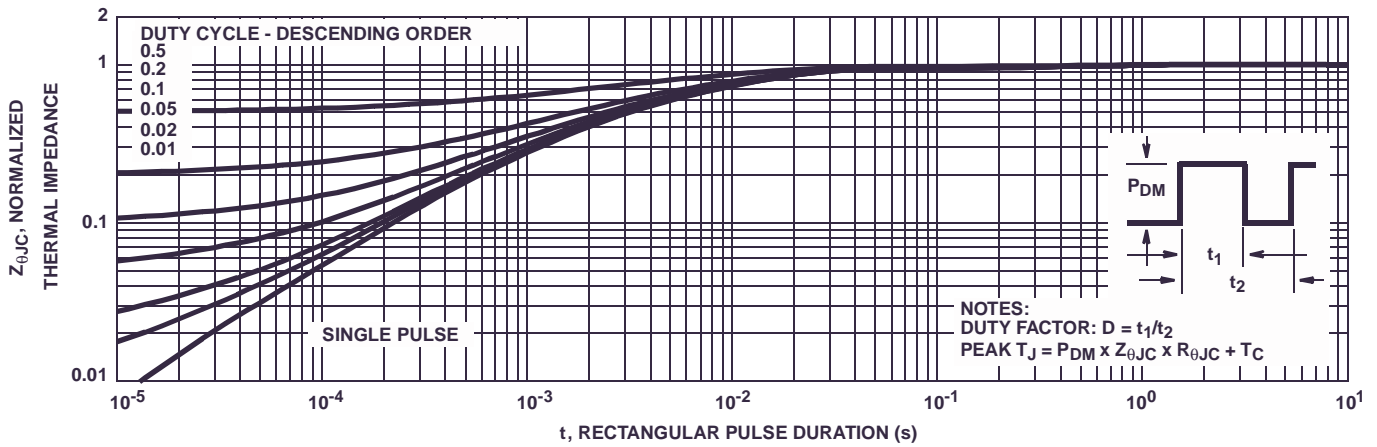


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

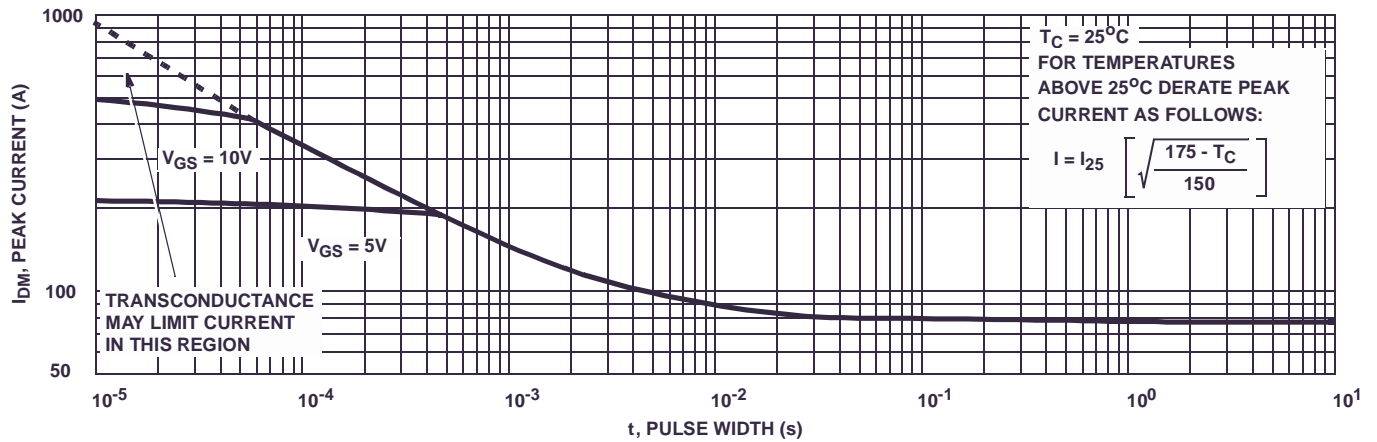


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

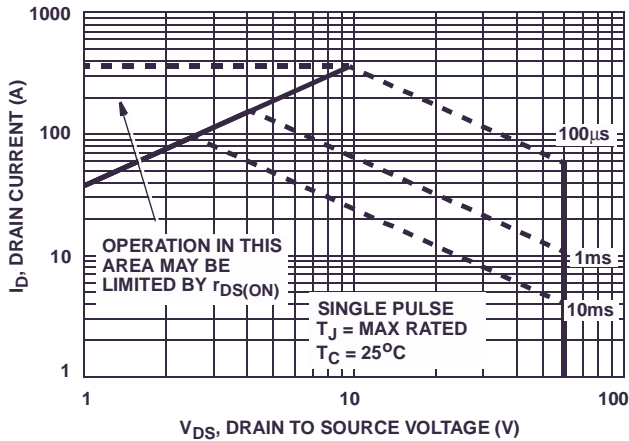
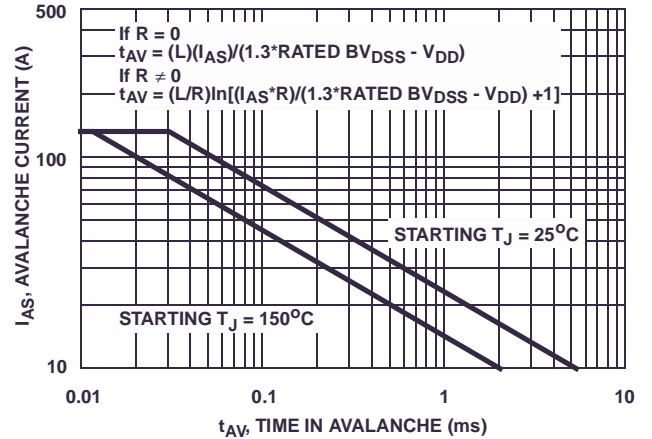


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

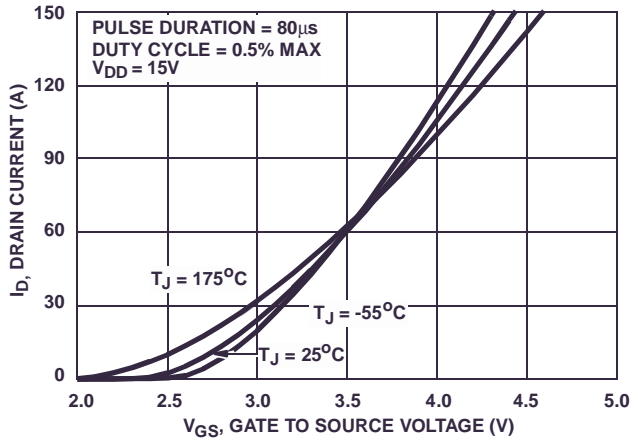


FIGURE 7. TRANSFER CHARACTERISTICS

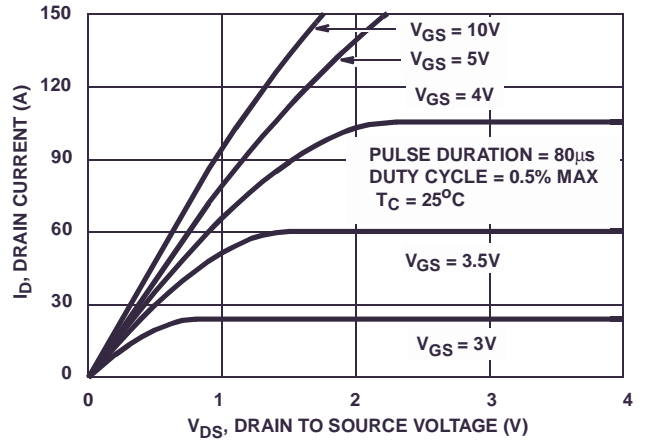


FIGURE 8. SATURATION CHARACTERISTICS

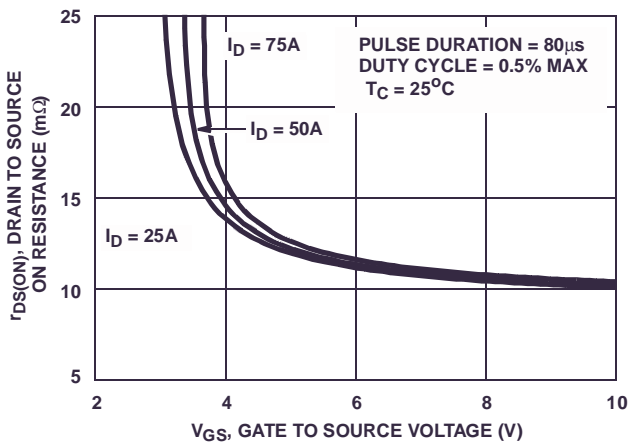


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

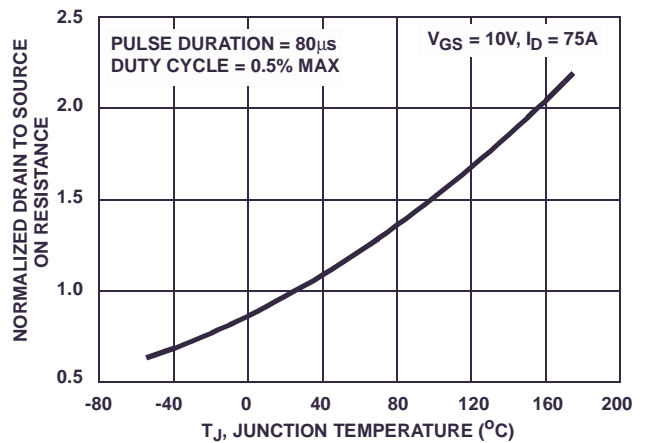


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

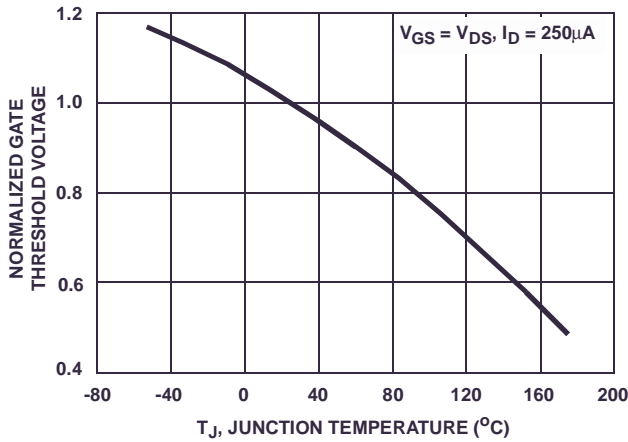


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

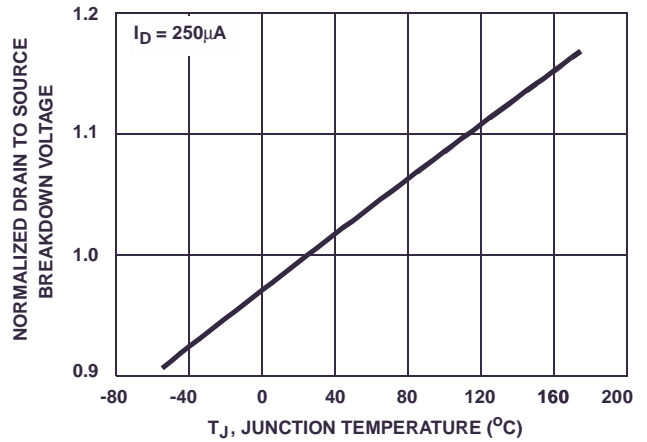


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

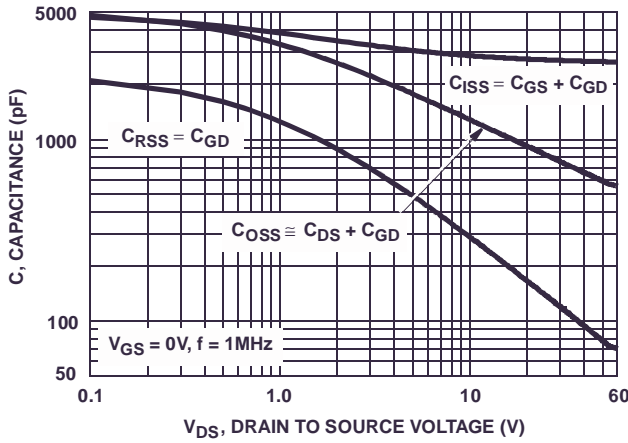
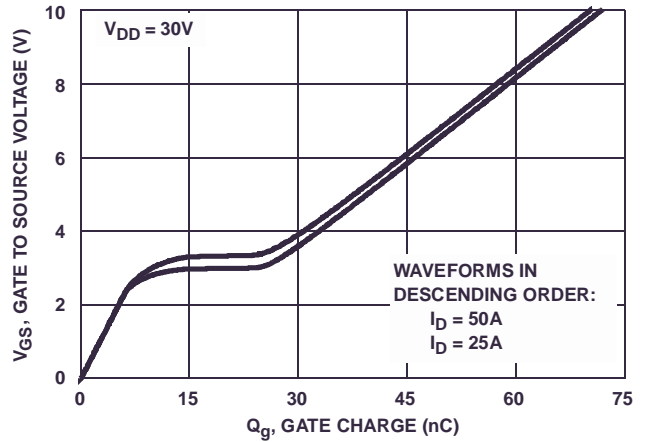


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

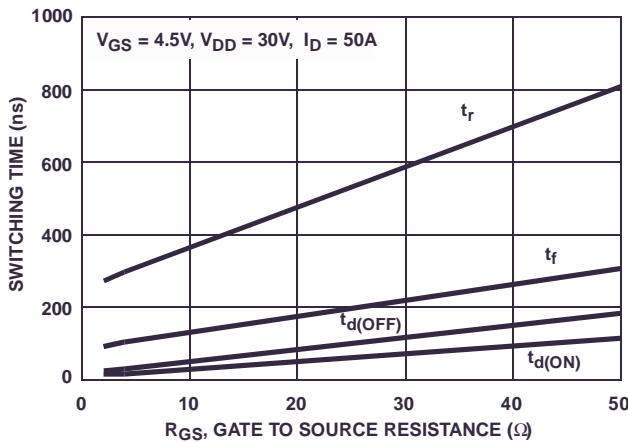


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

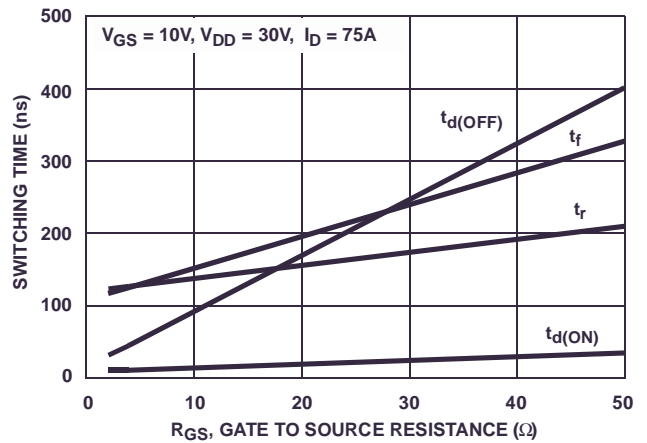


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

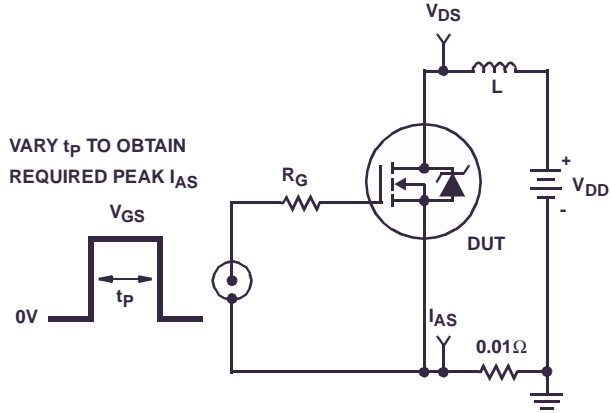


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

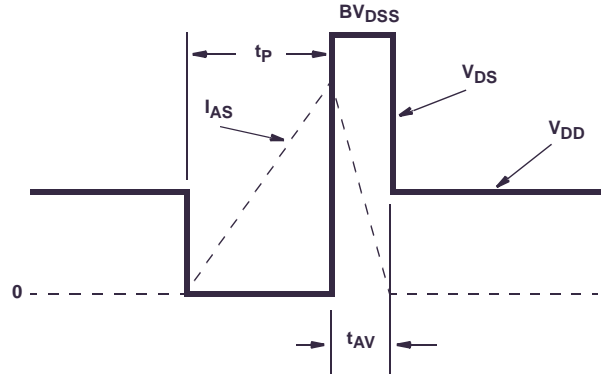


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

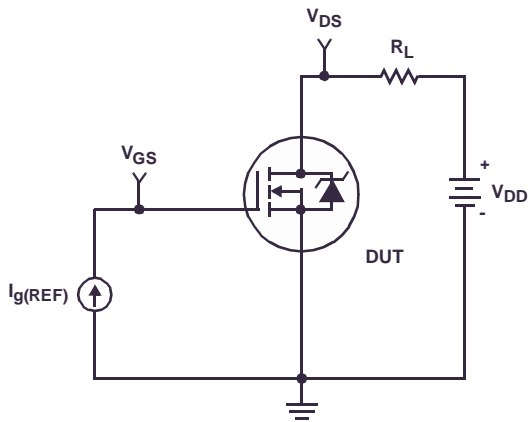


FIGURE 19. GATE CHARGE TEST CIRCUIT

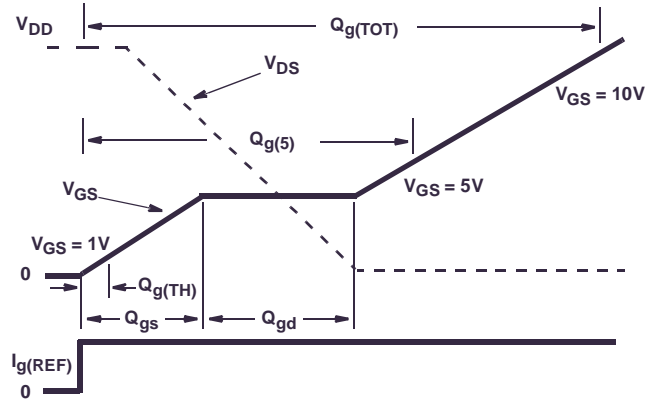


FIGURE 20. GATE CHARGE WAVEFORMS

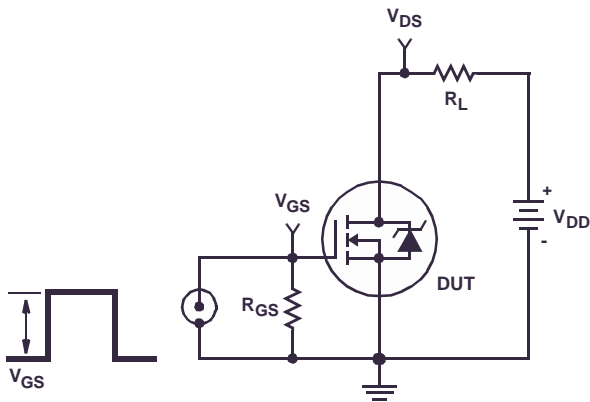


FIGURE 21. SWITCHING TIME TEST CIRCUIT

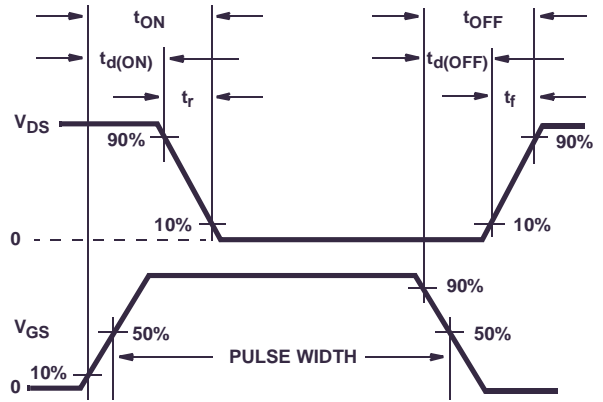


FIGURE 22. SWITCHING TIME WAVEFORM

**PSPICE Electrical Model**

.SUBCKT HUFA76439 2 1 3 ; rev 17 June 1999

CA 12 8 3.70e-9  
 CB 15 14 3.80e-9  
 CIN 6 8 2.60e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.25  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9  
 LGATE 1 9 5.17e-9  
 LSOURCE 3 7 2.33e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 4.72e-3  
 RGATE 9 20 0.88  
 RLDRAIN 2 5 10  
 RLGATE 1 9 51.7  
 RLSOURCE 3 7 23.3  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 4.43e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

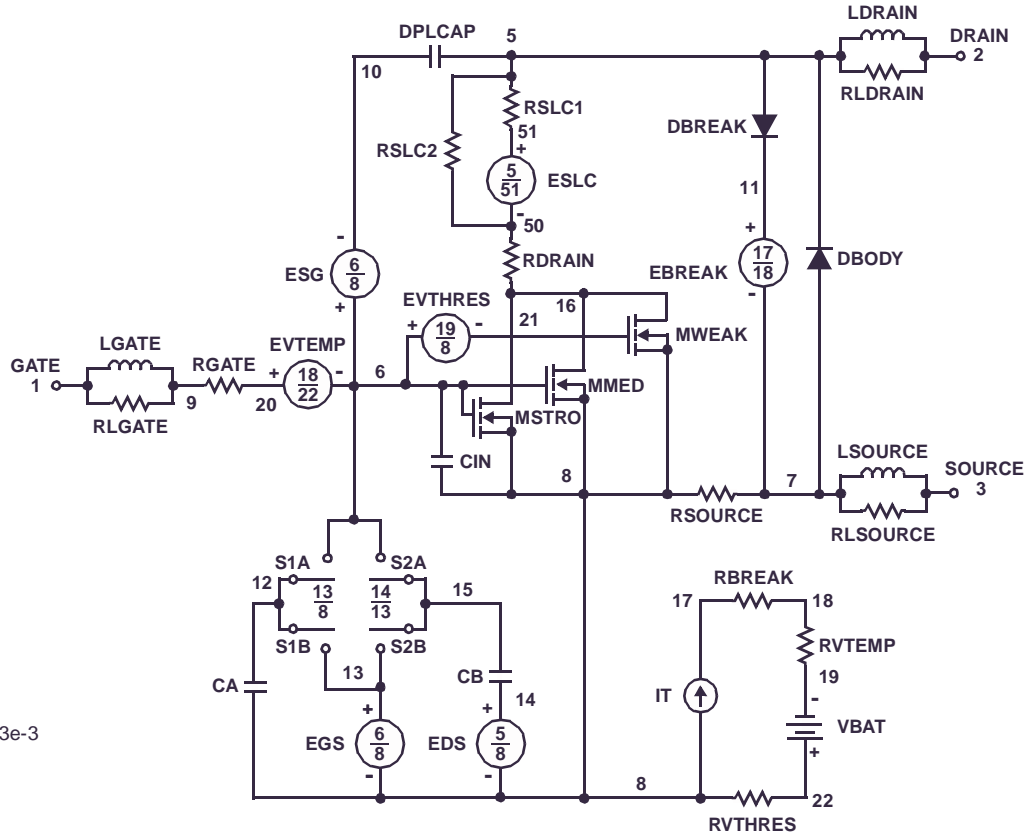
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*225),3.5))}

.MODEL DBODYMOD D (IS = 2.52e-12 RS = 3.53e-3 TRS1 = 1.79e-3 TRS2 = 1.27e-6 CJO = 2.82e-9 TT = 4.90e-8 M = 0.43)  
 .MODEL DBREAKMOD D (RS = 1.95e-1 TRS1 = 9.01e-4 TRS2 = 2.07e-6)  
 .MODEL DPLCAPMOD D (CJO = 2.28e-9 IS = 1e-30 M = 0.85)  
 .MODEL MMEDMOD NMOS (VTO = 1.88 KP = 2.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.88)  
 .MODEL MSTROMOD NMOS (VTO = 2.31 KP = 137 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 1.65 KP = 0.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.8 RS = 0.1)  
 .MODEL RBREAKMOD RES (TC1 = 1.19e-3 TC2 = -1.91e-7)  
 .MODEL RDRAINMOD RES (TC1 = 1.15e-2 TC2 = 3.07e-5)  
 .MODEL RSLCMOD RES (TC1 = 9.92e-4 TC2 = 1.23e-6)  
 .MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)  
 .MODEL RVTHRESMOD RES (TC1 = -2.65e-3 TC2 = -7.94e-6)  
 .MODEL RVTEMPMOD RES (TC1 = -1.39e-3 TC2 = -2.13e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF = -2.5)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.5 VOFF = -6.0)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF = 0.0)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.0 VOFF = -0.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



**SABER Electrical Model**

REV 17 June 1999

template ta76445 n2,n1,n3  
electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 2.52e-12, cjo = 2.82e-9, tt = 4.90e-8, m = 0.43)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 2.28e-9, is = 1e-30, m = 0.85 )
m..model mmedmod = (type=_n, vto = 1.88, kp = 2.1, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.31, kp = 137, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.65, kp = 0.05, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -6, voff = -2.5)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.5, voff = -6)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0, voff = -0.5)
```

```
c.ca n12 n8 = 3.70e-9
c.cb n15 n14 = 3.80e-9
c.cin n6 n8 = 2.60e-9
```

```
d.body n7 n71 = model=dbodymod
d.break n72 n11 = model=dbreakmod
d.plcap n10 n5 = model=dplcapmod
```

```
i.it n8 n17 = 1
```

```
l.drain n2 n5 = 1e-9
l.gate n1 n9 = 5.17e-9
l.source n3 n7 = 2.33e-9
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

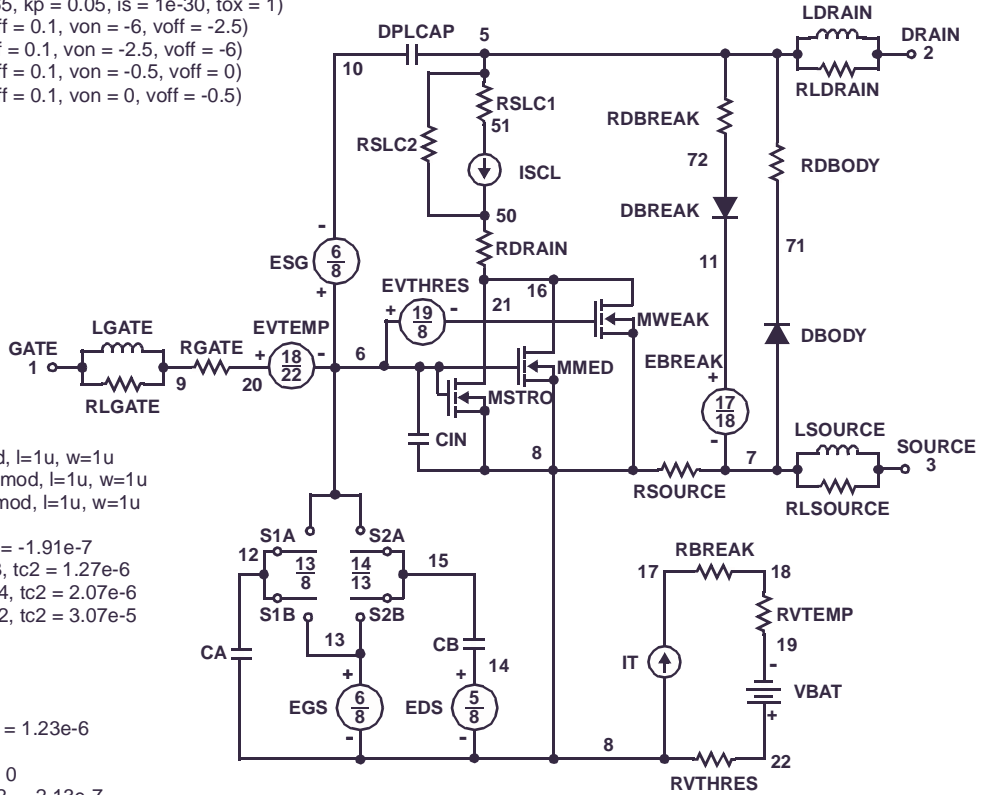
```
res.rbreak n17 n18 = 1, tc1 = 1.19e-3, tc2 = -1.91e-7
res.rbody n71 n5 = 3.53e-3, tc1 = 1.79e-3, tc2 = 1.27e-6
res.rdbreak n72 n5 = 1.95e-1, tc1 = 9.01e-4, tc2 = 2.07e-6
res.rdrain n50 n16 = 4.72e-3, tc1 = 1.15e-2, tc2 = 3.07e-5
res.rgate n9 n20 = 0.88
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 51.7
res.rlsource n3 n7 = 23.3
res.rslc1 n5 n51 = 1e-6, tc1 = 9.92e-4, tc2 = 1.23e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 4.43e-3, tc1 = 0, tc2 = 0
res.rvtemp n18 n19 = 1, tc1 = -1.39e-3, tc2 = -2.13e-7
res.rvthres n22 n8 = 1, tc1 = -2.65e-3, tc2 = -7.94e-6
```

```
spe.ebreak n11 n7 n17 n18 = 66.25
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/225)** 3.5))
}
}
```





**SPICE Thermal Model**

REV 23 June 1999

HUFA76439T

CTHERM1 th 6 3.00e-3  
 CHERM2 6 5 1.90e-2  
 CHERM3 5 4 6.95e-3  
 CHERM4 4 3 7.00e-3  
 CHERM5 3 2 2.95e-2  
 CHERM6 2 tl 12.55

RHERM1 th 6 6.32e-3  
 RHERM2 6 5 1.57e-2  
 RHERM3 5 4 4.43e-2  
 RHERM4 4 3 2.49e-1  
 RHERM5 3 2 3.75e-1  
 RHERM6 2 tl 4.98e-2

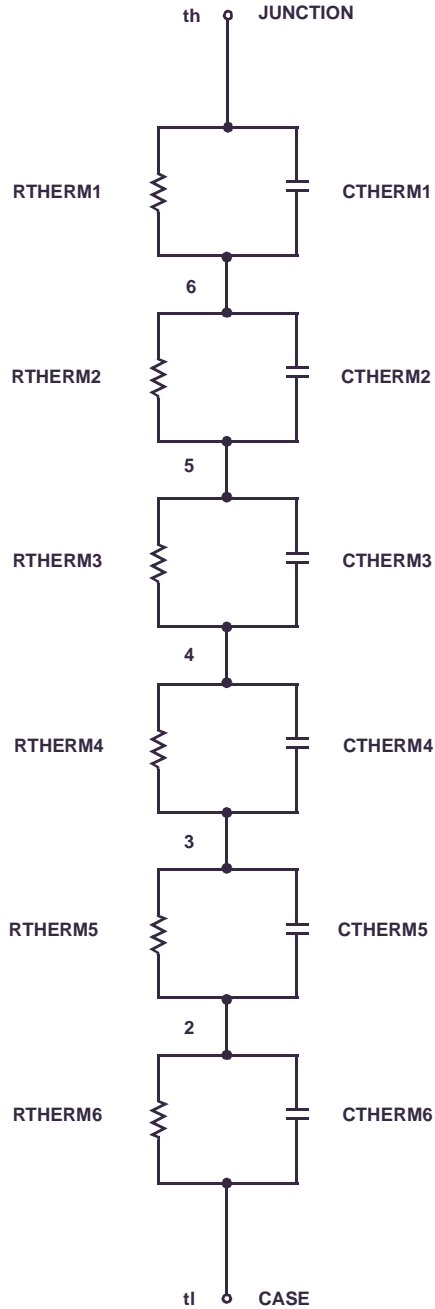
**SABER Thermal Model**

SABER thermal model HUFA76445T

```

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 3.00e-3
ctherm.ctherm2 6 5 = 1.90e-2
ctherm.ctherm3 5 4 = 6.95e-3
ctherm.ctherm4 4 3 = 7.00e-3
ctherm.ctherm5 3 2 = 2.95e-2
ctherm.ctherm6 2 tl = 12.55

rtherm.rtherm1 th 6 = 6.32e-3
rtherm.rtherm2 6 5 = 1.57e-2
rtherm.rtherm3 5 4 = 4.43e-2
rtherm.rtherm4 4 3 = 2.49e-1
rtherm.rtherm5 3 2 = 3.75e-1
rtherm.rtherm6 2 tl = 4.98e-2
}
    
```



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Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E <sup>2</sup> CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	µC™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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