

## SPICE Device Model SiE806DF Vishay Siliconix

## N-Channel 30-V (D-S) MOSFET

#### **CHARACTERISTICS**

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

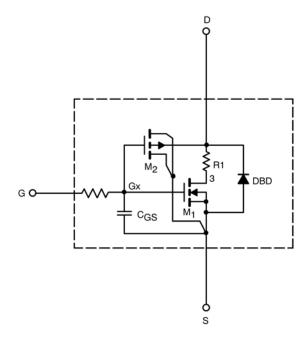
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### **DESCRIPTION**

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to  $125^{\circ}$ C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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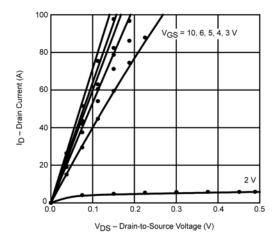
SPECIFICATIONS (T <sub>J</sub> = 25°C UN	NLESS OTHER	WISE NOTED)			
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					•
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.1		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS}~\geq 5~V,~V_{GS}$ = 10 $V$	3290		Α
Drain-Source On-State Resistance <sup>a</sup>	_	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A	0.0014	0.0015	Ω
	r <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 25 \text{ A}$	0.0017	0.0017	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A	180	130	S
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 10 A	0.83	0.90	V
Dynamic <sup>b</sup>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	9401	13000	pF
Output Capacitance	C <sub>oss</sub>		1096	1150	
Reverse Transfer Capacitance	$C_{rss}$		385	550	
Total Gate Charge	$Q_g$	$V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_{D}$ = 20 A	174	165	nC
		$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 20 A	83	75	
Gate-Source Charge	$Q_{gs}$		23	23	
Gate-Drain Charge	$Q_{gd}$		9.5	9.5	

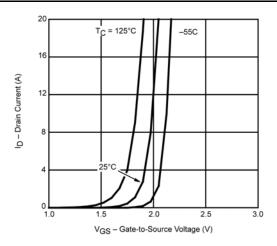
a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2\%.$  b. Guaranteed by design, not subject to production testing.

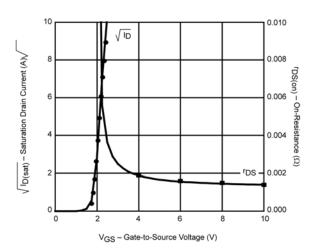


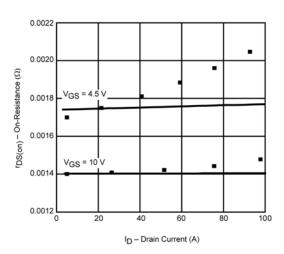
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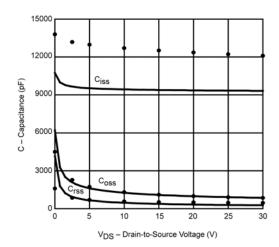
### COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

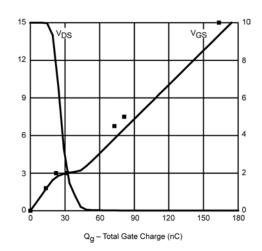












Note: Dots and squares represent measured data.