

Advanced Power MOSFET

SSF6N80A

FEATURES

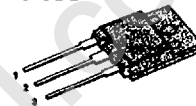
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 μ A (Max.) @ $V_{DS} = 800V$
- Low $R_{DS(ON)}$: 1.472 Ω (Typ.)

$$BV_{DSS} = 800 V$$

$$R_{DS(on)} = 2.0 \Omega$$

$$I_D = 4.5 A$$

TO-3PF



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	800	V
I_D	Continuous Drain Current ($T_c=25^\circ C$)	4.5	A
	Continuous Drain Current ($T_c=100^\circ C$)	2.8	
I_{DM}	Drain Current-Pulsed ①	24	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	486	mJ
I_{AR}	Avalanche Current ③	4.5	A
E_{AR}	Repetitive Avalanche Energy ④	9	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	2.0	V/ns
P_D	Total Power Dissipation ($T_c=25^\circ C$)	90	W
	Linear Derating Factor	0.72	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.39	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	—	40	



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Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV _{DSS}	Drain-Source Breakdown Voltage	800	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV/ΔT _J	Breakdown Voltage Temp. Coeff.	--	0.93	--	V/°C	I _D =250μA <i>See Fig 7</i>
V _{GS(th)}	Gate Threshold Voltage	2.0	--	3.5	V	V _{DS} =5V, I _D =250μA
I _{GSS}	Gate-Source Leakage, Forward	--	--	100	nA	V _{GS} =30V
	Gate-Source Leakage, Reverse	--	--	-100		V _{GS} =-30V
I _{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V _{DS} =800V
		--	--	250		V _{DS} =640V, T _C =125°C
R _{DS(on)}	Static Drain-Source On-State Resistance	--	--	2.0	Ω	V _{GS} =10V, I _D =0.85A ④*
g _{fs}	Forward Transconductance	--	3.87	--	Ω	V _{DS} =50V, I _D =0.85A ④
C _{iss}	Input Capacitance	--	1500	1950	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz <i>See Fig 5</i>
C _{oss}	Output Capacitance	--	140	165		
C _{rss}	Reverse Transfer Capacitance	--	57	66		
t _{d(on)}	Turn-On Delay Time	--	23	55	ns	V _{DD} =400V, I _D =2A, R _G =16Ω <i>See Fig 13</i> ④ ⑤
t _r	Rise Time	--	40	90		
t _{d(off)}	Turn-Off Delay Time	--	92	195		
t _f	Fall Time	--	34	80		
Q _g	Total Gate Charge	--	67	88	nC	V _{DS} =640V, V _{GS} =10V, I _D =2A <i>See Fig 6 & Fig 12</i> ④ ⑤
Q _{gs}	Gate-Source Charge	--	11.2	--		
Q _{gd}	Gate-Drain(Filler) Charge	--	29.6	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I _S	Continuous Source Current	--	--	4.5	A	Integral reverse pn-diode in the MOSFET
I _{SM}	Pulsed-Source Current ①	--	--	24		
V _{SD}	Diode Forward Voltage ④	--	--	1.4	V	T _J =25°C, I _S =--A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	520	--	ns	T _J =25°C, I _F =--A
Q _{rr}	Reverse Recovery Charge	--	6.66	--	μC	di _F /dt=100A/μs ④

Notes :

- Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- L=45mH, I_{AS}=4.5A, V_{DD}=50V, R_G=27Ω, Starting T_J=25°C
- I_{SD} ≤ 7A, di/dt ≤ 150A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C
- Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%
- Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

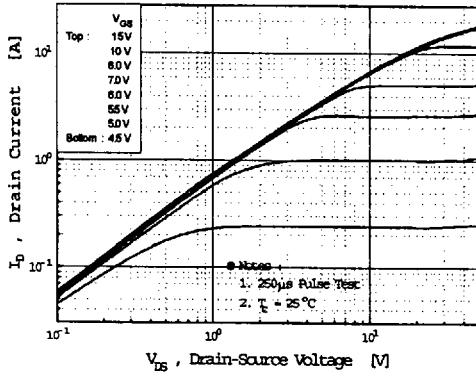


Fig 2. Transfer Characteristics

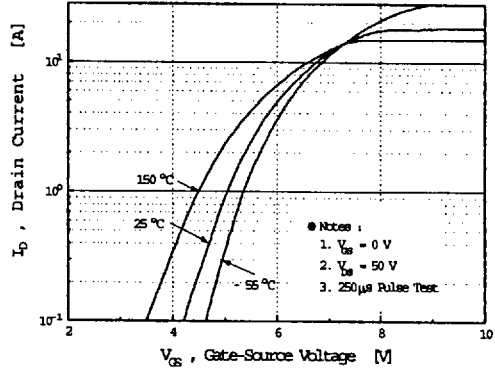


Fig 3. On-Resistance vs. Drain Current

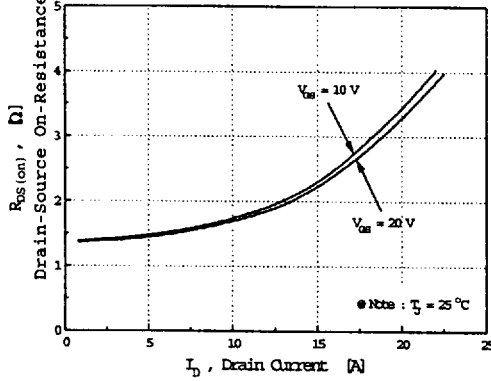


Fig 4. Source-Drain Diode Forward Voltage

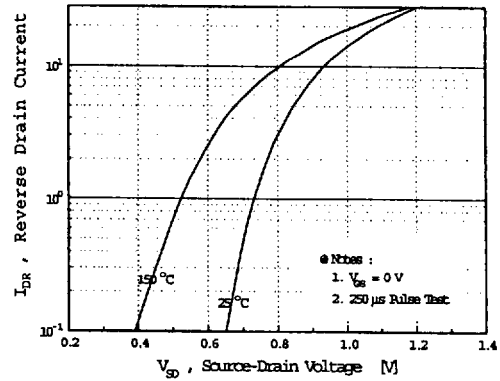


Fig 5. Capacitance vs. Drain-Source Voltage

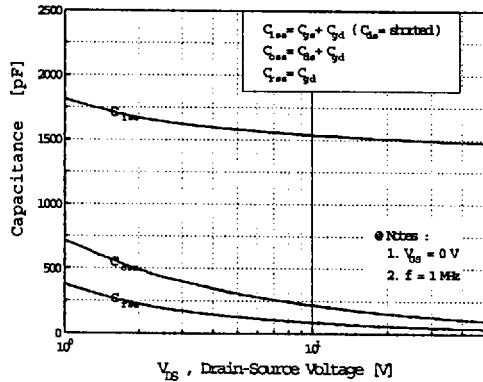
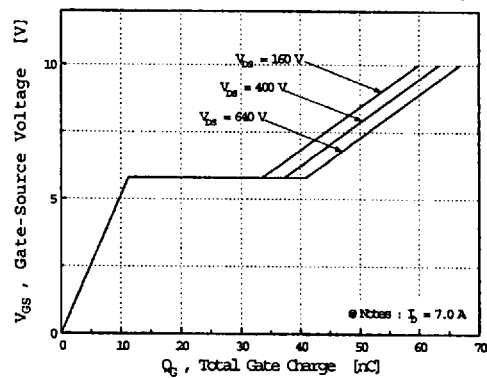


Fig 6. Gate Charge vs. Gate-Source Voltage



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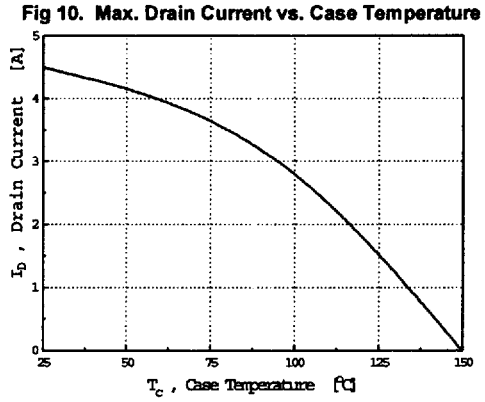
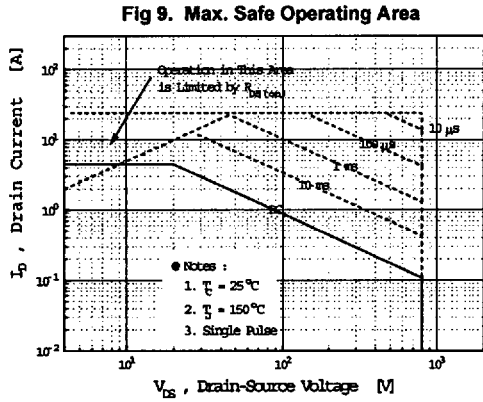
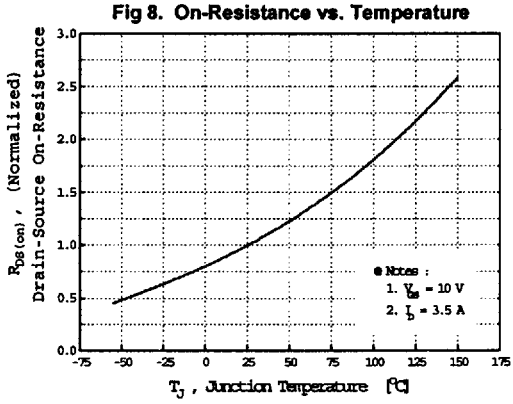
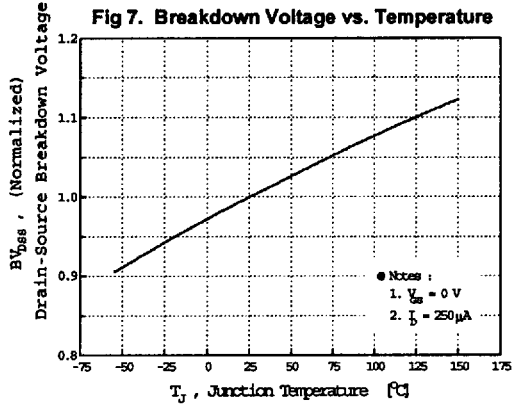


Fig 11. Thermal Response

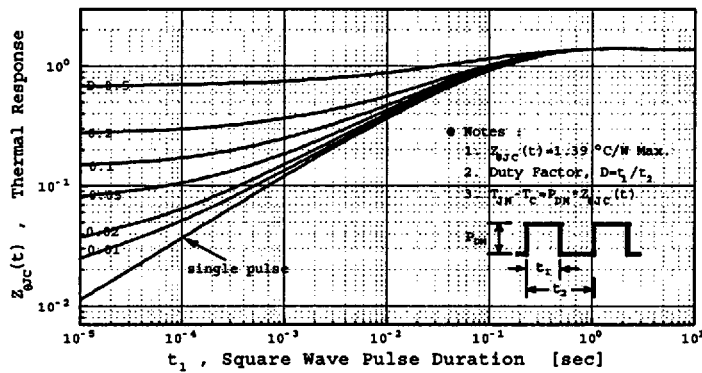


Fig 12. Gate Charge Test Circuit & Waveform

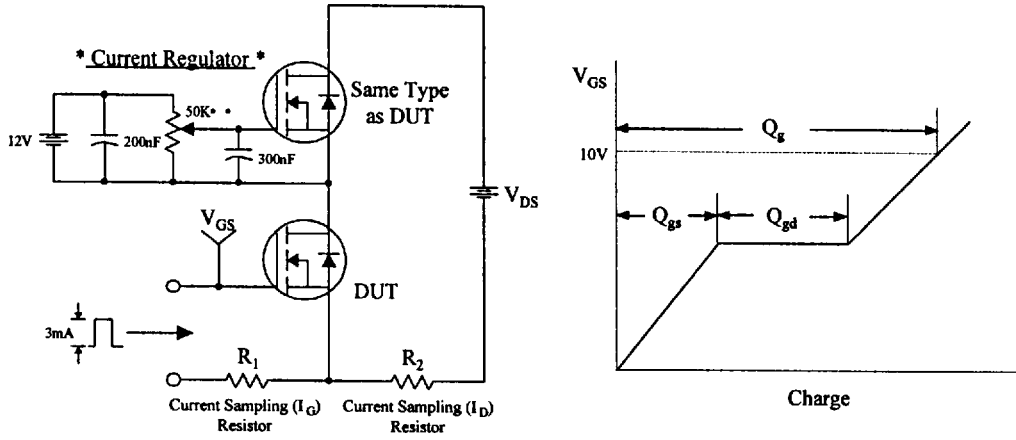


Fig 13. Resistive Switching Test Circuit & Waveforms

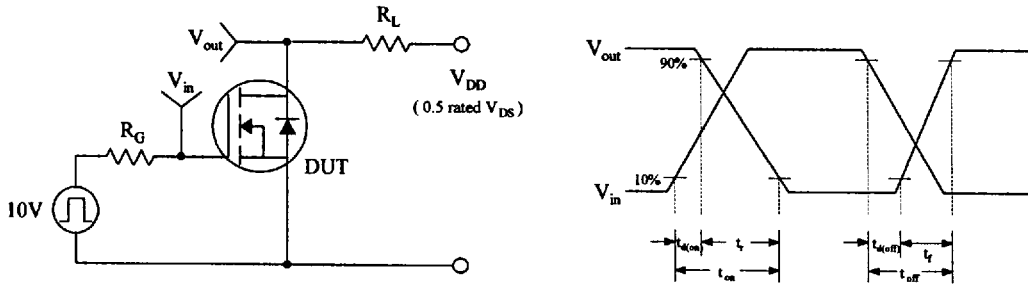


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

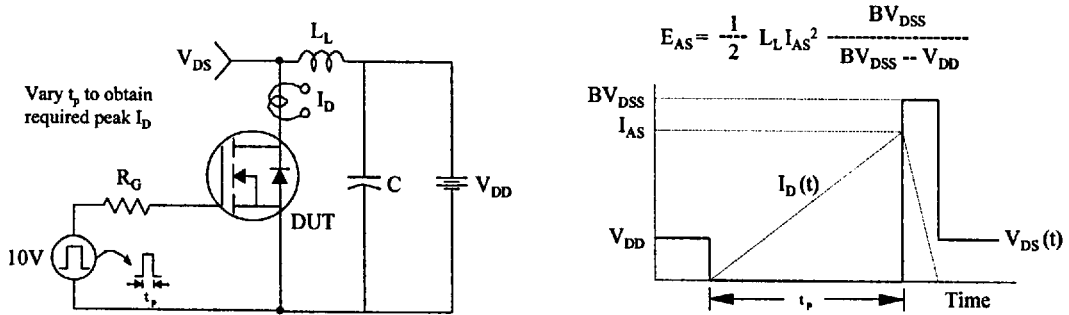
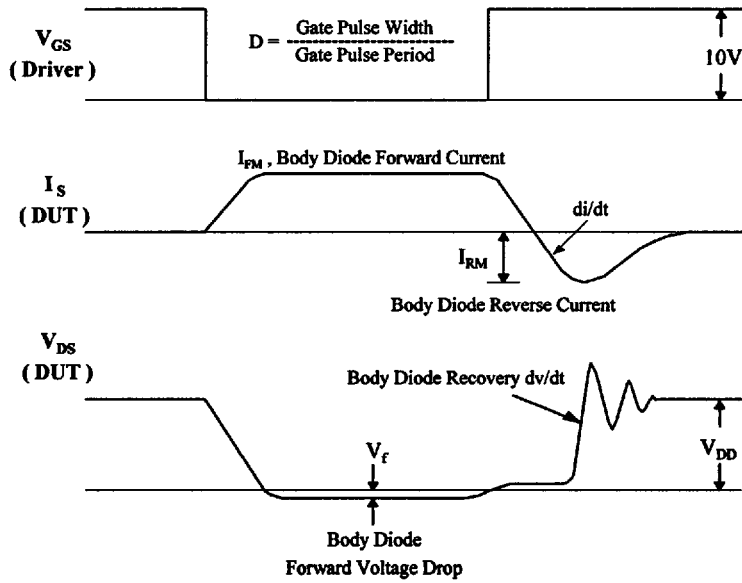
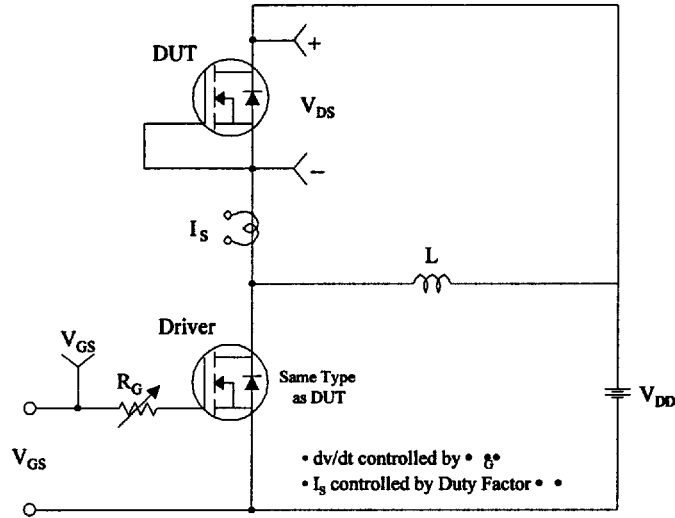
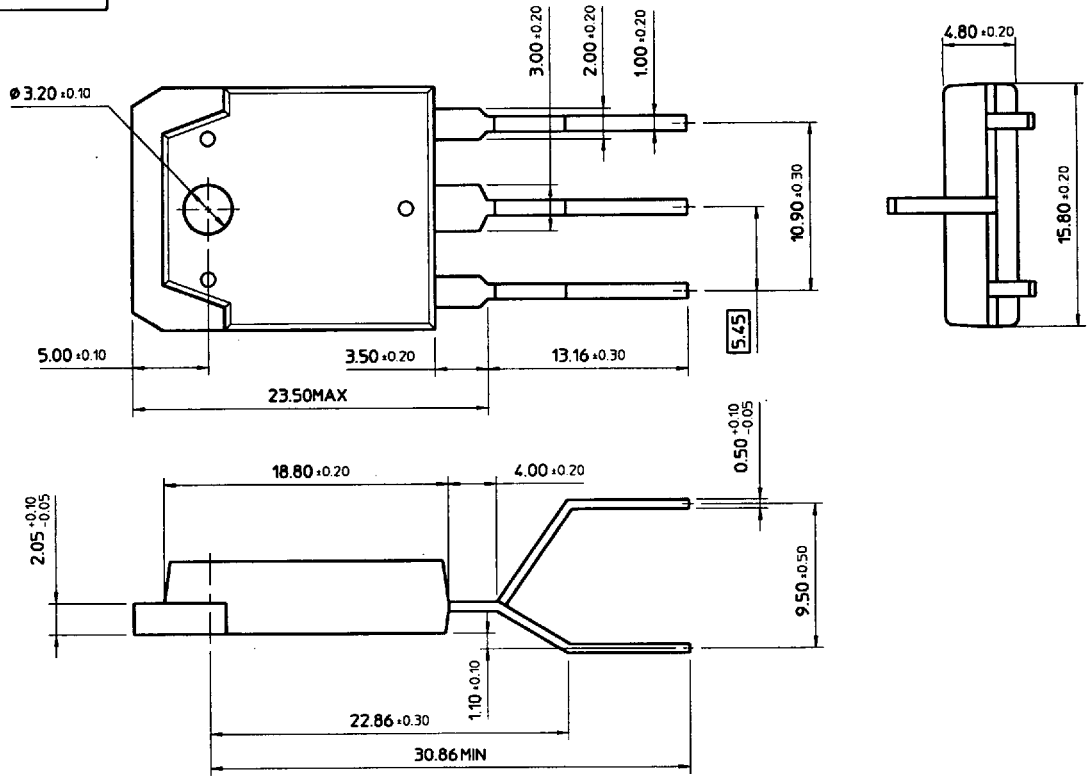


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

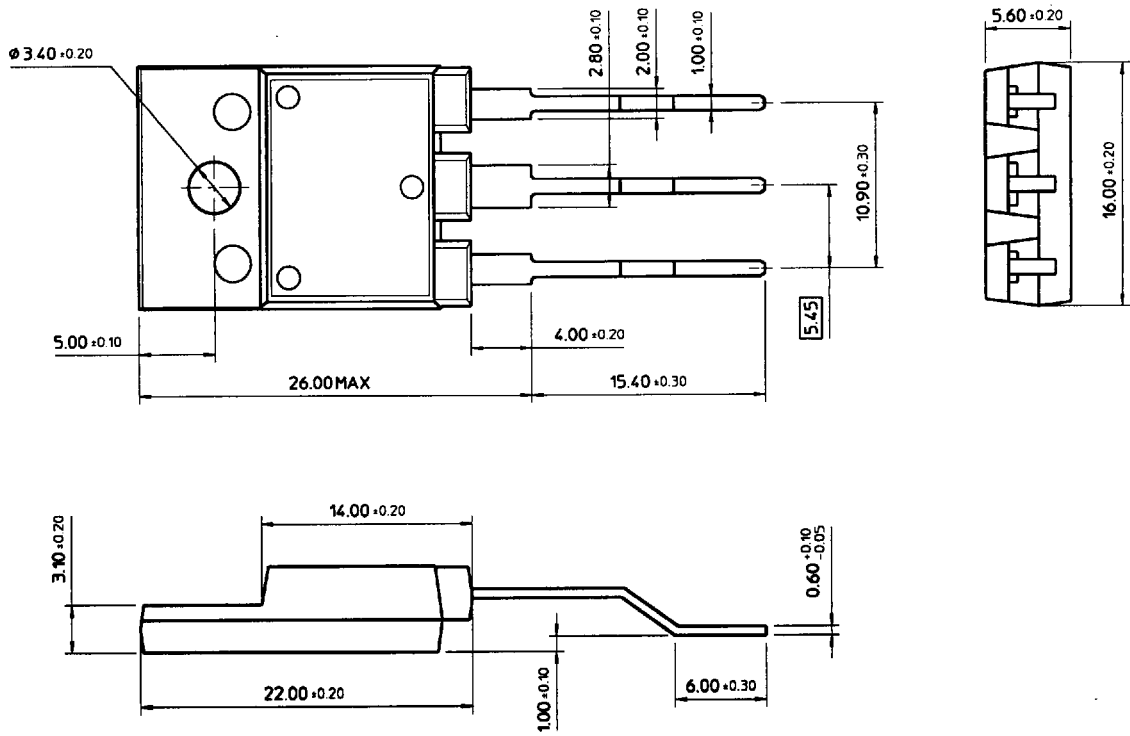


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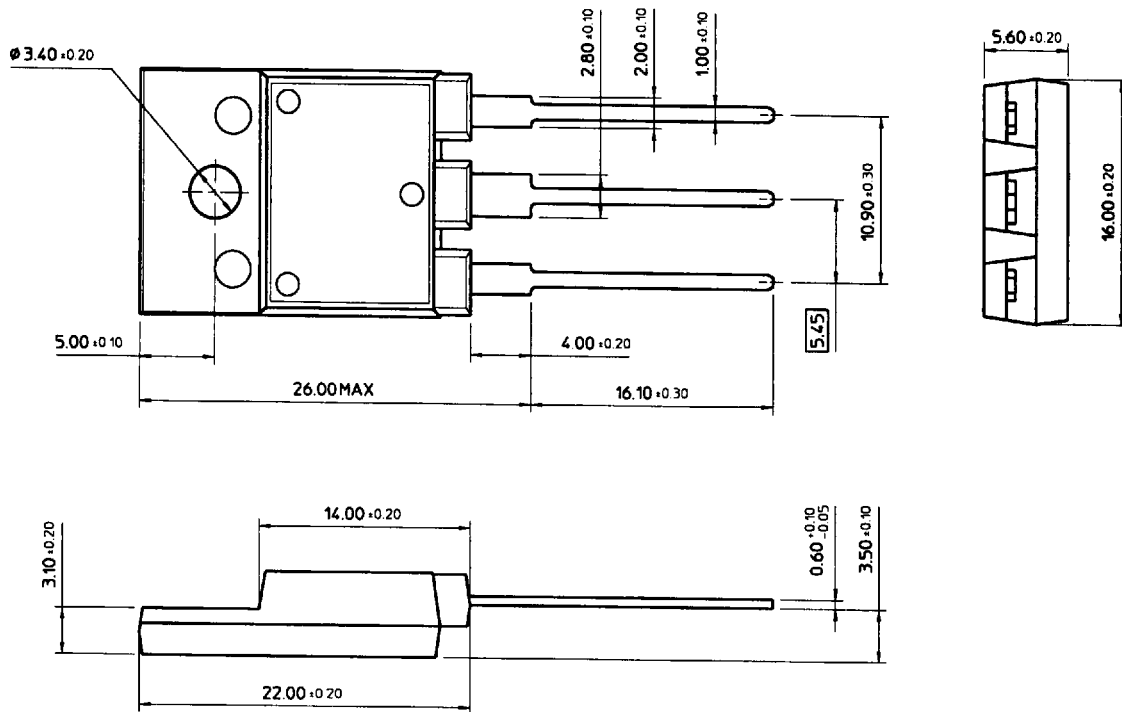
T0-3P (2)



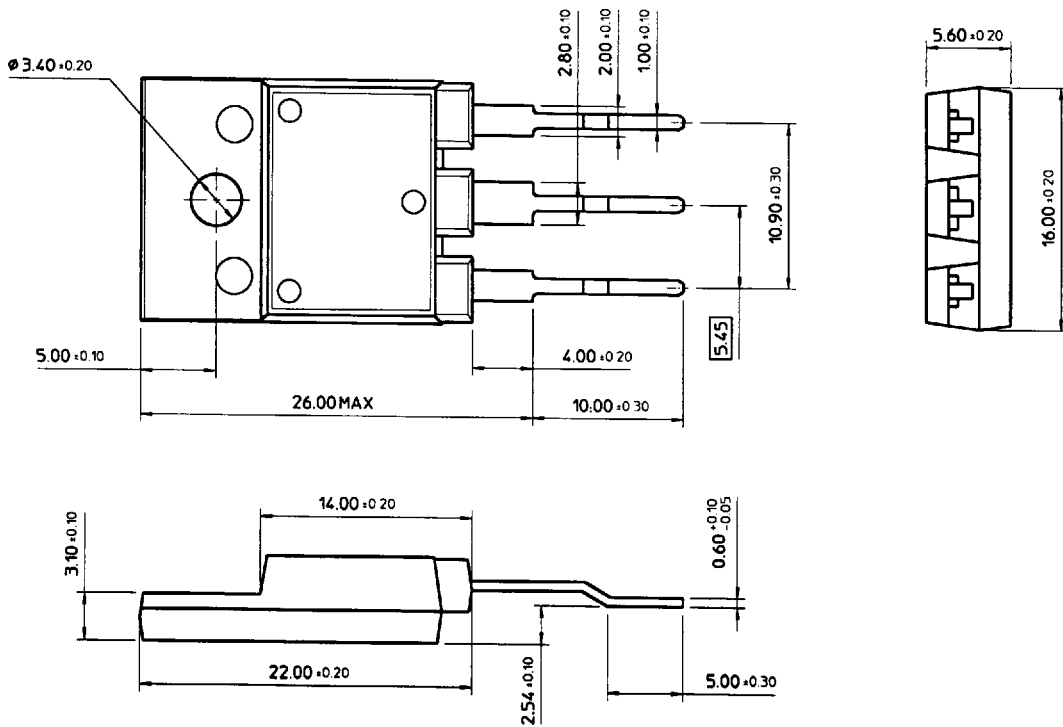
T0-3PF (1)



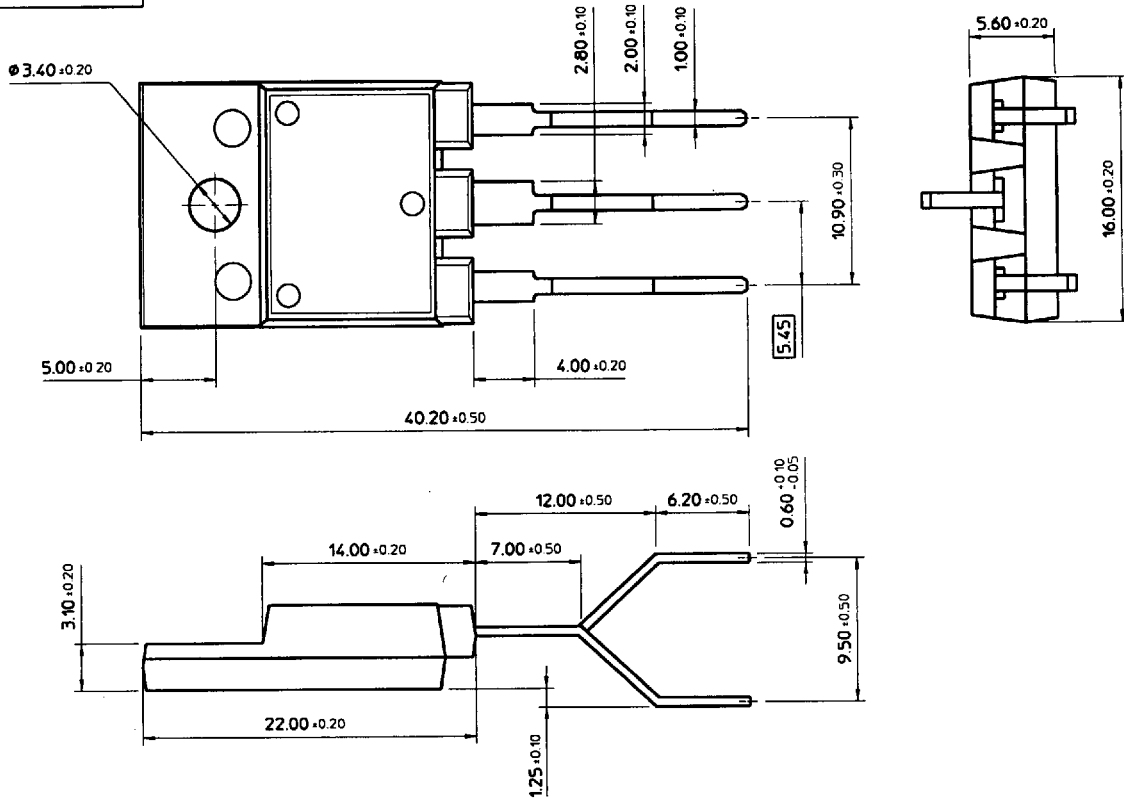
TO-3PF (2)



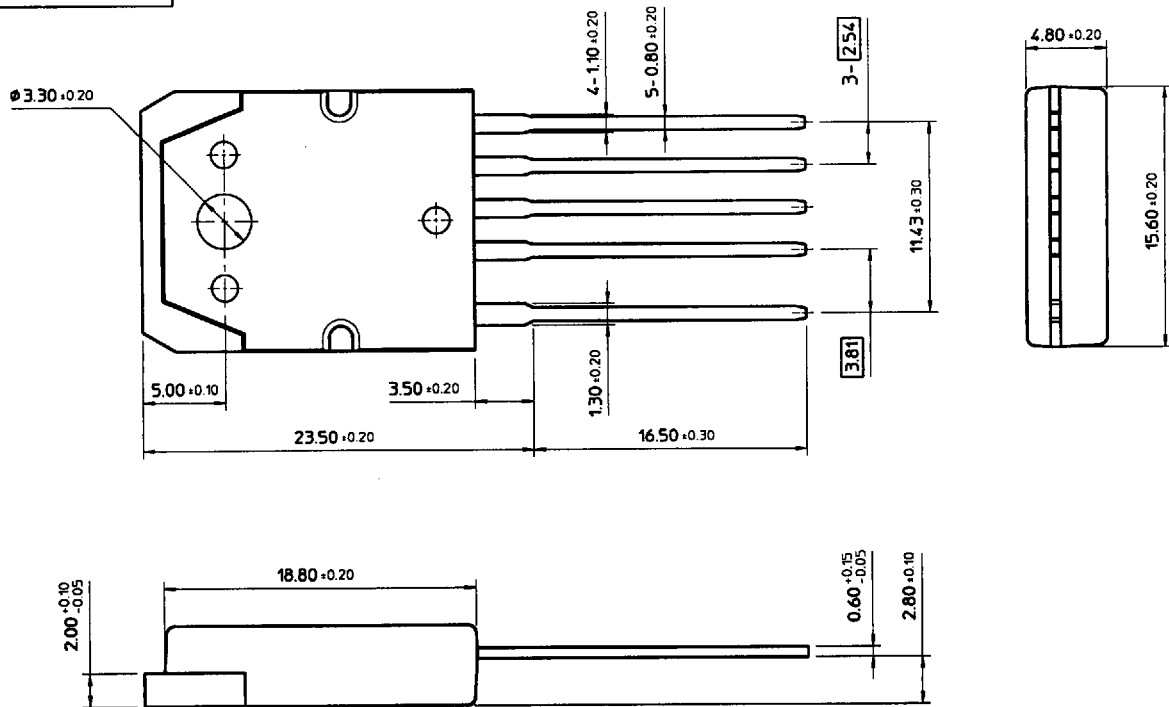
TO-3PF (3)



TO-3PF (4)



TO-3P-5L



Under Development