

## ECL SJ-2830 Series

Rev. G

### Description

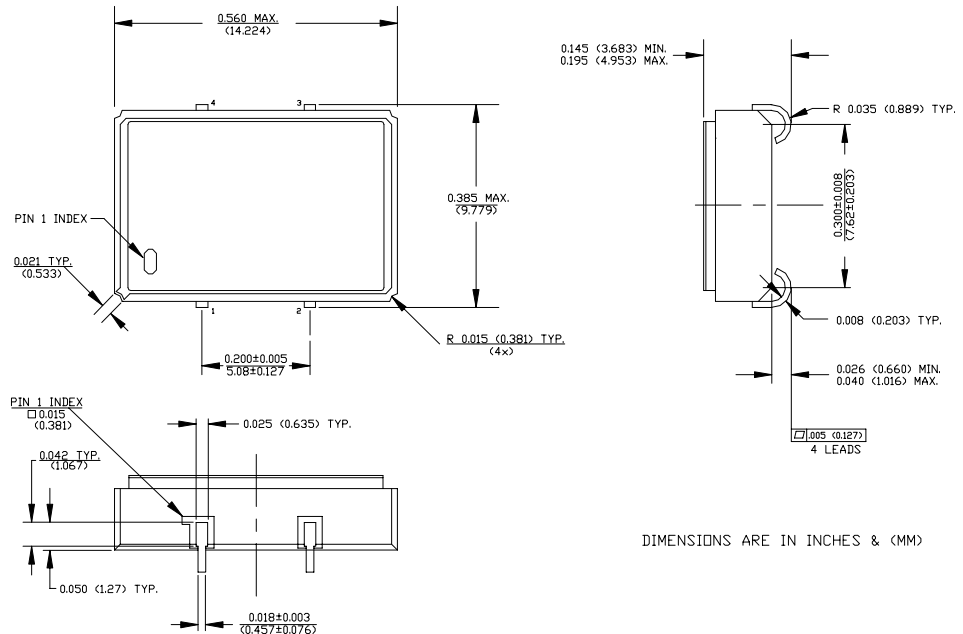
The **SJ-2830 Series** of quartz crystal oscillators provide F 100k series compatible signals in a ceramic SMD package. Systems designers may now specify space-saving, cost-effective packaged ECL oscillators to meet their timing requirements.

### Features

- Wide frequency range—15.0MHz to 250.0MHz
- User specified tolerance available
- Will withstand vapor phase temperatures of 253°C for 4 minutes maximum
- Space-saving alternative to discrete component oscillators
- High shock resistance, to 3000g
- Metal lid electrically connected to ground to reduce EMI
- Low Jitter
- F 100K series compatible output on Pin 3, complement on Pin 1
- High Q Crystal actively tuned oscillator circuit
- Power supply decoupling internal
- No internal PLL avoids cascading PLL problems
- High frequencies due to proprietary design
- Gold plated leads - Solder dipped leads available upon request
- RoHS Compliant, Lead Free Construction (unless solder dipped leads are supplied)

### Electrical Connection

Pin	Connection
1	Output Complement
2	V <sub>EE</sub> -4.5V
3	Output
4	V <sub>CC</sub> Ground



**SJ-2830 Series** Continued  
ECL

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## Operating Conditions and Output Characteristics

### Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	-----	-----	15.0MHz	-----	250.0MHz
Duty Cycle	-----	@ $V_{CC} = -1.29V$	45/55%	-----	55/45%
Logic 0 <sup>(2)</sup>	$V_{OL}$	-----	$V_{CC} - 1.95V$	-----	$V_{CC} - 1.60V$
Logic 1 <sup>(2)</sup>	$V_{OH}$	-----	$V_{CC} - 1.02V$	-----	$V_{CC} - 0.74V$
Rise & Fall Time	tr,tf	20-80% $V_O$ with 50 ohm load to $V_{CC} = -2V$	-----	1.0 ns	1.5 ns
Tpd <sup>(4)</sup>	-----	-----	-0.5 ns	-----	+0.5 ns
Jitter, RMS <sup>(3)</sup>	-----	-----	-----	-----	5 psec
Frequency Stability <sup>(1)</sup>	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100ppm	-----	+100ppm

### General Characteristics

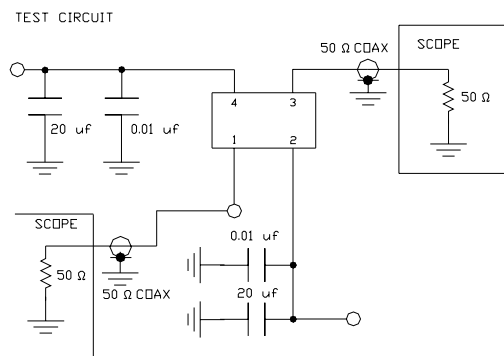
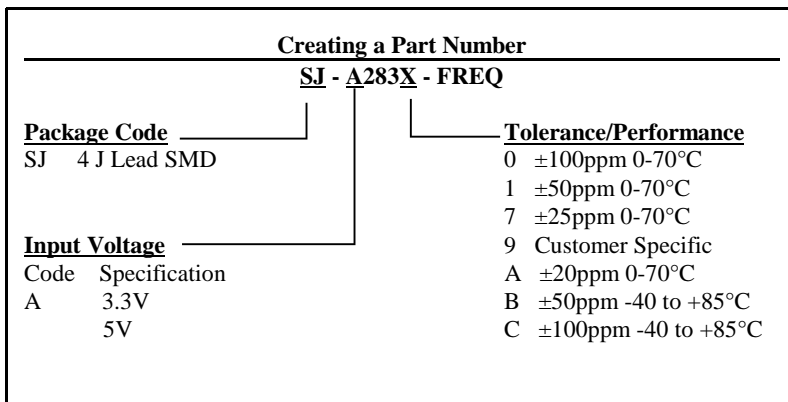
Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	$V_{EE}$	-----	-4.8V	-4.5V	-4.2V
Supply Current	$I_{EE}$	50 ohm termination To 2.00V below $V_{CC}$	0.0 mA	-----	80 mA
Output current	$I_O$	Low level Output Current	0.0 mA	-----	$\pm 50.0$ mA
Operating temperature	$T_A$	-----	0°C	-----	70°C
Storage temperature	$T_S$	-----	-55°C	-----	125°C
Power Dissipation	$P_D$	-----	-----	-----	384 mW
Lead temperature	$T_L$	Soldering, 10 sec.	-----	-----	300°C
Load		50 Ohm to $V_{CC} = -2V$ or Thevenin Equivalent, Bias Required	-----	-----	-----
Start-up time	$t_s$	-----	-----	2 ms	10 ms

### Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55Hz to 2000 Hz
Soldering Condition	300°C for 10 seconds
Hermetic Seal	Leak rate less than $1 \times 10^{-8}$ atm.cc/sec of helium
ESD Sensitivity	Human Body Model per ON Semiconductor 10kH series ECL: 500V min.

#### Footnotes:

- Standard frequency stability ( $\pm 20, \pm 25, \pm 50$ ppm & others available)
- $V_{OL}, V_{OH}$ , referenced to ground ( $V_{CC}$ ) with  $V_{EE} = -4.5V$
- Jitter performance is frequency dependent. Please contact factory for full characterization. RMS jitter bandwidth of 12kHz to 20 MHz.
- Tpd is phase shift between the falling edge of pin 3 at  $V_{CC} = -1.29V$  and rising edge of pin 1 at  $V_{CC} = -1.29V$ .



TEST CIRCUIT USES A SPLIT SUPPLY OF +2V AND -2.5V FOR EASE OF TESTING.