Preliminary

2M X 16 Bit Low Voltage Super RAM™

Features

- Operating voltage: 1.65V to 2.2V
- Access times:
  Address Access , t_{AA} = 70 ns (max.)
  Page Mode Address Access, t_{PAA} = 25ns (max)
- Current:
  Operating Current (Icc2) : 20mA (max.)
  Standby Current (Isb1) : 60uA (max)
  Power Down Standby Current (Isb2) : 10μA (max.)
- Fully SRAM compatible operation
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Support 3 distinct operation modes for reducing standby power :
  Reduced Memory Size Operation (8M,16M,24M,32M)
  Partial Array Refresh (8M,16M,24M)
  Deep Power Down Mode
- Page Mode Read/Write Operation by 8 words
- Industrial operating temperature range: -25°C to +85°C for -I
- Available in 48-ball CSP (6X8) package.

General Description

The A64E16161 is a low operating current 33,554,432-bit Super RAM organized as 2,097,152 words by 16 bits and operates on low power supply voltage from 1.65V to 2.2V. It is built using AMIC's high performance CMOS DRAM process.Using hidden refresh technique, the A64E16161 provides a 100% compatible asynchronous interface.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
This A64E16161 is suited for low power application such as mobile phone and PDA or other battery-operated handheld device.

Pin Configuration

■ **Mini BGA (6X8) Top View**

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O_8	$\overline{HB}$	A3	A4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A5	A6	I/O_1	I/O_2
D	VSS	I/O_{11}	A17	A7	I/O_3	VCC
E	VCC	I/O_{12}	GND	A16	I/O_4	VSS
F	I/O_{14}	I/O_{13}	A14	A15	I/O_5	I/O_6
G	I/O_{15}	A19	A12	A13	$\overline{WE}$	I/O_7
H	A18	A8	A9	A10	A11	A20

A64E16161G