SIEMENS

IL4108

ZERO VOLTAGE CROSSING 800 V TRIAC DRIVER OPTOCOUPLER

FEATURES

- **On-State Current, 300 mA**
- **Zero Voltage Crossing**
- **Blocking Voltage, 800 V**
- **Isolation Test Voltage 5300 VACRMS**
- **High Input Sensitivity**
  IFT=2 mA, PF=1.0
  IFT=5 mA, PF≤1.0
- **High Static dv/dt 10,000 V/μs**
- **Inverse Parallel SCRs Provide Commutating dv/dt >10K V/μs**
- **Very Low Leakage <10 μA**
- **Small 6-Pin DIP Package**
- **Underwriters Lab File #E52744**
- **VDE Approval #0884 (Optional with Option 1, Add -X001 Suffix)**

Maximum Ratings

Emitter

Reverse Voltage ..... 6 V
Forward Current ..... 60 mA
Surge Current ..... 2.5 A
Thermal Resistance ..... 750 °C/W
Derate from 25°C ..... 1.33 mW/°C

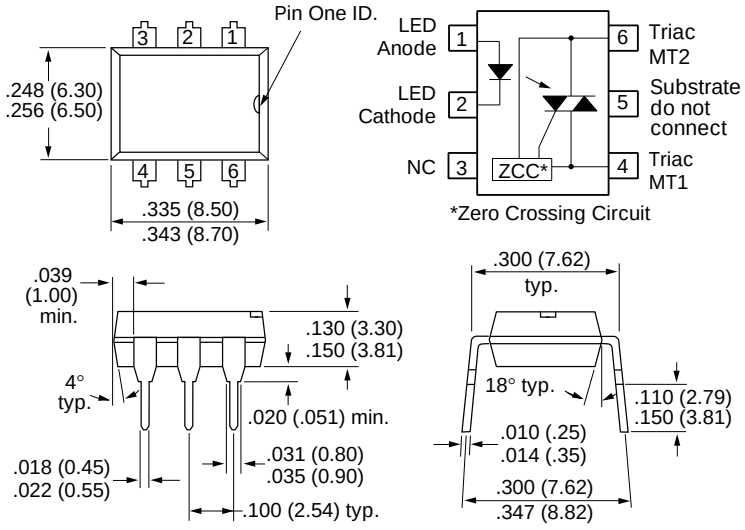
Detector

Peak Off-state Voltage ..... 800 V
Peak Reverse Voltage ..... 800 V
RMS On-state Current ..... 300 mA
Single Cycle Surge ..... 3 A
Thermal Resistance ..... 125 °C/W
Total Power Dissipation ..... 500 mW
Derate from 25°C ..... 6.6 mW/°C

Package

Isolation Test Voltage (between emitter and detector, climate per DIN 40046, part 2, Nov. 74 (t=1 min.) ..... 5300 VAC_{RMS}
Pollution Degree (DIN VDE 0109) 2
Creepage Distance ..... ≥7 mm
Clearance ..... ≥7 mm
Comparative Tracking Index per DIN IEC 112/VDE 0303 part 1, Group IIIa per DIN VDE 6110 ..... ≥175
Isolation Resistance
V_{IO}=500 V, T_A=25°C ..... $\geq 10^{12}\ \Omega$
V_{IO}=500 V, T_A=100°C ..... $\geq 10^{11}\ \Omega$
Storage Temperature Range ..... –55°C to +125°C
Ambient Temperature Range ..... –55°C to +100°C
Soldering Temperature (max. ≤10 sec. dip soldering ≥0.5 mm from case bottom) ..... 260°C

Package Dimensions in inches (mm)



DESCRIPTION

The IL4108 consists of a GaAs IRLED optically coupled to a photosensitive zero crossing TRIAC network. The TRIAC consists of two inverse parallel connected monolithic SCRs. These three semiconductors are assembled in a six pin 0.3 inch dual in-line package, using high insulation double molded, over/under leadframe construction.

High input sensitivity is achieved by using an emitter follower phototransistor and a cascaded SCR predriver resulting in an LED trigger current of less than 2 mA (DC).

The IL4108 uses two discrete SCRs resulting in a commutating dV/dt greater than 10KV/μs. The use of a proprietary dv/dt clamp results in a static dV/dt of greater than 10KV/μs. This clamp circuit has a MOSFET that is enhanced when high dV/dt spikes occur between MT1 and MT2 of the TRIAC. When conducting, the FET clamps the base of the phototransistor, disabling the first stage SCR predriver.

The zero cross line voltage detection circuit consists of two enhancement MOSFETS and a photodiode. The inhibit voltage of the network is determined by the enhancement voltage of the N-channel FET. The P-channel FET is enabled by a photocurrent source that permits the FET to conduct the main voltage to gate on the N-channel FET. Once the main voltage can enable the N-channel, it clamps the base of the phototransistor, disabling the first stage SCR predriver.

The 800V blocking voltage permits control of off-line voltages up to 240VAC, with a safety factor of more than two, and is sufficient for as much as 380VAC.

The IL4108 isolates low-voltage logic from 120, 240, and 380 VAC lines to control resistive, inductive, or capacitive loads including motors, solenoids, high current thyristors or TRIAC and relays.

Applications include solid-state relays, industrial controls, office equipment, and consumer appliances.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Emitter						
Forward Voltage	V_F		1.16	1.35	V	I_F=10 mA
Breakdown Voltage	V_{BR}	6	30		V	I_R=10 µA
Reverse Current	I_R		0.1	10	µA	V_R=6 V
Capacitance	C_0		25		pF	V_F=0 V, f=1 MHz
Thermal Resistance, Junction to Lead	R_{THJL}		750		°C/W	
Output Detector						
Repetitive Peak Off-state Voltage	V_{DRM}	800			V	I_{DRM}=100 µA
Off-state Voltage	$V_{D(RMS)}$	565			V	$I_{D(RMS)}$=70 µA
Off-state Current	$I_{D(RMS)1}$		10	100	µA	V_D=800 V, T_A100°C, I_F=0 mA
Off-state Current	$I_{D(RMS)2}$			200	µA	V_D=800 V, I_F=Rated I_{FT}
On-state Voltage	V_{TM}		1.7	3	V	I_T=300 mA
On-state Current	I_{TM}			300	mA	PF=1.0, $V_{T(RMS)}$=1.7 V
Surge (Non-repetitive On-state Current)	I_{TSM}			3	A	f=50 Hz
Trigger Current 1	I_{FT1}			2.0	mA	V_D=5 V
Trigger Current 2	I_{FT2}			6.0	mA	V_{op}=220 V, f=50 Hz, T_j=100°C, t_{pF}>10 ms
Trigger Current Termperature Gradient	$\Delta I_{FT1}/\Delta T_j$ $\Delta I_{FT2}/\Delta T_j$		7 7	14 14	µA/K µA/K	
Inhibit Voltage Temperature Gradient	$\Delta V_{DINH}/\Delta T_j$		–20		mV/K	
Off-state Current in Inhibit State	I_{DINH}		50	200	µA	I_F=I_{FT1}, V_{DRM}
Capacitance between Input and Output Circuit	C_{IO}		2.0		pF	V_D=0, f=1 kHz
Holding Current	I_H		65	500	µA	
Latching Current	I_L		5		mA	V_T=2.2 V
Zero Cross Inhibit Voltage	V_{IH}		15	25	V	I_F=Rated I_{FT}
Turn-on Time	t_{ON}		35		µs	V_{RM}=V_{DM}=565 VAC
Turn-off Time	t_{OFF}		50		µs	PF=1.0, I_T=300 mA
Critical Rate of Rise of Off-State Voltage	dv/dt_{cr} dv/dt_{cr}	10000 5000			V/µs V/µs	V_D=0.67 V_{DRM}, T_j=25°C T_j=80°C
Critical Rate of Rise of Voltage at Current Commutation	 dv/dt_{crq} dv/dt_{crq}	 10000 5000			 V/µs V/µs	V_D=0.67 V_{DRM}, di/dt_{crq}<15 A/ms T_j=25°C T_j=80°C
Critical Rate of Rise of On-state Current	$di/dt/_{cr}$			8	A/µs	
Thermal Resistance, Junction to Lead	R_{THJL}		150		°C/W	
Package						
Critical Rate of Rise of Coupled Input/Output Voltage	$dv_{(IO)}/dt$		10000		V/µs	I_T=0 A, V_{RM}=V_{DM}=565 VAC
Common Mode Coupling Capacitor	C_{CM}		0.01		pF	
Package Capacitance	C_{IO}		0.8		pF	f=1 MHz, V_{IO}=0 V