

1GB – 128Mx72 DDR2 SDRAM RDIMM, VLP

FEATURES

- VLP (very low profile) 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4300 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5* and 6*
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- Auto & self refresh (64ms: 8,192 cycle refresh)
- Gold edge contacts
- RoHS compliant
- Package option
 - 240 Pin DIMM VLP
 - PCB – 18.29mm (0.720") Max

DESCRIPTION

The WV3HG128M72AER is a 128Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of eighteen 128Mx4 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a VLP 240-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

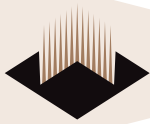
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4300	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t _{RCD} -t _{RP}	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability



PIN CONFIGURATION

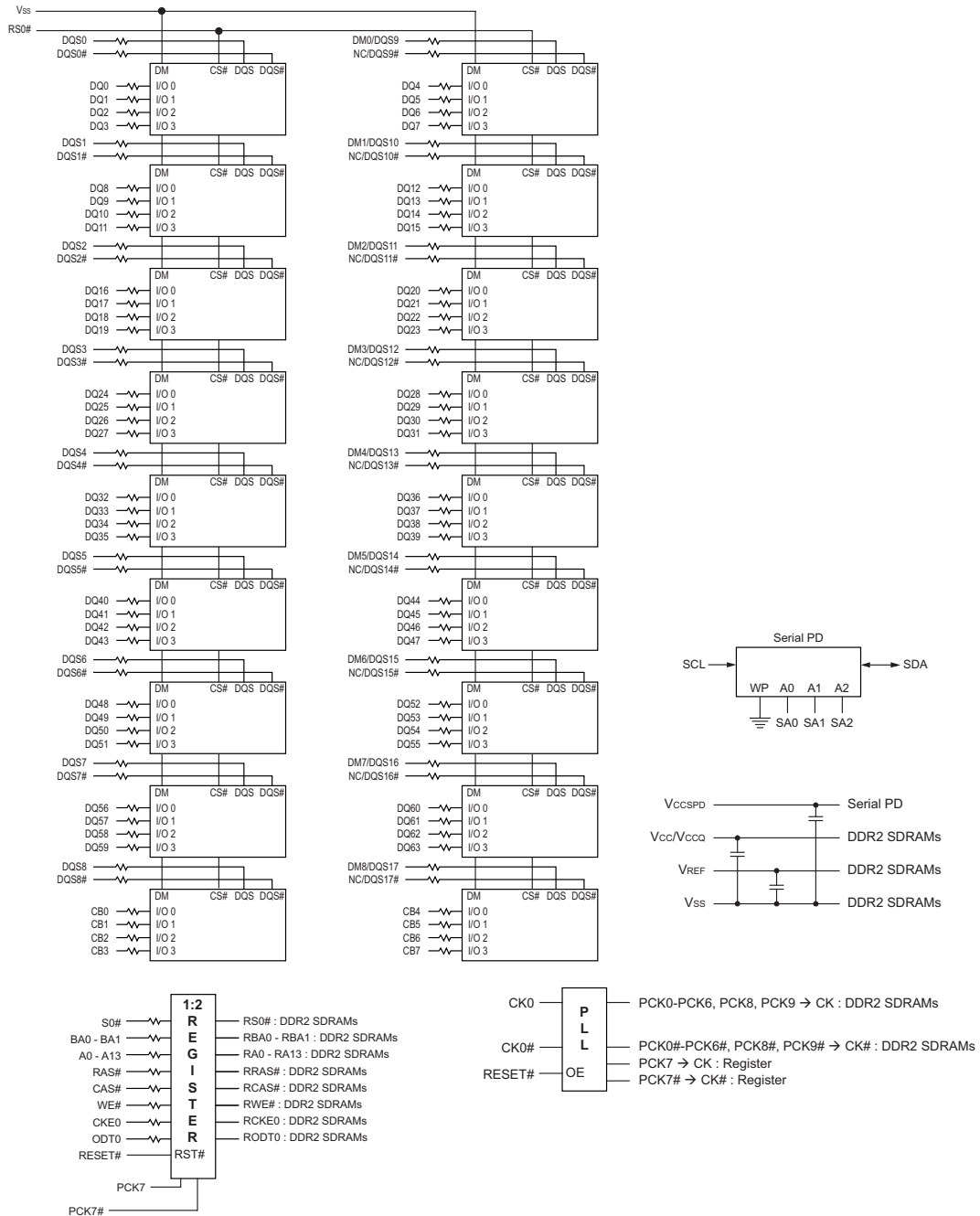
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	61	A4	121	Vss	181	Vccq
2	Vss	62	Vccq	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	Vcc	124	Vss	184	Vcc
5	Vss	65	Vss	125	DM0/DQS9	185	CK0
6	DQS0#	66	Vss	126	NC/DQS9#	186	CK0#
7	DQS0	67	Vcc	127	Vss	187	Vcc
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	Vcc	129	DQ7	189	Vcc
10	DQ3	70	A10/AP	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	Vccq
12	DQ8	72	Vccq	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	S0#
14	Vss	74	CAS#	134	DM1/DQS10	194	Vccq
15	DQS1#	75	Vccq	135	NC/DQS10#	195	ODT0
16	DQS1	76	NC	136	Vss	196	A13
17	Vss	77	NC	137	NC	197	Vcc
18	RESET#	78	Vccq	138	NC	198	Vss
19	NC	79	Vss	139	Vss	199	DQ36
20	Vss	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	Vss
22	DQ11	82	Vss	142	Vss	202	DM4/DQS13
23	Vss	83	DQS4#	143	DQ20	203	NC/DQS13#
24	DQ16	84	DQS4	144	DQ21	204	Vss
25	DQ17	85	Vss	145	Vss	205	DQ38
26	Vss	86	DQ34	146	DM2/DQS11	206	DQ39
27	DQS2#	87	DQ35	147	NC/DQS11#	207	Vss
28	DQS2	88	Vss	148	Vss	208	DQ44
29	Vss	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	Vss
31	DQ19	91	Vss	151	Vss	211	DM5/14
32	Vss	92	DQS5#	152	DQ28	212	NC/DQS14#
33	DQ24	93	DQS5	153	DQ29	213	Vss
34	DQ25	94	Vss	154	Vss	214	DQ46
35	Vss	95	DQ42	155	DM3/DQS12	215	DQ47
36	DQS3#	96	DQ43	156	NC/DQS12#	216	Vss
37	DQS3	97	Vss	157	Vss	217	DQ52
38	Vss	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	Vss
40	DQ27	100	Vss	160	Vss	220	NC
41	Vss	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	Vss
43	CB1	103	Vss	163	Vss	223	DM6/DQS15
44	Vss	104	DQS6#	164	DM8/DQS17	224	NC/DQS15#
45	DQS8#	105	DQS6	165	NC/DQS17#	225	Vss
46	DQS8	106	Vss	166	Vss	226	DQ54
47	Vss	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	Vss
49	CB3	109	Vss	169	Vss	229	DQ60
50	Vss	110	DQ56	170	Vccq	230	DQ61
51	Vccq	111	DQ57	171	NC	231	Vss
52	CKE0	112	Vss	172	Vcc	232	DM7/DQS16
53	Vcc	113	DQS7#	173	NC	233	NC/DQS16#
54	NC	114	DQS7	174	NC	234	Vss
55	NC	115	Vss	175	Vccq	235	DQ62
56	Vccq	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	Vss
58	A7	118	Vss	178	Vcc	238	VccSPD
59	Vcc	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

PIN NAMES

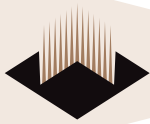
Pin Name	Function
CK0,CK0#	Clock Inputs
CKE0	Clock Enable
CB0-CB7	Check Bits
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
S0#	Chip Select
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
ODT0	On-die termination control
SCL	SPD Clock Input
SDA	SPD Data Input/Output
SA0-SA2	SPD address
DQ0-DQ63	Data Input/Output
DM0-DM8	Data Masks
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
Vcc, Vccq	Core and I/O Power
Vss	Ground
VREF	Input/Output Reference
VccSPD	SPD Power
NC	No connect
RESET#	Reset Input



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.



DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	3
I/O Reference Voltage	V _{REF}	0.49 x V _{CC}	0.50 x V _{CC}	0.51 x V _{CC}	V	1
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	2
SPD Supply Voltage	V _{CCSPD}	1.7	-	3.6	V	

Notes:

- V_{REF} is expected to equal V_{CC/2} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCQ} of all IC's are tied to V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-0.5	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
I _L	Input leakage current; Any input 0V<V _{IN} <V _{CC} ; V _{REF} input 0V,V _{IN} ,0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#,	-5	5	μA
		CK, CK#	-10	10	μA
		DM	-2	2	μA
I _{OZ}	Output leakage current; 0V<V _{IN} <V _{CC} ; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	μA
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-36	36	μA	
PD	Power dissipation	18		W	

CAPACITANCE

T_A = 25°C, f = 100MHz, V_{CC} = V_{CCQ} = 1.8V

Parameter	Symbol	Max	Units
Input Capacitance: CK, CK#	C _{CK}	11	pF
Input Capacitance: KE, CS#	C _{I1}	12	pF
Input Capacitance: Addr. RAS#, CAS#, WE#	C _{I2}	12	pF
Input/Output Capacitance: DQ, DQS, DM, DQS#	C _{IO}	10	pF

Note: Based on **SAMSUNG** components



OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating Case Temperature (Commercial)	TOPER	0 to +85°C	°C	1, 2

- NOTE:
1. Operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
 2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{CC} + 0.300	V
Input High (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	V _{IH} (AC)	V _{REF} + 0.250	-	V
AC Input High (Logic 0) Voltage	V _{IL} (AC)	-	V _{REF} - 0.250	V

INPUT/OUTPUT CAPACITANCE

T_A=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (0A~A13, BA0~BA1, RAS#, CAS#, WE#)	C _{IN1}	6.5	7.5	pF
Input capacitance (CKE0), (ODT0)	C _{IN2}	6.5	7.5	pF
Input capacitance (CS0#)	C _{IN3}	6.5	7.5	pF
Input capacitance (CK0, CK0#)	C _{IN4}	6	7	pF
Input capacitance (DQS0 ~ DQS17, DQS0# ~ DQS17#)	C _{IN5} (534, 403)	6.5	8	pF
Input capacitance (DQ0~DQ63), (CB0~CB7)	C _{OUT1} (534, 403)	6.5	8	pF

Notes: Based on **ELPIDA** components

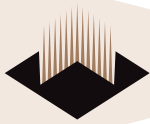


DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

V_{CC} = +1.8V ± 0.1V

Symbol	Proposed Conditions	534	403	Units	
I _{CC0}	Operating one bank active-precharge current; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2,420	2,250	mA	
I _{CC1}	Operating one bank active-read-precharge current; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}), t _{RCD} = t _{RCD} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{DAD6W}	2,640	2,400	mA	
I _{CC2P}	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	784	724	mA	
I _{CC2Q}	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	1,110	1,040	mA	
I _{CC2N}	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1,090	1,130	mA	
I _{CC3P}	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	1,190	1,190	mA
		Slow PDN Exit MRS(12) = 1	600	570	mA
I _{CC3N}	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1,840	1,730	mA	
I _{DAD6W}	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	3,820	2,900	mA	
I _{DAD6R}	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{DAD6W}	3,590	3,000	mA	
I _{CC5B}	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{RFC} (I _{CC}) interval; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	4,150	3,880	mA	
I _{CC6}	Self refresh current; CK and CK1 at 0V; CE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	99	99	mA	
I _{CC7}	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RCD} (I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I _{DAD6R} ; Refer to the following page for detailed timing conditions	5,900	5,570	mA	

Note: I_{CC} specification is based on **SAMSUNG** components. Other DRAM Manufacturers specification may be different.



DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

V_{CC} = +1.8V ± 0.1V

Symbol	Proposed Conditions	534	403	Units	
I _{CC0}	Operating one bank active-precharge current; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2,390	2,120	mA	
I _{CC1}	Operating one bank active-read-precharge current; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}), t _{RCD} = t _{RCD} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{DAD6W}	2,660	2,390	mA	
I _{CC2P}	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	680	644	mA	
I _{CC2Q}	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	950	860	mA	
I _{CC2N}	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1,040	950	mA	
I _{CC3P}	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	1,220	1,130	mA
		Slow PDN Exit MRS(12) = 1	950	860	mA
I _{CC3N}	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1,670	1,580	mA	
I _{DAD6W}	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	3,560	3,020	mA	
I _{DAD6R}	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{DAD6W}	3,560	3,020	mA	
I _{CC5B}	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{RFC} (I _{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	5,000	4,640	mA	
I _{CC6}	Self refresh current; CK and CKl at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	108	108	mA	
I _{CC7}	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RCD} (I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I _{DAD6R} ; Refer to the following page for detailed timing conditions	5,900	5,540	mA	

Note: I_{CC} specification is based on **ELPIDA** components. Other DRAM Manufacturers specification may be different.



AC TIMING PARAMETERS

V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS			534		403			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 4	t _{CK (4)}	3,750	8,000	5,000	8,000	ps
		CL = 3	t _{CK (3)}	5,000	8,000	5,000	8,000	ps
	CK high-level width		t _{CH}	0.45	0.55	0.45	0.55	t _{CK}
	CK low-level width		t _{CL}	0.45	0.55	0.45	0.55	t _{CK}
	Half clock period		t _{HP}	MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		ps
	Clock jitter		t _{JT}	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t _{AC}	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t _{HZ}		t _{AC} MAX		t _{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t _{LZ}	t _{AC} MIN	t _{AC} MAX	t _{AC} MIN	t _{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t _{DS}	100		150		ps
	DQ and DM input hold time relative to DQS		t _{DH}	225		275		ps
	A DQ and DM input pulse width (for each input)		t _{DLPW}	0.35		0.35		t _{CK}
	Data hold skew factor		t _{QHS}		400		450	ps
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access		t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps
	Data valid output window (DVW)		t _{DVW}	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns
Data Strobe	DQS input high pulse width		t _{DQSH}	0.35		0.35		t _{CK}
	DQS input low pulse width		t _{DQSL}	0.35		0.35		t _{CK}
	DQS output access time from CK/CK#		t _{DQSCK}	-450	+450	-500	+500	ps
	DQS falling edge to CK rising ... setup time		t _{DSS}	0.2		0.2		t _{CK}
	DQS falling edge from CK rising ... hold time		t _{DSH}	0.2		0.2		t _{CK}
	DQS...DQ skew, DQS to last DQ valid, per group, per access		t _{DQSQ}		300		350	ps
	DQS read preamble		t _{RPRE}	0.9	1.1	0.9	1.1	t _{CK}
	DQS read postamble		t _{RPST}	0.4	0.6	0.4	0.6	t _{CK}
	DQS write preamble setup time		t _{WPRES}	0		0		ps
	DQS write preamble		t _{WPRE}	0.35		0.35		t _{CK}
	DQS write postamble		t _{WPST}	0.4	0.6	0.4	0.6	t _{CK}
	Write command to first DQS latching transition		t _{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t _{CK}

Continued on next page



AC TIMING PARAMETERS (cont'd)

V_{CC} = +1.8V ± 0.1V

AC CHARACTERISTICS			534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNIT
Command and Address	Address and control input pulse width for each input	t _{IPW}	0.6		0.6		t _{CK}
	Address and control input setup time	t _{IS}	250		350		ps
	Address and control input hold time	t _{IH}	375		475		ps
	CAS# to CAS# command delay	t _{CCD}	2		2		t _{CK}
	ACTIVE to ACTIVE (same bank) command	t _{RC}	60		55		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCD}	15		15		ns
	Four Bank Activate period	t _{FAW}	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	45	70,000	40	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	7.5		7.5		ns
	6 Write recovery time	t _{WR}	15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	t _{WR} + t _{RP}		t _{WR} + t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	7.5		10		ns
	PRECHARGE command period	t _{RP}	15		15		ns
	PRECHARGE ALL command period	t _{RPA}	t _{RP} +t _{CK}		t _{RP} +t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	2		2		t _{CK}
	OCD Drive mode delay	t _{OLT}	0	12	0	12	ns
	CKE low to CK,CK# uncertainty	t _{DELAY}	t _{IS} + t _{CK} + t _{IH}		t _{IS} + t _{CK} + t _{IH}		ns
Refresh	REFRESH to REFRESH command interval	t _{RFC}	105	70,000	105	70,000	ns
	Average periodic refresh interval	t _{REFI}		7.8		7.8	μs
Self Refresh	Exit self refresh to non-READ command	t _{XSNR}	t _{RFC} (MIN) + 10		t _{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t _{XSRD}	200		200		t _{CK}
	Exit self refresh timing reference	t _{ISXR}	t _{IS}		t _{IS}		ps
	Exit self refresh timing reference	t _{ISXR}	250		350		ps
ODT	ODT turn-on delay	t _{AO_{ND}}	2	2	2	2	t _{CK}
	ODT turn-on	t _{AO_N}	t _{AC} (MIN)	t _{AC} (MAX) + 1000	t _{AC} (MIN)	t _{AC} (MAX) + 1000	ps
	ODT turn-off delay	t _{AO_{FD}}	2.5	2.5	2.5	2.5	t _{CK}
	ODT turn-off	t _{AO_F}	t _{AC} (MIN)	t _{AC} (MAX) + 600	t _{AC} (MIN)	t _{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t _{AO_{NP_D}}	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t _{AO_{FP_D}}	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	t _{AC} (MIN) + 2000	2.5 x t _{CK} + t _{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t _{AN_{PD}}	3		3		t _{CK}
	ODT power-down exit latency	t _{AX_{PD}}	8		8		t _{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	2		2		t _{CK}
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	6 - AL		6 - AL		t _{CK}
	A Exit precharge power-down to any non-READ command.	t _{XP}	2		2		t _{CK}
	CKE minimum high/low time	t _{CKE}	3		3		t _{CK}



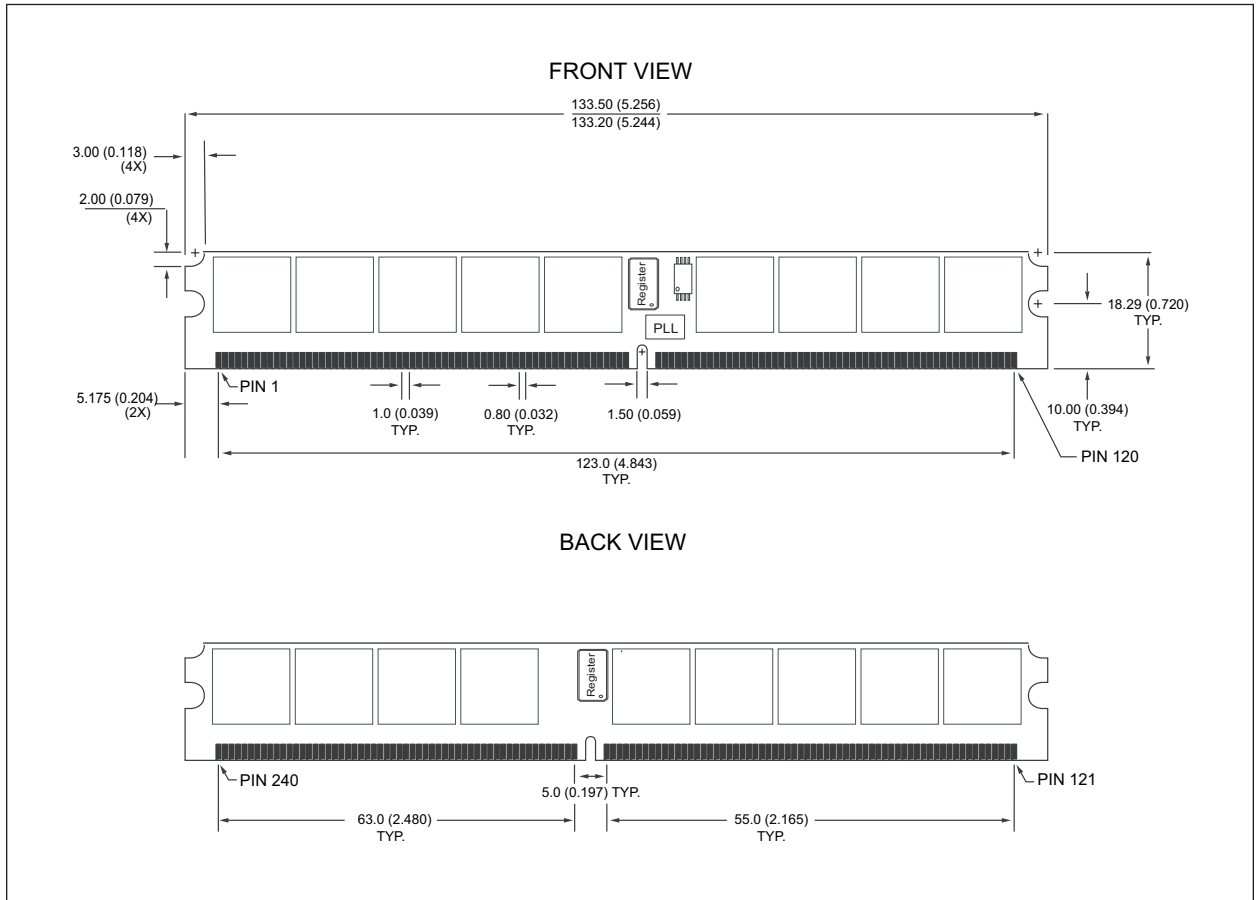
ORDERING INFORMATION FOR AD6

Part Number	Speed/Data Rate	CAS Latency	t _{RCD}	t _{RP}	Height*
WV3HG128M72AER534AD6xxG	266MHz/533Mb/s	4	4	4	18.29mm (0.72")
WV3HG128M72AER403AD6xxG	200MHz/400Mb/s	3	3	3	18.29mm (0.72")

NOTES:

- RoHS products. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options.
(E = Elpida, M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

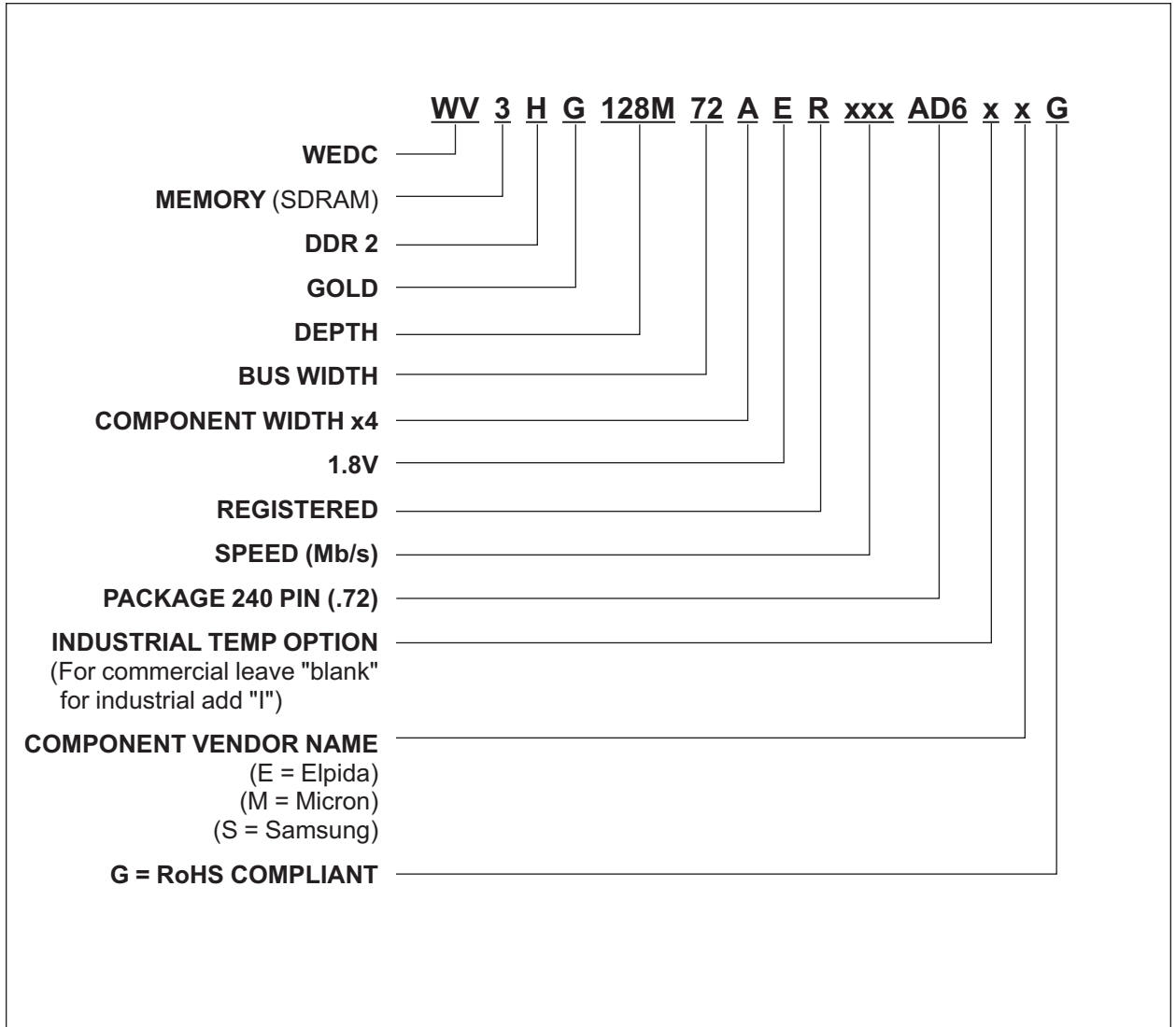
PACKAGE DIMENSIONS FOR AD6

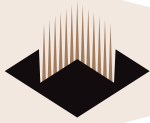


* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE



**Document Title**

1GB – 128Mx72 DDR2 SDRAM REGISTERED, w/PLL

DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q3'06
- MICRON: U27Y: B-Die, will move to U37Y: D-Die Q4"06
- ELPIDA: E-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	March 2005	Advanced
Rev 1	1.0 Updated "Absolute Maximum Ratings"	April 2006	Advanced
	1.1 Added Elpida "CAP" specifications		
	1.2 Added Elpida "Icc" specifications		
	1.3 Updated "AC Timing Parameters"		
	1.4 Added Elpida to part marking info & number guide		
	1.5 Added "Industrial Temperature" to part numbering guide		
	1.6 Added DRAM die rev option		